

## Programmable Timing Control Hub™ for Next Gen P4™ processor

### Recommended Application:

CK410 compliant clock

### Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 6 - 0.7V current-mode differential SRC pair
- 1 - 0.7V current-mode differential CPU\_ITP/SRC selectable pair
- 6 - PCI (33MHz)
- 3 - PCICLK\_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, 14.318MHz

### Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 85ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

### Features/Benefits:

- Programmable output frequencies
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Programmable watch dog safe frequency.
- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, 0 to -0.5% down spread, ±0.25% center spread, and ±0.3% center spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.

### Functionality

| Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | CPU    | SRC    | SATA   | PCI   |
|------|------|------|------|------|--------|--------|--------|-------|
|      |      | FSLC | FSLB | FSLA | MHz    | MHz    | MHz    | MHz   |
| 0    | 0    | 0    | 0    | 0    | 266.66 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 0    | 0    | 1    | 133.33 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 0    | 1    | 0    | 200.00 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 0    | 1    | 1    | 166.66 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 1    | 0    | 0    | 333.33 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 1    | 0    | 1    | 100.00 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 1    | 1    | 0    | 400.00 | 100.00 | 100.00 | 33.33 |
| 0    | 0    | 1    | 1    | 1    | 200.00 | 100.00 | 100.00 | 33.33 |
| 0    | 1    | 0    | 0    | 0    | 266.66 | 133.33 | 133.33 | 33.33 |
| 0    | 1    | 0    | 0    | 1    | 133.33 | 133.33 | 133.33 | 33.33 |
| 0    | 1    | 0    | 1    | 0    | 200.00 | 133.33 | 133.33 | 33.33 |
| 0    | 1    | 0    | 1    | 1    | 166.66 | 125.00 | 125.00 | 33.33 |
| 0    | 1    | 1    | 0    | 0    | 333.33 | 125.00 | 125.00 | 33.33 |
| 0    | 1    | 1    | 0    | 1    | 100.00 | 133.33 | 133.33 | 33.33 |
| 0    | 1    | 1    | 1    | 0    | 400.00 | 133.33 | 133.33 | 33.33 |
| 0    | 1    | 1    | 1    | 1    | 200.00 | 133.33 | 133.33 | 33.33 |
| 1    | 0    | 0    | 0    | 0    | 269.33 | 101.00 | 101.00 | 33.67 |
| 1    | 0    | 0    | 0    | 1    | 134.66 | 101.00 | 101.00 | 33.67 |
| 1    | 0    | 0    | 1    | 0    | 202.00 | 101.00 | 101.00 | 33.67 |
| 1    | 0    | 0    | 1    | 1    | 168.33 | 101.00 | 101.00 | 33.67 |
| 1    | 0    | 1    | 0    | 0    | 274.66 | 103.00 | 103.00 | 34.33 |
| 1    | 0    | 1    | 0    | 1    | 137.33 | 103.00 | 103.00 | 34.33 |
| 1    | 0    | 1    | 1    | 0    | 206.00 | 103.00 | 103.00 | 34.33 |
| 1    | 0    | 1    | 1    | 1    | 171.66 | 103.00 | 103.00 | 34.33 |
| 1    | 1    | 0    | 0    | 0    | 279.99 | 105.00 | 105.00 | 35.00 |
| 1    | 1    | 0    | 0    | 1    | 140.00 | 105.00 | 105.00 | 35.00 |
| 1    | 1    | 0    | 1    | 0    | 210.00 | 105.00 | 105.00 | 35.00 |
| 1    | 1    | 0    | 1    | 1    | 174.99 | 105.00 | 105.00 | 35.00 |
| 1    | 1    | 1    | 0    | 0    | 287.99 | 108.00 | 108.00 | 36.00 |
| 1    | 1    | 1    | 0    | 1    | 144.00 | 108.00 | 108.00 | 36.00 |
| 1    | 1    | 1    | 1    | 0    | 216.00 | 108.00 | 108.00 | 36.00 |
| 1    | 1    | 1    | 1    | 1    | 179.99 | 108.00 | 108.00 | 36.00 |

### Pin Configuration

|                  |    |    |                        |
|------------------|----|----|------------------------|
| VDDPCI           | 1  | 56 | PCICLK2                |
| GND              | 2  | 55 | PCICLK1                |
| PCICLK3          | 3  | 54 | PCICLK0                |
| PCICLK4          | 4  | 53 | FS_C                   |
| PCICLK5          | 5  | 52 | REFOUT                 |
| GND              | 6  | 51 | GND                    |
| VDDPCI           | 7  | 50 | X1                     |
| ITP_EN/PCICLK_F0 | 8  | 49 | X2                     |
| PCICLK_F1        | 9  | 48 | VDDREF                 |
| PCICLK_F2        | 10 | 47 | SDATA                  |
| VDD48            | 11 | 46 | SCLK                   |
| USB_48MHz        | 12 | 45 | GND                    |
| GND              | 13 | 44 | CPUCLKT0               |
| DOTT_96MHz       | 14 | 43 | CPUCLKC0               |
| DOTC_96MHz       | 15 | 42 | VDDCPU                 |
| FS_B             | 16 | 41 | CPUCLKT1               |
| Vtt_PwrGd#/PD    | 17 | 40 | CPUCLKC1               |
| FS_A             | 18 | 39 | IREF                   |
| SRCCLKT1         | 19 | 38 | GNDA                   |
| SRCCLKC1         | 20 | 37 | VDDA                   |
| VDDSRC           | 21 | 36 | CPUCLKT2_ITP/SRCCLKT_7 |
| SRCCLKT2         | 22 | 35 | CPUCLKC2_ITP/SRCCLKC_7 |
| SRCCLKC2         | 23 | 34 | VDDSRC                 |
| SRCCLKT3         | 24 | 33 | SRCCLKT6               |
| SRCCLKC3         | 25 | 32 | SRCCLKC6               |
| SRCCLKT4_SATA    | 26 | 31 | SRCCLKT5               |
| SRCCLKC4_SATA    | 27 | 30 | SRCCLKC5               |
| VDDSRC           | 28 | 29 | GND                    |

### 56-Pin SSOP and TSSOP

\* Internal Pull-Up Resistor

\*\* Internal Pull-Down Resistor

## Pin Description

| PIN # | PIN NAME         | TYPE | DESCRIPTION                                                                                                                                                                                                                                                   |
|-------|------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VDDPCI           | PWR  | Power supply for PCI clocks, nominal 3.3V                                                                                                                                                                                                                     |
| 2     | GND              | PWR  | Ground pin.                                                                                                                                                                                                                                                   |
| 3     | PCICLK3          | OUT  | PCI clock output.                                                                                                                                                                                                                                             |
| 4     | PCICLK4          | OUT  | PCI clock output.                                                                                                                                                                                                                                             |
| 5     | PCICLK5          | OUT  | PCI clock output.                                                                                                                                                                                                                                             |
| 6     | GND              | PWR  | Ground pin.                                                                                                                                                                                                                                                   |
| 7     | VDDPCI           | PWR  | Power supply for PCI clocks, nominal 3.3V                                                                                                                                                                                                                     |
| 8     | ITP_EN/PCICLK_F0 | I/O  | Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality<br>1 = CPU_ITP pair<br>0 = SRC pair                                                                                                                       |
| 9     | PCICLK_F1        | OUT  | Free running PCI clock not affected by PCI_STOP#.                                                                                                                                                                                                             |
| 10    | PCICLK_F2        | OUT  | Free running PCI clock not affected by PCI_STOP#.                                                                                                                                                                                                             |
| 11    | VDD48            | PWR  | Power pin for the 48MHz output.3.3V                                                                                                                                                                                                                           |
| 12    | USB_48MHz        | OUT  | 48.00MHz USB clock                                                                                                                                                                                                                                            |
| 13    | GND              | PWR  | Ground pin.                                                                                                                                                                                                                                                   |
| 14    | DOTT_96MHz       | OUT  | True clock of differential pair for 96.00MHz DOT clock.                                                                                                                                                                                                       |
| 15    | DOTC_96MHz       | OUT  | Complement clock of differential pair for 96.00MHz DOT clock.                                                                                                                                                                                                 |
| 16    | FSLB             | IN   | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.                                                                                                                                      |
| 17    | Vtt_PwrGd#/PD    | IN   | Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped. |
| 18    | FSLA             | IN   | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.                                                                                                                                      |
| 19    | SRCCLKT1         | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 20    | SRCCLKC1         | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 21    | VDDSRC           | PWR  | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                                           |
| 22    | SRCCLKT2         | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 23    | SRCCLKC2         | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 24    | SRCCLKT3         | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                                                    |
| 25    | SRCCLKC3         | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                                              |
| 26    | SRCCLKT4_SATA    | OUT  | True clock of differential SRC/SATA pair.                                                                                                                                                                                                                     |
| 27    | SRCCLKC4_SATA    | OUT  | Complement clock of differential SRC/SATA pair.                                                                                                                                                                                                               |
| 28    | VDDSRC           | PWR  | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                                           |

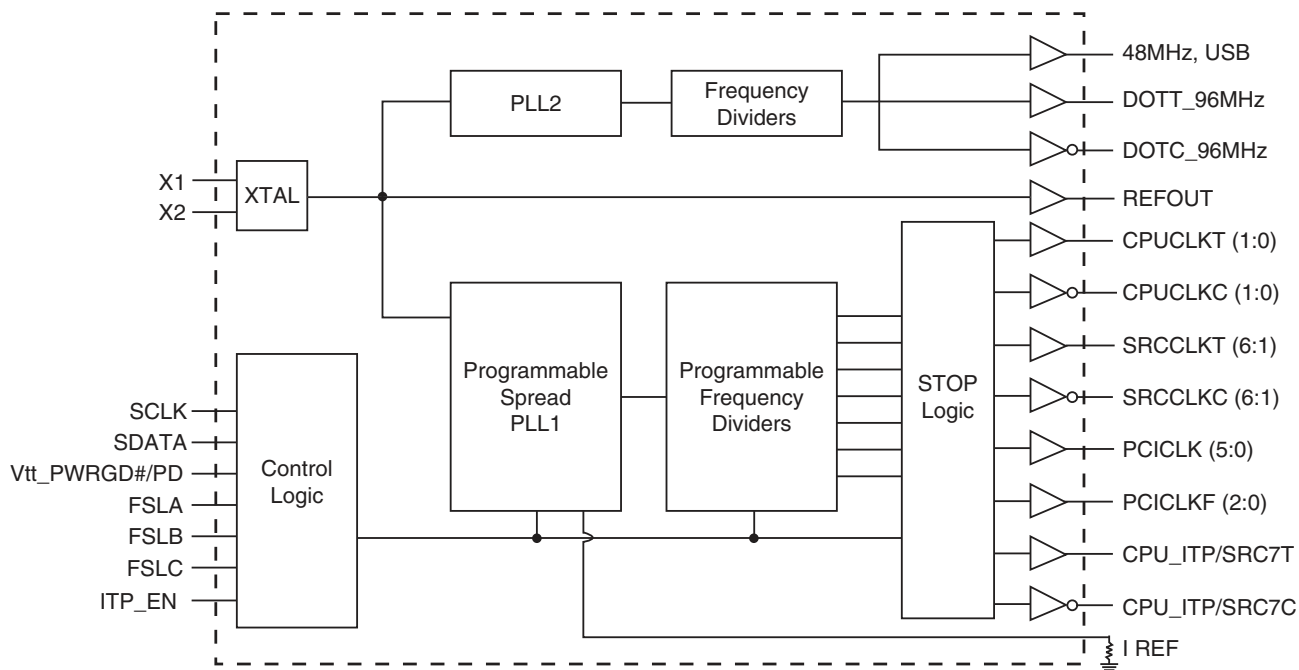
## Pin Description

| PIN # | PIN NAME               | TYPE | DESCRIPTION                                                                                                                                                                                                                           |
|-------|------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 30    | SRCCLKC5               | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                      |
| 31    | SRCCLKT5               | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                            |
| 32    | SRCCLKC6               | OUT  | Complement clock of differential SRC clock pair.                                                                                                                                                                                      |
| 33    | SRCCLKT6               | OUT  | True clock of differential SRC clock pair.                                                                                                                                                                                            |
| 34    | VDDSRC                 | PWR  | Supply for SRC clocks, 3.3V nominal                                                                                                                                                                                                   |
| 35    | CPUCLKC2_ITP/SRCCLKC_7 | OUT  | Complimentary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.                                                  |
| 36    | CPUCLKT2_ITP/SRCCLKT_7 | OUT  | True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.                                                           |
| 37    | VDDA                   | PWR  | 3.3V power for the PLL core.                                                                                                                                                                                                          |
| 38    | GNDA                   | PWR  | Ground pin for the PLL core.                                                                                                                                                                                                          |
| 39    | IREF                   | OUT  | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 40    | CPUCLKC1               | OUT  | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                               |
| 41    | CPUCLKT1               | OUT  | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                        |
| 42    | VDDCPU                 | PWR  | Supply for CPU clocks, 3.3V nominal                                                                                                                                                                                                   |
| 43    | CPUCLKC0               | OUT  | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                               |
| 44    | CPUCLKT0               | OUT  | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.                                                                                                        |
| 45    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 46    | SCLK                   | IN   | Clock pin of SMBus circuitry, 5V tolerant.                                                                                                                                                                                            |
| 47    | SDATA                  | I/O  | Data pin for SMBus circuitry, 5V tolerant.                                                                                                                                                                                            |
| 48    | VDDREF                 | PWR  | Ref, XTAL power supply, nominal 3.3V                                                                                                                                                                                                  |
| 49    | X2                     | OUT  | Crystal output, Nominally 14.318MHz                                                                                                                                                                                                   |
| 50    | X1                     | IN   | Crystal input, Nominally 14.318MHz.                                                                                                                                                                                                   |
| 51    | GND                    | PWR  | Ground pin.                                                                                                                                                                                                                           |
| 52    | REFOUT                 | OUT  | Reference Clock output                                                                                                                                                                                                                |
| 53    | FSLC                   | IN   | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values.                                                                                                  |
| 54    | PCICLK0                | OUT  | PCI clock output.                                                                                                                                                                                                                     |
| 55    | PCICLK1                | OUT  | PCI clock output.                                                                                                                                                                                                                     |
| 56    | PCICLK2                | OUT  | PCI clock output.                                                                                                                                                                                                                     |

## General Description

**ICS954141A** follows Intel CK410 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954141A** is driven with a 14.318MHz crystal.

## Block Diagram



## General I<sup>2</sup>C serial interface information for the ICS954141A

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation     |           |                      |     |
|---------------------------------|-----------|----------------------|-----|
| Controller (Host)               |           | ICS (Slave/Receiver) |     |
| T                               | starT bit |                      |     |
| Slave Address D2 <sub>(H)</sub> |           |                      |     |
| WR                              | WRite     |                      |     |
|                                 |           | ACK                  |     |
| Beginning Byte = N              |           |                      |     |
|                                 |           | ACK                  |     |
| Data Byte Count = X             |           |                      |     |
|                                 |           | ACK                  |     |
| Beginning Byte N                |           | X Byte               |     |
|                                 |           |                      | ACK |
| ○                               |           |                      |     |
| ○                               |           |                      | ○   |
| ○                               |           |                      | ○   |
|                                 |           |                      | ○   |
| Byte N + X - 1                  |           |                      |     |
|                                 |           | ACK                  |     |
| P                               | stoP bit  |                      |     |

| Index Block Read Operation      |                 |                      |                  |
|---------------------------------|-----------------|----------------------|------------------|
| Controller (Host)               |                 | ICS (Slave/Receiver) |                  |
| T                               | starT bit       |                      |                  |
| Slave Address D2 <sub>(H)</sub> |                 |                      |                  |
| WR                              | WRite           |                      |                  |
|                                 |                 | ACK                  |                  |
| Beginning Byte = N              |                 |                      |                  |
|                                 |                 | ACK                  |                  |
| RT                              | Repeat starT    |                      |                  |
| Slave Address D3 <sub>(H)</sub> |                 |                      |                  |
| RD                              | ReaD            |                      |                  |
|                                 |                 | ACK                  |                  |
|                                 |                 |                      |                  |
|                                 |                 | Data Byte Count = X  |                  |
| ACK                             |                 |                      |                  |
|                                 |                 | X Byte               |                  |
| ACK                             |                 |                      | Beginning Byte N |
|                                 |                 |                      |                  |
| ○                               |                 |                      | ○                |
| ○                               |                 |                      | ○                |
| ○                               |                 |                      | ○                |
| ○                               |                 |                      |                  |
|                                 |                 | Byte N + X - 1       |                  |
| N                               | Not acknowledge |                      |                  |
| P                               | stoP bit        |                      |                  |

**Table1: Frequency Selection Table**

| Bit4 | Bit3 | Bit2<br>FSLC | Bit1<br>FSLB | Bit0<br>FSLA | CPU<br>MHz | SRC<br>MHz | SATA<br>MHz | PCI<br>MHz | Spread<br>%     |
|------|------|--------------|--------------|--------------|------------|------------|-------------|------------|-----------------|
| 0    | 0    | 0            | 0            | 0            | 266.66     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 0            | 0            | 1            | 133.33     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 0            | 1            | 0            | 200.00     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 0            | 1            | 1            | 166.66     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 1            | 0            | 0            | 333.33     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 1            | 0            | 1            | 100.00     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 1            | 1            | 0            | 400.00     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 0    | 1            | 1            | 1            | 200.00     | 100.00     | 100.00      | 33.33      | 0 to -0.5% Down |
| 0    | 1    | 0            | 0            | 0            | 266.66     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 0    | 1    | 0            | 0            | 1            | 133.33     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 0    | 1    | 0            | 1            | 0            | 200.00     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 0    | 1    | 0            | 1            | 1            | 166.66     | 125.00     | 125.00      | 33.33      | +/-0.25% Center |
| 0    | 1    | 1            | 0            | 0            | 333.33     | 125.00     | 125.00      | 33.33      | +/-0.25% Center |
| 0    | 1    | 1            | 0            | 1            | 100.00     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 0    | 1    | 1            | 1            | 0            | 400.00     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 0    | 1    | 1            | 1            | 1            | 200.00     | 133.33     | 133.33      | 33.33      | +/-0.25% Center |
| 1    | 0    | 0            | 0            | 0            | 269.33     | 101.00     | 101.00      | 33.67      | +/-0.3% Center  |
| 1    | 0    | 0            | 0            | 1            | 134.66     | 101.00     | 101.00      | 33.67      | +/-0.3% Center  |
| 1    | 0    | 0            | 1            | 0            | 202.00     | 101.00     | 101.00      | 33.67      | +/-0.3% Center  |
| 1    | 0    | 0            | 1            | 1            | 168.33     | 101.00     | 101.00      | 33.67      | +/-0.3% Center  |
| 1    | 0    | 1            | 0            | 0            | 274.66     | 103.00     | 103.00      | 34.33      | +/-0.3% Center  |
| 1    | 0    | 1            | 0            | 1            | 137.33     | 103.00     | 103.00      | 34.33      | +/-0.3% Center  |
| 1    | 0    | 1            | 1            | 0            | 206.00     | 103.00     | 103.00      | 34.33      | +/-0.3% Center  |
| 1    | 0    | 1            | 1            | 1            | 171.66     | 103.00     | 103.00      | 34.33      | +/-0.3% Center  |
| 1    | 1    | 0            | 0            | 0            | 279.99     | 105.00     | 105.00      | 35.00      | +/-0.3% Center  |
| 1    | 1    | 0            | 0            | 1            | 140.00     | 105.00     | 105.00      | 35.00      | +/-0.3% Center  |
| 1    | 1    | 0            | 1            | 0            | 210.00     | 105.00     | 105.00      | 35.00      | +/-0.3% Center  |
| 1    | 1    | 0            | 1            | 1            | 174.99     | 105.00     | 105.00      | 35.00      | +/-0.3% Center  |
| 1    | 1    | 1            | 0            | 0            | 287.99     | 108.00     | 108.00      | 36.00      | +/-0.3% Center  |
| 1    | 1    | 1            | 0            | 1            | 144.00     | 108.00     | 108.00      | 36.00      | +/-0.3% Center  |
| 1    | 1    | 1            | 1            | 0            | 216.00     | 108.00     | 108.00      | 36.00      | +/-0.3% Center  |
| 1    | 1    | 1            | 1            | 1            | 179.99     | 108.00     | 108.00      | 36.00      | +/-0.3% Center  |

I<sup>2</sup>C Table: Frequency Select Register

| Byte 0 | Pin # | Name      | Control Function         | Type | 0                                            | 1   | PWD   |
|--------|-------|-----------|--------------------------|------|----------------------------------------------|-----|-------|
| Bit 7  | -     | FS Source | Frequency H/W IIC Select | RW   | Latch Inputs                                 | IIC | 0     |
| Bit 6  | -     | SS_EN1    | PLL1 Spread Enable       | RW   | OFF                                          | ON  | 1     |
| Bit 5  | -     | SS_EN2    | PLL2 Spread Enable       | RW   | OFF                                          | ON  | 1     |
| Bit 4  | -     | Bit4      | Freq Select Bit 4        | RW   | See Table 1: PLL 1 Frequency Selection Table |     | 0     |
| Bit 3  | -     | Bit3      | Freq Select Bit 3        | RW   |                                              |     | 0     |
| Bit 2  | -     | FSLC      | Freq Select Bit 2        | RW   |                                              |     | Latch |
| Bit 1  | -     | FSLB      | Freq Select Bit 1        | RW   |                                              |     | Latch |
| Bit 0  | -     | FSLA      | Freq Select Bit 0        | RW   |                                              |     | Latch |

I<sup>2</sup>C Table: Output Control Register

| Byte 1 | Pin # | Name         | Control Function             | Type | 0       | 1      | PWD |
|--------|-------|--------------|------------------------------|------|---------|--------|-----|
| Bit 7  | -     | PCICLK_F0    | Output Control               | RW   | Disable | Enable | 1   |
| Bit 6  | -     | DOTT/C_96MHz | Output Control               | RW   | Disable | Enable | 1   |
| Bit 5  | -     | USB_48MHz    | Output Control               | RW   | Disable | Enable | 1   |
| Bit 4  | -     | REFOUT       | Output Control               | RW   | Disable | Enable | 1   |
| Bit 3  | -     | Reserved     | Reserved                     | RW   | -       | -      | 1   |
| Bit 2  | -     | CPUCLKT/C1   | Output Control               | RW   | Disable | Enable | 1   |
| Bit 1  | -     | CPUCLKT/C0   | Output Control               | RW   | Disable | Enable | 1   |
| Bit 0  | -     | CPUCLK's     | PD Mode Output State Control | RW   | Driven  | Hi-Z   | 0   |

I<sup>2</sup>C Table: Output Control Register

| Byte 2 | Pin # | Name      | Control Function | Type | 0       | 1      | PWD |
|--------|-------|-----------|------------------|------|---------|--------|-----|
| Bit 7  | -     | PCICLK5   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 6  | -     | PCICLK4   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 5  | -     | PCICLK3   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 4  | -     | PCICLK2   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 3  | -     | PCICLK1   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 2  | -     | PCICLK0   | Output Control   | RW   | Disable | Enable | 1   |
| Bit 1  | -     | PCICLK_F2 | Output Control   | RW   | Disable | Enable | 1   |
| Bit 0  | -     | PCICLK_F1 | Output Control   | RW   | Disable | Enable | 1   |

I<sup>2</sup>C Table: Output Control Register

| Byte 3 | Pin # | Name                 | Control Function             | Type | 0       | 1      | PWD |
|--------|-------|----------------------|------------------------------|------|---------|--------|-----|
| Bit 7  | -     | SRCCLK's             | PD Mode Output State Control | RW   | Driven  | Hi-Z   | 0   |
| Bit 6  | -     | CPUCLKT/C2 / SRCCLK7 | Output Control               | RW   | Disable | Enable | 1   |
| Bit 5  | -     | SRCCLKT/C6           | Output Control               | RW   | Disable | Enable | 1   |
| Bit 4  | -     | SRCCLKT/C5           | Output Control               | RW   | Disable | Enable | 1   |
| Bit 3  | -     | SRCCLKT/C_SATA4      | Output Control               | RW   | Disable | Enable | 1   |
| Bit 2  | -     | SRCCLKT/C3           | Output Control               | RW   | Disable | Enable | 1   |
| Bit 1  | -     | SRCCLKT/C2           | Output Control               | RW   | Disable | Enable | 1   |
| Bit 0  | -     | SRCCLKT/C1           | Output Control               | RW   | Disable | Enable | 1   |

I<sup>2</sup>C Table: Output Control Register

| Byte 4 | Pin # | Name            | Control Function          | Type | 0            | 1         | PWD |
|--------|-------|-----------------|---------------------------|------|--------------|-----------|-----|
| Bit 7  | -     | PCI/SRC Stop EN | Stop all PCI / SRC clocks |      | Enable       | Disable   | 1   |
| Bit 6  | -     | PCICLK_F2       | Stop Control              | RW   | Free Running | Stoppable | 0   |
| Bit 5  | -     | PCICLK_F1       | Stop Control              | RW   | Free Running | Stoppable | 0   |
| Bit 4  | -     | PCICLK_F0       | Stop Control              | RW   | Free Running | Stoppable | 0   |
| Bit 3  | -     | SRCLKT/C (7:5)  | Stop Control              | RW   | Free Running | Stoppable | 1   |
| Bit 2  | -     | SRCLKT/C 4      | Stop Control              | RW   | Free Running | Stoppable | 1   |
| Bit 1  | -     | SRCLKT/C (3:1)  | Stop Control              | RW   | Free Running | Stoppable | 1   |
| Bit 0  | -     | Reserved        | Reserved                  | RW   | -            | -         | 1   |

I<sup>2</sup>C Table: Programmable Skew Control Register

| Byte 5 |   | Pin # | Name     | Control Function                                     | Type | 0               |          | 1         |          | PWD |
|--------|---|-------|----------|------------------------------------------------------|------|-----------------|----------|-----------|----------|-----|
| Bit 7  | - |       | PCISkw3  | CPU-PCI 7 Steps Skew Control (ps) (Also see Table 3) | RW   | 0000:0          | 0100:150 | 1000:300  | 1100:450 | 0   |
| Bit 6  | - |       | PCISkw2  |                                                      | RW   | 0001:N/A        | 0101:N/A | 1001:N/A  | 1101:600 | 0   |
| Bit 5  | - |       | PCISkw1  |                                                      | RW   | 0010:N/A        | 0110:N/A | 1010:N/A  | 1110:750 | 0   |
| Bit 4  | - |       | PCISkw0  |                                                      | RW   | 0011:N/A        | 0111:N/A | 1011:N/A  | 1111:900 | 0   |
| Bit 3  | - |       | ASYNC1   | PCI Async Freq (see Table 6)                         | RW   | 00 = PLL1/ PLL2 |          | 10 = 37.7 |          | 0   |
| Bit 2  | - |       | ASYNC0   |                                                      | RW   | 01 = 33.0       |          | 11 = 44.0 |          | 0   |
| Bit 1  | - |       | Reserved | Reserved                                             | RW   | -               |          | -         |          | 0   |
| Bit 0  | - |       | Reserved | Reserved                                             | RW   | -               |          | -         |          | 0   |

I<sup>2</sup>C Table: Output Drive Control Register

| Byte 6 | Pin # | Name     | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------|------------------|------|---|---|-----|
| Bit 7  | -     | Reserved | Reserved         | RW   | - | - | 1   |
| Bit 6  | -     | Reserved |                  | RW   | - | - | 1   |
| Bit 5  | -     | Reserved | Reserved         | RW   | - | - | 1   |
| Bit 4  | -     | Reserved |                  | RW   | - | - | 1   |
| Bit 3  | -     | Reserved | Reserved         | RW   | - | - | 1   |
| Bit 2  | -     | Reserved |                  | RW   | - | - | 1   |
| Bit 1  | -     | Reserved | Reserved         | RW   | - | - | 1   |
| Bit 0  | -     | Reserved |                  | RW   | - | - | 1   |

I<sup>2</sup>C Table: Vendor ID Register

| Byte 7 | Pin # | Name            | Control Function                      | Type | 0         | 1    | PWD |
|--------|-------|-----------------|---------------------------------------|------|-----------|------|-----|
| Bit 7  | -     | SRC_SOURCE      | SRC comes from                        | RW   | PLL1      | PLL2 | 0   |
| Bit 6  | -     | PCI_SOURCE      | PCI comes from                        | RW   | PLL1      | PLL2 | 0   |
| Bit 5  | -     | SRC_SATA_Source | SATA comes from                       | RW   | PLL1      | PLL2 | 0   |
| Bit 4  | -     | PLL2 Sync       | PLL2 (SATA, SRC,PCI ) Synchronization | RW   | Async     | Sync | 0   |
| Bit 3  | -     | VID3            | VENDOR ID                             | R    | -         | -    | 0   |
| Bit 2  | -     | VID2            |                                       | R    | -         | -    | 0   |
| Bit 1  | -     | VID1            |                                       | R    | 001 = ICS | -    | 0   |
| Bit 0  | -     | VID0            |                                       | R    | -         | -    | 1   |

I<sup>2</sup>C Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function                 | Type | 0                                                                                                   | 1 | PWD |
|--------|-------|------|----------------------------------|------|-----------------------------------------------------------------------------------------------------|---|-----|
| Bit 7  | -     | BC7  | Byte Count Programming<br>b(7:0) | RW   | Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes. |   | 0   |
| Bit 6  | -     | BC6  |                                  | RW   |                                                                                                     |   | 0   |
| Bit 5  | -     | BC5  |                                  | RW   |                                                                                                     |   | 0   |
| Bit 4  | -     | BC4  |                                  | RW   |                                                                                                     |   | 0   |
| Bit 3  | -     | BC3  |                                  | RW   |                                                                                                     |   | 1   |
| Bit 2  | -     | BC2  |                                  | RW   |                                                                                                     |   | 1   |
| Bit 1  | -     | BC1  |                                  | RW   |                                                                                                     |   | 1   |
| Bit 0  | -     | BC0  |                                  | RW   |                                                                                                     |   | 1   |

I<sup>2</sup>C Table: WD Time Control Register

| Byte 9 | Pin # | Name           | Control Function            | Type | 0                                                                                                                         | 1           | PWD |
|--------|-------|----------------|-----------------------------|------|---------------------------------------------------------------------------------------------------------------------------|-------------|-----|
| Bit 7  | -     | WDH_EN         | Watchdog Hard Alarm Enable  | RW   | Disable                                                                                                                   | Enable      | 0   |
| Bit 6  | -     | WDS_EN         | Watchdog Soft Alarm Enable  | RW   | Disable                                                                                                                   | Enable      | 0   |
| Bit 5  | -     | WD Hard Status | WD Hard Alarm Status        | R    | Normal                                                                                                                    | Alarm       | X   |
| Bit 4  | -     | WD Soft Status | WD Soft Alarm Status        | R    | Normal                                                                                                                    | Alarm       | X   |
| Bit 3  | -     | WDTCtrl        | Watch Dog Time base Control | RW   | 290ms Base                                                                                                                | 1160ms Base | 0   |
| Bit 2  | -     | WD2            | WD Timer Bit 2              | RW   | These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s. |             | 1   |
| Bit 1  | -     | WD1            | WD Timer Bit 1              | RW   |                                                                                                                           |             | 1   |
| Bit 0  | -     | WD0            | WD Timer Bit 0              | RW   |                                                                                                                           |             | 1   |

I<sup>2</sup>C Table: M/N Programming & WD Safe Frequency Control Register

| Byte 10 | Pin # | Name                | Control Function                     | Type | 0                                                                          | 1                    | PWD |
|---------|-------|---------------------|--------------------------------------|------|----------------------------------------------------------------------------|----------------------|-----|
| Bit 7   | -     | M/N_EN              | PLL1 M/N Programming Enable          | RW   | Disable                                                                    | Enable               | 0   |
| Bit 6   | -     | Reserved            | Reserved                             | RW   | -                                                                          | -                    | 0   |
| Bit 5   | -     | WD Safe Freq Source | WD Safe Freq Source                  | RW   | B10b(4:0)                                                                  | Latch Inputs/B0(4:0) | 0   |
| Bit 4   | -     | WD SF4              | Watch Dog Safe Freq Programming bits | RW   | Writing to these bit will configure the safe frequency as Byte0 bit (4:0). |                      | 0   |
| Bit 3   | -     | WD SF3              |                                      | RW   |                                                                            |                      | 0   |
| Bit 2   | -     | WD SF2              |                                      | RW   |                                                                            |                      | 0   |
| Bit 1   | -     | WD SF1              |                                      | RW   |                                                                            |                      | 0   |
| Bit 0   | -     | WD SF0              |                                      | RW   |                                                                            |                      | 0   |

I<sup>2</sup>C Table: PLL1 Frequency Control Register

| Byte 11 | Pin # | Name   | Control Function                | Type | 0                                                                                                                                                                                                                 | 1 | PWD |
|---------|-------|--------|---------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | N Div8 | N Divider Prog bit 8            | RW   | The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] |   | X   |
| Bit 6   | -     | N Div9 | N Divider Prog bit 9            | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 5   | -     | M Div5 | M Divider Programming bit (5:0) | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 4   | -     | M Div4 |                                 | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 3   | -     | M Div3 |                                 | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 2   | -     | M Div2 |                                 | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 1   | -     | M Div1 |                                 | RW   |                                                                                                                                                                                                                   |   | X   |
| Bit 0   | -     | M Div0 |                                 | RW   |                                                                                                                                                                                                                   |   | X   |

I<sup>2</sup>C Table: PLL1 Frequency Control Register

| Byte 12 | Pin # | Name   | Control Function                                                | Type | 0                                                                                                                                                                                                                             | 1 | PWD |
|---------|-------|--------|-----------------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | N Div7 | N Divider Programming<br>Byte12 bit(7:0) and Byte11<br>bit(7:6) | RW   | The decimal representation of M and N Divider in<br>Byte 11 and 12 will configure the PLL1 VCO<br>frequency. Default at power up = latch-in or Byte 0<br>Rom table. VCO Frequency = 14.318 x<br>[NDiv(9:0)+8] / [MDiv(5:0)+2] |   | X   |
| Bit 6   | -     | N Div6 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 5   | -     | N Div5 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 4   | -     | N Div4 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 3   | -     | N Div3 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 2   | -     | N Div2 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 1   | -     | N Div1 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 0   | -     | N Div0 |                                                                 | RW   |                                                                                                                                                                                                                               |   | X   |

I<sup>2</sup>C Table: PLL1 Spread Spectrum Control Register

| Byte 13 | Pin # | Name | Control Function                        | Type | 0                                                                                          | 1 | PWD |
|---------|-------|------|-----------------------------------------|------|--------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | SSP7 | Spread Spectrum<br>Programming bit(7:0) | RW   | These Spread Spectrum bits in Byte 13 and 14 will<br>program the spread percentage of PLL1 |   | X   |
| Bit 6   | -     | SSP6 |                                         | RW   |                                                                                            |   | X   |
| Bit 5   | -     | SSP5 |                                         | RW   |                                                                                            |   | X   |
| Bit 4   | -     | SSP4 |                                         | RW   |                                                                                            |   | X   |
| Bit 3   | -     | SSP3 |                                         | RW   |                                                                                            |   | X   |
| Bit 2   | -     | SSP2 |                                         | RW   |                                                                                            |   | X   |
| Bit 1   | -     | SSP1 |                                         | RW   |                                                                                            |   | X   |
| Bit 0   | -     | SSP0 |                                         | RW   |                                                                                            |   | X   |

I<sup>2</sup>C Table: PLL1 Spread Spectrum Control Register

| Byte 14 | Pin # | Name     | Control Function                         | Type | 0                                                                                          | 1 | PWD |
|---------|-------|----------|------------------------------------------|------|--------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | Reserved | Reserved                                 | R    | -                                                                                          | - | 0   |
| Bit 6   | -     | SSP14    | Spread Spectrum<br>Programming bit(14:8) | RW   | These Spread Spectrum bits in Byte 13 and 14 will<br>program the spread percentage of PLL1 |   | X   |
| Bit 5   | -     | SSP13    |                                          | RW   |                                                                                            |   | X   |
| Bit 4   | -     | SSP12    |                                          | RW   |                                                                                            |   | X   |
| Bit 3   | -     | SSP11    |                                          | RW   |                                                                                            |   | X   |
| Bit 2   | -     | SSP10    |                                          | RW   |                                                                                            |   | X   |
| Bit 1   | -     | SSP9     |                                          | RW   |                                                                                            |   | X   |
| Bit 0   | -     | SSP8     |                                          | RW   |                                                                                            |   | X   |

I<sup>2</sup>C Table: PLL2 Frequency Control Register

| Byte 15 | Pin # | Name   | Control Function              | Type | 0                                                                                                                                                                                                                             | 1 | PWD |
|---------|-------|--------|-------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | N Div8 | N Divider Prog bit 8          | RW   | The decimal representation of M and N Divider in<br>Byte 15 and 16 will configure the PLL2 VCO<br>frequency. Default at power up = latch-in or Byte 0<br>Rom table. VCO Frequency = 14.318 x<br>[NDiv(9:0)+8] / [MDiv(5:0)+2] |   | X   |
| Bit 6   | -     | N Div9 | N Divider Prog bit 9          | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 5   | -     | M Div5 | M Divider Programming<br>bits | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 4   | -     | M Div4 |                               | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 3   | -     | M Div3 |                               | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 2   | -     | M Div2 |                               | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 1   | -     | M Div1 |                               | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 0   | -     | M Div0 |                               | RW   |                                                                                                                                                                                                                               |   | X   |

I<sup>2</sup>C Table: PLL2 Frequency Control Register

| Byte 16 | Pin # | Name   | Control Function                | Type | 0                                                                                                                                                                                                                             | 1 | PWD |
|---------|-------|--------|---------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | N Div7 | N Divider Programming<br>b(7:0) | RW   | The decimal representation of M and N Divider in<br>Byte 15 and 16 will configure the PLL2 VCO<br>frequency. Default at power up = latch-in or Byte 0<br>Rom table. VCO Frequency = 14.318 x<br>[NDiv(9:0)+8] / [MDiv(5:0)+2] |   | X   |
| Bit 6   | -     | N Div6 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 5   | -     | N Div5 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 4   | -     | N Div4 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 3   | -     | N Div3 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 2   | -     | N Div2 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 1   | -     | N Div1 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |
| Bit 0   | -     | N Div0 |                                 | RW   |                                                                                                                                                                                                                               |   | X   |

I<sup>2</sup>C Table: PLL2 Spread Spectrum Control Register

| Byte 17 | Pin # | Name | Control Function                      | Type | 0                                                                                          | 1 | PWD |
|---------|-------|------|---------------------------------------|------|--------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | SSP7 | Spread Spectrum<br>Programming b(7:0) | RW   | These Spread Spectrum bits in Byte 17 and 18 will<br>program the spread percentage of PLL2 |   | X   |
| Bit 6   | -     | SSP6 |                                       | RW   |                                                                                            |   | X   |
| Bit 5   | -     | SSP5 |                                       | RW   |                                                                                            |   | X   |
| Bit 4   | -     | SSP4 |                                       | RW   |                                                                                            |   | X   |
| Bit 3   | -     | SSP3 |                                       | RW   |                                                                                            |   | X   |
| Bit 2   | -     | SSP2 |                                       | RW   |                                                                                            |   | X   |
| Bit 1   | -     | SSP1 |                                       | RW   |                                                                                            |   | X   |
| Bit 0   | -     | SSP0 |                                       | RW   |                                                                                            |   | X   |

I<sup>2</sup>C Table: PLL2 Spread Spectrum Control Register

| Byte 18 | Pin # | Name     | Control Function                       | Type | 0                                                                                          | 1 | PWD |
|---------|-------|----------|----------------------------------------|------|--------------------------------------------------------------------------------------------|---|-----|
| Bit 7   | -     | Reserved | Reserved                               | R    | -                                                                                          | - | 0   |
| Bit 6   | -     | SSP14    | Spread Spectrum<br>Programming b(14:8) | RW   | These Spread Spectrum bits in Byte 17 and 18 will<br>program the spread percentage of PLL2 |   | X   |
| Bit 5   | -     | SSP13    |                                        | RW   |                                                                                            |   | X   |
| Bit 4   | -     | SSP12    |                                        | RW   |                                                                                            |   | X   |
| Bit 3   | -     | SSP11    |                                        | RW   |                                                                                            |   | X   |
| Bit 2   | -     | SSP10    |                                        | RW   |                                                                                            |   | X   |
| Bit 1   | -     | SSP9     |                                        | RW   |                                                                                            |   | X   |
| Bit 0   | -     | SSP8     |                                        | RW   |                                                                                            |   | X   |

I<sup>2</sup>C Table: Programmable Output Divider Register

| Byte 19 |   | Pin # | Name    | Control Function                               | Type | 0       |          | 1        |          | PWD |
|---------|---|-------|---------|------------------------------------------------|------|---------|----------|----------|----------|-----|
| Bit 7   | - |       | CPUDiv3 | CPU Divider Ratio<br>Programming Bits for PLL1 | RW   | 0000:/2 | 0100:/4  | 1000:/8  | 1100:/16 | X   |
| Bit 6   | - |       | CPUDiv2 |                                                | RW   | 0001:/3 | 0101:/6  | 1001:/12 | 1101:/24 | X   |
| Bit 5   | - |       | CPUDiv1 |                                                | RW   | 0010:/5 | 0110:/10 | 1010:/20 | 1110:/40 | X   |
| Bit 4   | - |       | CPUDiv0 |                                                | RW   | 0011:/7 | 0111:/14 | 1011:/28 | 1111:/56 | X   |
| Bit 3   | - |       | SRCDiv3 | SRC Divider Ratio<br>Programming Bits for PLL1 | RW   | 0000:/2 | 0100:/4  | 1000:/8  | 1100:/16 | X   |
| Bit 2   | - |       | SRCDiv2 |                                                | RW   | 0001:/3 | 0101:/6  | 1001:/12 | 1101:/24 | X   |
| Bit 1   | - |       | SRCDiv1 |                                                | RW   | 0010:/5 | 0110:/10 | 1010:/20 | 1110:/40 | X   |
| Bit 0   | - |       | SRCDiv0 |                                                | RW   | 0011:/7 | 0111:/14 | 1011:/28 | 1111:/56 | X   |

## Absolute Maximum Rating

| PARAMETER                       | SYMBOL   | CONDITIONS | MIN       | TYP | MAX                    | UNITS | Notes |
|---------------------------------|----------|------------|-----------|-----|------------------------|-------|-------|
| 3.3V Core Supply Voltage        | VDD_A    | -          |           |     | V <sub>DD</sub> + 0.5V | V     | 1     |
| 3.3V Logic Input Supply Voltage | VDD_In   | -          | GND - 0.5 |     | V <sub>DD</sub> + 0.5V | V     | 1     |
| Storage Temperature             | Ts       | -          | -65       |     | 150                    | °C    | 1     |
| Ambient Operating Temp          | Tambient | -          | 0         |     | 70                     | °C    | 1     |
| Case Temperature                | Tcase    | -          |           |     | 115                    | °C    | 1     |
| Input ESD protection HBM        | ESD prot | -          | 2000      |     |                        | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER                                  | SYMBOL               | CONDITIONS*                                                       | MIN                   | TYP      | MAX                   | UNITS | Notes |
|--------------------------------------------|----------------------|-------------------------------------------------------------------|-----------------------|----------|-----------------------|-------|-------|
| Input High Voltage                         | V <sub>IH</sub>      | 3.3 V +/-5%                                                       | 2                     |          | V <sub>DD</sub> + 0.3 | V     | 1     |
| Input Low Voltage                          | V <sub>IL</sub>      | 3.3 V +/-5%                                                       | V <sub>SS</sub> - 0.3 |          | 0.8                   | V     | 1     |
| Input High Current                         | I <sub>IH</sub>      | V <sub>IN</sub> = V <sub>DD</sub>                                 | -5                    |          | 5                     | uA    | 1     |
| Input Low Current                          | I <sub>IL1</sub>     | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors           | -5                    |          |                       | uA    | 1     |
|                                            | I <sub>IL2</sub>     | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors              | -200                  |          |                       | uA    | 1     |
| Low Threshold Input-High Voltage           | V <sub>IH_FSL</sub>  | 3.3 V +/-5%                                                       | 0.7                   |          | V <sub>DD</sub> + 0.3 | V     | 1     |
| Low Threshold Input-Low Voltage            | V <sub>IL_FSL</sub>  | 3.3 V +/-5%                                                       | V <sub>SS</sub> - 0.3 |          | 0.35                  | V     | 1     |
| Operating Supply Current                   | I <sub>DD3.3OP</sub> | Full Active, C <sub>L</sub> = Full load;                          |                       |          | 350                   | mA    | 1     |
| Operating Current                          | I <sub>DD3.3OP</sub> | all outputs driven                                                |                       |          | 400                   | mA    | 1     |
| Powerdown Current                          | I <sub>DD3.3PD</sub> | all diff pairs driven                                             |                       |          | 70                    | mA    | 1     |
|                                            |                      | all differential pairs tri-stated                                 |                       |          | 12                    | mA    | 1     |
| Input Frequency                            | F <sub>i</sub>       | V <sub>DD</sub> = 3.3 V                                           |                       | 14.31818 |                       | MHz   | 2     |
| Pin Inductance                             | L <sub>pin</sub>     |                                                                   |                       |          | 7                     | nH    | 1     |
| Input Capacitance                          | C <sub>IN</sub>      | Logic Inputs                                                      |                       |          | 5                     | pF    | 1     |
|                                            | C <sub>OUT</sub>     | Output pin capacitance                                            |                       |          | 6                     | pF    | 1     |
|                                            | C <sub>INX</sub>     | X1 & X2 pins                                                      |                       |          | 5                     | pF    | 1     |
| Clk Stabilization                          | T <sub>STAB</sub>    | From V <sub>DD</sub> Power-Up or de-assertion of PD# to 1st clock |                       |          | 1.8                   | ms    | 1     |
| Modulation Frequency                       |                      | Triangular Modulation                                             | 30                    |          | 33                    | kHz   | 1     |
| Tdrive_PD#                                 |                      | CPU output enable after PD# de-assertion                          |                       |          | 300                   | us    | 1     |
| Tfall_Pd#                                  |                      | PD# fall time of                                                  |                       |          | 5                     | ns    | 1     |
| Trise_Pd#                                  |                      | PD# rise time of                                                  |                       |          | 5                     | ns    | 1     |
| SMBus Voltage                              | V <sub>DD</sub>      |                                                                   | 2.7                   |          | 5.5                   | V     | 1     |
| Low-level Output Voltage                   | V <sub>OL</sub>      | @ I <sub>PULLUP</sub>                                             |                       |          | 0.4                   | V     | 1     |
| Current sinking at V <sub>OL</sub> = 0.4 V | I <sub>PULLUP</sub>  |                                                                   | 4                     |          |                       | mA    | 1     |
| SCLK/SDATA Clock/Data Rise Time            | T <sub>RI2C</sub>    | (Max VIL - 0.15) to (Min VIH + 0.15)                              |                       |          | 1000                  | ns    | 1     |
| SCLK/SDATA Clock/Data Fall Time            | T <sub>FI2C</sub>    | (Min VIH + 0.15) to (Max VIL - 0.15)                              |                       |          | 300                   | ns    | 1     |

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

## Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

| PARAMETER                       | SYMBOL               | CONDITIONS*                                              | MIN    | TYP | MAX     | UNITS | NOTES |
|---------------------------------|----------------------|----------------------------------------------------------|--------|-----|---------|-------|-------|
| Current Source Output Impedance | Z <sub>o</sub>       | V <sub>O</sub> = V <sub>x</sub>                          | 3000   |     |         | Ω     | 1     |
| Voltage High                    | V <sub>High</sub>    | Statistical measurement on single ended signal           | 660    |     | 850     | mV    | 1,3   |
| Voltage Low                     | V <sub>Low</sub>     |                                                          | -150   |     | 150     | mV    | 1,3   |
| Max Voltage                     | V <sub>ovs</sub>     | Measurement on single ended signal using absolute value. |        |     | 1150    | mV    | 1     |
| Min Voltage                     | V <sub>uds</sub>     |                                                          | -300   |     |         | mV    | 1     |
| Crossing Voltage (abs)          | V <sub>x(abs)</sub>  |                                                          | 250    |     | 550     | mV    | 1     |
| Crossing Voltage (var)          | d-V <sub>x</sub>     | Variation of crossing over all edges                     |        |     | 140     | mV    | 1     |
| Long Accuracy                   | ppm                  | see Tperiod min-max values                               | -300   |     | 300     | ppm   | 1,2   |
| Average period                  | Tperiod              | 400MHz nominal                                           | 2.4993 |     | 2.5008  | ns    | 2     |
|                                 |                      | 400MHz spread                                            | 2.4993 |     | 2.5133  | ns    | 2     |
|                                 |                      | 333.33MHz nominal                                        | 2.9991 |     | 3.0009  | ns    | 2     |
|                                 |                      | 333.33MHz spread                                         | 2.9991 |     | 3.016   | ns    | 2     |
|                                 |                      | 266.66MHz nominal                                        | 3.7489 |     | 3.7511  | ns    | 2     |
|                                 |                      | 266.66MHz spread                                         | 3.7489 |     | 3.77    | ns    | 2     |
|                                 |                      | 200MHz nominal                                           | 4.9985 |     | 5.0015  | ns    | 2     |
|                                 |                      | 200MHz spread                                            | 4.9985 |     | 5.0266  | ns    | 2     |
|                                 |                      | 166.66MHz nominal                                        | 5.9982 |     | 6.0018  | ns    | 2     |
|                                 |                      | 166.66MHz spread                                         | 5.9982 |     | 6.0320  | ns    | 2     |
|                                 |                      | 133.33MHz nominal                                        | 7.4978 |     | 7.5023  | ns    | 2     |
|                                 |                      | 133.33MHz spread                                         | 7.4978 |     | 7.5400  | ns    | 2     |
|                                 |                      | 100.00MHz nominal                                        | 9.9970 |     | 10.0030 | ns    | 2     |
|                                 |                      | 100.00MHz spread                                         | 9.9970 |     | 10.0533 | ns    | 2     |
| Absolute min period             | T <sub>absmin</sub>  | 400MHz nominal/spread                                    | 2.4143 |     |         | ns    | 1,2   |
|                                 |                      | 333.33MHz nominal/spread                                 | 2.9141 |     |         | ns    | 1,2   |
|                                 |                      | 266.66MHz nominal/spread                                 | 3.6639 |     |         | ns    | 1,2   |
|                                 |                      | 200MHz nominal/spread                                    | 4.8735 |     |         | ns    | 1,2   |
|                                 |                      | 166.66MHz nominal/spread                                 | 5.8732 |     |         | ns    | 1,2   |
|                                 |                      | 133.33MHz nominal/spread                                 | 7.3728 |     |         | ns    | 1,2   |
|                                 |                      | 100.00MHz nominal/spread                                 | 9.8720 |     |         | ns    | 1,2   |
| Rise Time                       | t <sub>r</sub>       | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       | 175    |     | 700     | ps    | 1     |
| Fall Time                       | t <sub>f</sub>       | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        | 175    |     | 700     | ps    | 1     |
| Rise Time Variation             | d-t <sub>r</sub>     | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       |        |     | 125     | ps    | 1     |
| Fall Time Variation             | d-t <sub>f</sub>     | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        |        |     | 125     | ps    | 1     |
| Duty Cycle                      | d <sub>l3</sub>      | Measurement from differential waveform                   | 45     |     | 55      | %     | 1     |
| Skew                            | t <sub>sk3</sub>     | CPU(1:0), V <sub>T</sub> = 50%                           |        |     | 100     | ps    | 1     |
| Skew                            | t <sub>sk4</sub>     | CPU(1:0) to CPU2_ITP, V <sub>T</sub> = 50%               |        |     | 150     | ps    | 1     |
| Jitter, Cycle to cycle          | t <sub>jcy-cyc</sub> | Measurement from differential waveform (CPU2_ITP)        |        |     | 125     | ps    | 1     |
| Jitter, Cycle to cycle          | t <sub>jcy-cyc</sub> | Measurement from differential waveform, (CPU(1:0))       |        |     | 85      | ps    | 1     |

\*T<sub>A</sub> = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 2pF, R<sub>S</sub> = 33.2Ω, R<sub>P</sub> = 49.9Ω, I<sub>REF</sub> = 475Ω

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>3</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub> = 50Ω.

## Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

| PARAMETER                       | SYMBOL               | CONDITIONS*                                              | MIN    | TYP | MAX     | UNITS | Notes |
|---------------------------------|----------------------|----------------------------------------------------------|--------|-----|---------|-------|-------|
| Current Source Output Impedance | Z <sub>o</sub>       | V <sub>O</sub> = V <sub>x</sub>                          | 3000   |     |         | Ω     | 1     |
| Voltage High                    | V <sub>High</sub>    | Statistical measurement on single ended signal           | 660    |     | 850     | mV    | 1,3   |
| Voltage Low                     | V <sub>Low</sub>     |                                                          | -150   |     | 150     | mV    | 1,3   |
| Max Voltage                     | V <sub>ovs</sub>     | Measurement on single ended signal using absolute value. |        |     | 1150    | mV    | 1     |
| Min Voltage                     | V <sub>uds</sub>     |                                                          | -300   |     |         | mV    | 1     |
| Crossing Voltage (abs)          | V <sub>x(abs)</sub>  |                                                          | 250    |     | 550     | mV    | 1     |
| Crossing Voltage (var)          | d-V <sub>x</sub>     | Variation of crossing over all edges                     |        |     | 140     | mV    | 1     |
| Long Accuracy                   | ppm                  | see Tperiod min-max values                               | -300   |     | 300     | ppm   | 1,2   |
| Average period                  | Tperiod              | 100.00MHz nominal                                        | 9.9970 |     | 10.0030 | ns    | 2     |
|                                 |                      | 100.00MHz spread                                         | 9.9970 |     | 10.0533 | ns    | 2     |
| Absolute min period             | T <sub>absmin</sub>  | 100.00MHz nominal/spread                                 | 9.8720 |     |         | ns    | 1,2   |
| Rise Time                       | t <sub>r</sub>       | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       | 175    |     | 700     | ps    | 1     |
| Fall Time                       | t <sub>f</sub>       | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        | 175    |     | 700     | ps    | 1     |
| Rise Time Variation             | d-t <sub>r</sub>     | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       |        |     | 125     | ps    | 1     |
| Fall Time Variation             | d-t <sub>f</sub>     | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        |        |     | 125     | ps    | 1     |
| Duty Cycle                      | d <sub>i3</sub>      | Measurement from differential waveform                   | 45     |     | 55      | %     | 1     |
| Skew                            | t <sub>sk3</sub>     | V <sub>T</sub> = 50%                                     |        |     | 250     | ps    | 1     |
| Jitter, Cycle to cycle          | t <sub>jcy-cyc</sub> | Measurement from differential waveform                   |        |     | 125     | ps    | 1     |

\*T<sub>A</sub> = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 2pF, R<sub>S</sub> = 33.2Ω, R<sub>P</sub> = 49.9Ω, I<sub>REF</sub> = 475Ω

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>3</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub> = 50Ω.

## Electrical Characteristics - PCICLK/PCICLK\_F

| PARAMETER              | SYMBOL               | CONDITIONS*                                      | MIN | TYP | MAX  | UNITS | NOTES |
|------------------------|----------------------|--------------------------------------------------|-----|-----|------|-------|-------|
| Output Impedance       | R <sub>DSP</sub>     | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12  |     | 55   | Ω     | 1     |
| Output High Voltage    | V <sub>OH</sub>      | I <sub>OH</sub> = -1 mA                          | 2.4 |     |      | V     | 1     |
| Output Low Voltage     | V <sub>OL</sub>      | I <sub>OL</sub> = 1 mA                           |     |     | 0.55 | V     | 1     |
| Output High Current    | I <sub>OH</sub>      | V <sub>OH</sub> @ MIN = 1.0 V                    | -33 |     |      | mA    | 1     |
|                        |                      | V <sub>OH</sub> @ MAX = 3.135 V                  |     |     | -33  | mA    | 1     |
| Output Low Current     | I <sub>OL</sub>      | V <sub>OL</sub> @ MIN = 1.95 V                   | 30  |     |      | mA    | 1     |
|                        |                      | V <sub>OL</sub> @ MAX = 0.4 V                    |     |     | 38   | mA    | 1     |
| Edge Rate              | t <sub>slewr/f</sub> | Rising/Falling edge rate                         | 1   |     | 4    | V/ns  | 1     |
| Rise Time              | t <sub>r</sub>       | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.5 |     | 2    | ns    | 1     |
| Fall Time              | t <sub>f</sub>       | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.5 |     | 2    | ns    | 1     |
| Duty Cycle             | d <sub>t1</sub>      | V <sub>T</sub> = 1.5 V                           | 45  |     | 55   | %     | 1     |
| Group Skew             | t <sub>skew</sub>    | V <sub>T</sub> = 1.5 V                           |     |     | 500  | ps    | 1     |
| Jitter, Cycle to cycle | t <sub>jcy-cyc</sub> | V <sub>T</sub> = 1.5 V                           |     |     | 250  | ps    | 1     |

\*T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, C<sub>L</sub> = 4 pF with R<sub>S</sub> = 33Ω (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - 48MHz/USB48MHz/24\_48MHz

| PARAMETER              | SYMBOL                   | CONDITIONS*                                      | MIN     | TYP | MAX     | UNITS | NOTES |
|------------------------|--------------------------|--------------------------------------------------|---------|-----|---------|-------|-------|
| Long Accuracy          | ppm                      | see Tperiod min-max values                       | -100    |     | 100     | ppm   | 1     |
| Clock period           | Tperiod                  | 48.00MHz output nominal                          | 20.8313 |     | 20.8354 | ns    |       |
| Output Impedance       | R <sub>DSP</sub>         | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12      |     | 55      | Ω     | 1     |
| Output High Voltage    | V <sub>OH</sub>          | I <sub>OH</sub> = -1 mA                          | 2.4     |     |         | V     | 1     |
| Output Low Voltage     | V <sub>OL</sub>          | I <sub>OL</sub> = 1 mA                           |         |     | 0.55    | V     | 1     |
| Output High Current    | I <sub>OH</sub>          | V <sub>OH</sub> @ MIN = 1.0 V                    | -33     |     |         | mA    | 1     |
|                        |                          | V <sub>OH</sub> @ MAX = 3.135 V                  |         |     | -33     | mA    | 1     |
| Output Low Current     | I <sub>OL</sub>          | V <sub>OL</sub> @ MIN = 1.95 V                   | 30      |     |         | mA    | 1     |
|                        |                          | V <sub>OL</sub> @ MAX = 0.4 V                    |         |     | 38      | mA    | 1     |
| Edge Rate              | t <sub>slewr/f</sub>     | Rising/Falling edge rate                         | 1       |     | 4       | V/ns  | 1     |
| Edge Rate              | t <sub>slewr/f_USB</sub> | USB48 Rising/Falling edge rate                   | 1       |     | 2       | V/ns  | 1     |
| Rise Time              | t <sub>r</sub>           | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.5     |     | 2       | ns    | 1     |
| Fall Time              | t <sub>f</sub>           | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.5     |     | 2       | ns    | 1     |
| Rise Time              | t <sub>r_USB</sub>       | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 1       |     | 2       | ns    | 1     |
| Fall Time              | t <sub>f_USB</sub>       | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 1       |     | 2       | ns    | 1     |
| Duty Cycle             | d <sub>t1</sub>          | V <sub>T</sub> = 1.5 V                           | 45      |     | 55      | %     | 1     |
| Jitter, Cycle to cycle | t <sub>jcy-cyc</sub>     | V <sub>T</sub> = 1.5 V                           |         |     | 500     | ps    | 1     |

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 4 pF with Rs = 33Ω (Rs is used in USB48MHz test only)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - DOT\_96MHz 0.7V Current Mode Differential Pair

| PARAMETER                       | SYMBOL               | CONDITIONS*                                              | MIN     | TYP | MAX     | UNITS | Notes |
|---------------------------------|----------------------|----------------------------------------------------------|---------|-----|---------|-------|-------|
| Current Source Output Impedance | Z <sub>o</sub>       | V <sub>O</sub> = V <sub>x</sub>                          | 3000    |     |         | Ω     | 1     |
| Voltage High                    | V <sub>High</sub>    | Statistical measurement on single ended signal           | 660     |     | 850     | mV    | 1,3   |
| Voltage Low                     | V <sub>Low</sub>     |                                                          | -150    |     | 150     | mV    | 1,3   |
| Max Voltage                     | V <sub>ovs</sub>     | Measurement on single ended signal using absolute value. |         |     | 1150    | mV    | 1     |
| Min Voltage                     | V <sub>uds</sub>     |                                                          | -300    |     |         | mV    | 1     |
| Crossing Voltage (abs)          | V <sub>x(abs)</sub>  |                                                          | 250     |     | 550     | mV    | 1     |
| Crossing Voltage (var)          | d-V <sub>cross</sub> | Variation of crossing over all edges                     |         |     | 140     | mV    | 1     |
| Long Accuracy                   | ppm                  | see Tperiod min-max values                               | -100    |     | 100     | ppm   | 1,2   |
| Average period                  | Tperiod              | 96.00MHz nominal                                         | 10.4135 |     | 10.4198 | ns    | 2     |
| Absolute min period             | T <sub>absmin</sub>  | 96.00MHz nominal                                         | 10.1635 |     |         | ns    | 1,2   |
| Rise Time                       | t <sub>r</sub>       | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       | 175     |     | 700     | ps    | 1     |
| Fall Time                       | t <sub>f</sub>       | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        | 175     |     | 700     | ps    | 1     |
| Rise Time Variation             | d-t <sub>r</sub>     | V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V       |         |     | 125     | ps    | 1     |
| Fall Time Variation             | d-t <sub>f</sub>     | V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V        |         |     | 125     | ps    | 1     |
| Duty Cycle                      | d <sub>i3</sub>      | Measurement from differential waveform                   | 45      |     | 55      | %     | 1     |
| Jitter, Cycle to cycle          | t <sub>jcy-cyc</sub> | Measurement from differential waveform                   |         |     | 250     | ps    | 1     |

\*TA = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 2pF, R<sub>S</sub> = 33.2Ω, R<sub>P</sub> = 49.9Ω, I<sub>REF</sub> = 475Ω

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>3</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub> = 50Ω.

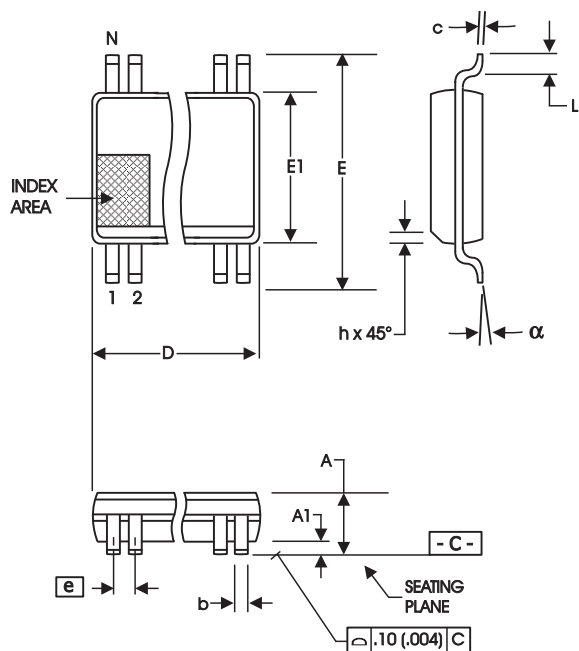
## Electrical Characteristics - REF-14.318MHz

| PARAMETER           | SYMBOL                 | CONDITIONS                                                        | MIN     | TYP | MAX     | UNITS | Notes |
|---------------------|------------------------|-------------------------------------------------------------------|---------|-----|---------|-------|-------|
| Long Accuracy       | ppm                    | see Tperiod min-max values                                        | -300    |     | 300     | ppm   | 1,2   |
| Clock period        | T <sub>period</sub>    | 14.318MHz output nominal                                          | 69.8270 |     | 69.8550 | ns    | 2     |
| Output High Voltage | V <sub>OH</sub>        | I <sub>OH</sub> = -1 mA                                           | 2.4     |     |         | V     | 1     |
| Output Low Voltage  | V <sub>OL</sub>        | I <sub>OL</sub> = 1 mA                                            |         |     | 0.4     | V     | 1     |
| Output High Current | I <sub>OH</sub>        | V <sub>OH</sub> @ MIN = 1.0 V,<br>V <sub>OH</sub> @ MAX = 3.135 V | -29     |     | -23     | mA    | 1     |
| Output Low Current  | I <sub>OL</sub>        | V <sub>OL</sub> @ MIN = 1.95 V,<br>@ MAX = 0.4 V                  | 29      |     | 27      | mA    | 1     |
| Edge Rate           | t <sub>slewr/f</sub>   | Rising/Falling edge rate                                          | 1       |     | 4       | V/ns  | 1     |
| Rise Time           | t <sub>r1</sub>        | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V                  | 1       |     | 2       | ns    | 1     |
| Fall Time           | t <sub>f1</sub>        | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V                  | 1       |     | 2       | ns    | 1     |
| Duty Cycle          | d <sub>t1</sub>        | V <sub>T</sub> = 1.5 V                                            | 45      |     | 55      | %     | 1     |
| Jitter              | t <sub>jycyc-cyc</sub> | V <sub>T</sub> = 1.5 V                                            |         |     | 1000    | ps    | 1     |

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 4 pF with Rs = 39Ω (Rs is used in USB48MHz test only)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



**56-Lead, 300 mil Body, 25 mil, SSOP**

| SYMBOL | In Millimeters<br>COMMON DIMENSIONS |       | In Inches<br>COMMON DIMENSIONS |       |
|--------|-------------------------------------|-------|--------------------------------|-------|
|        | MIN                                 | MAX   | MIN                            | MAX   |
| A      | 2.41                                | 2.80  | .095                           | .110  |
| A1     | 0.20                                | 0.40  | .008                           | .016  |
| b      | 0.20                                | 0.34  | .008                           | .0135 |
| c      | 0.13                                | 0.25  | .005                           | .010  |
| D      | SEE VARIATIONS                      |       | SEE VARIATIONS                 |       |
| E      | 10.03                               | 10.68 | .395                           | .420  |
| E1     | 7.40                                | 7.60  | .291                           | .299  |
| e      | 0.635 BASIC                         |       | 0.025 BASIC                    |       |
| h      | 0.38                                | 0.64  | .015                           | .025  |
| L      | 0.50                                | 1.02  | .020                           | .040  |
| N      | SEE VARIATIONS                      |       | SEE VARIATIONS                 |       |
| a      | 0°                                  | 8°    | 0°                             | 8°    |

**VARIATIONS**

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 18.31 | 18.55 | .720     | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**954141AFLF-T**

Example:

**XXXX A F LF-T**

Designation for tape and reel packaging

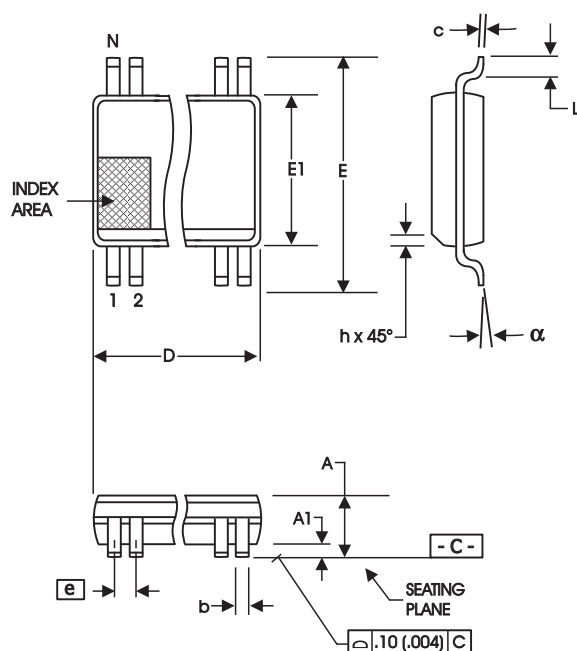
Annealed Lead Free (Optional)

Package Type

F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type



**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**  
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters    |      | In Inches         |      |
|--------|-------------------|------|-------------------|------|
|        | COMMON DIMENSIONS |      | COMMON DIMENSIONS |      |
|        | MIN               | MAX  | MIN               | MAX  |
| A      | --                | 1.20 | --                | .047 |
| A1     | 0.05              | 0.15 | .002              | .006 |
| A2     | 0.80              | 1.05 | .032              | .041 |
| b      | 0.17              | 0.27 | .007              | .011 |
| c      | 0.09              | 0.20 | .0035             | .008 |
| D      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| E      | 8.10 BASIC        |      | 0.319 BASIC       |      |
| E1     | 6.00              | 6.20 | .236              | .244 |
| e      | 0.50 BASIC        |      | 0.020 BASIC       |      |
| L      | 0.45              | 0.75 | .018              | .030 |
| N      | SEE VARIATIONS    |      | SEE VARIATIONS    |      |
| a      | 0°                | 8°   | 0°                | 8°   |
| aaa    | --                | 0.10 | --                | .004 |

**VARIATIONS**

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 13.90 | 14.10 | .547     | .555 |

Reference Doc.: JEDEC Publication 95, M O-153

10-0039

## Ordering Information

**954141AGLF-T**

Example:

**XXXX A G LF- T**

- XXXX — Designation for tape and reel packaging
- A — Annealed Lead Free (Optional)
- G — Package Type  
G = TSSOP
- LF — Revision Designator (will not correlate with datasheet revision)
- T — Device Type

### Revision History

| Rev. | Issue Date | Description                                                                                                                        | Page #  |
|------|------------|------------------------------------------------------------------------------------------------------------------------------------|---------|
| N/A  | 10/13/2004 | Added TSSOP ordering information                                                                                                   | 18      |
| A    | 3/30/2009  | 1. Corrected single-ended clock loading.<br>2. Updated part ordering information.<br>3. Removed water marks.<br>4. Moved to final. | Various |
|      |            |                                                                                                                                    |         |
|      |            |                                                                                                                                    |         |
|      |            |                                                                                                                                    |         |

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