

High Voltage 3-Phase Motor Drivers

Features and Benefits

- Built-in bootstrap diodes with limit resistors
- Built-in protection circuit for controlling power supply voltage drop on VCC and VB (UVLO)
- Built-in Thermal Shutdown (TSD)
- Built-in Current Limiter (OCL)
- Built-in Overcurrent Protection (OCP)
- 7.5 V regulated output
- Output of fault signal during operation of protection circuit
- Small SOP package

Package: 27-pin SOP



Not to scale

Description

The SX68000MH series provides the solution for controlling 3-phase full bridges that utilize MOSFETs rated at 250 V/2 A, 500 V/1.5 A, or 500 V/2.5 A.

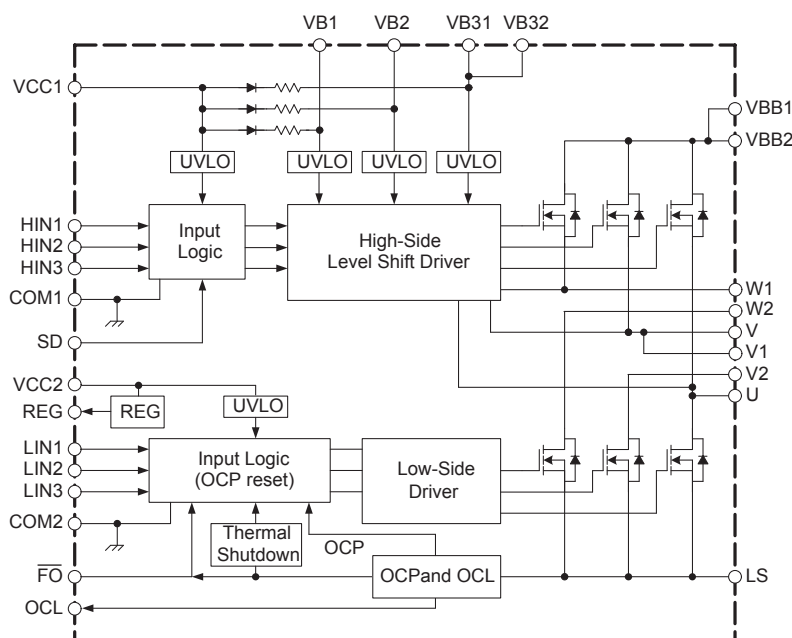
The IC includes in a single package: protection functions such as UVLO (protection circuit for controlling power supply voltage drop), OCP (overcurrent protection), TSD (thermal shutdown), and OCL (current limiting), and a pre-driver with \overline{FO} (Fault Output) terminal and bootstrap diodes with limit resistors.

The SX68000MH series is packaged in a fully-molded SOP with 27 pins at 1.2 mm pitch. Body size: 22 × 14.1 × 2.1 mm.

Applications

- Small motor control:
 - Air conditioning fan
 - White goods cooling fans
 - Ventilation blowers

Functional Block Diagram



Selection Guide (Values at $T_A = 25^\circ\text{C}$)

Part Number	Rating		MOSFET V_{DSS} (V)	I_O (A)	I_{OP} (A)	P_D (W)	Thermal Resistance	
	(V)	(A)					Junction to Case, $R_{\theta JC}$ ($^\circ\text{C/W}$)	Junction to Ambient, $R_{\theta JA}$ ($^\circ\text{C/W}$)
SX68001MH	250	2	250	2	3	3	15	41.7
SX68002MH	500	1.5	500	1.5	2.25			
SX68003MH	500	2.5	500	2.5	3.75			

Absolute Maximum Ratings, valid at $T_A = 25^\circ\text{C}$

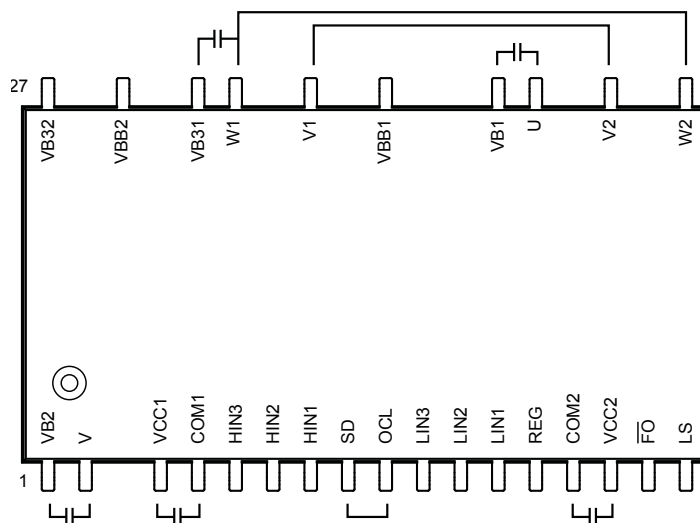
Characteristic	Symbol	Notes	Rating	Unit
MOSFET Breakdown Voltage	V_{DSS}	SX68001MH	250	V
		SX68002MH	500	V
		SX68003MH	500	V
Logic Supply Voltage	V_{CC}	VCC to COM	20	V
Bootstrap Voltage	V_{BS}	VB to high side (U,V,W)	20	V
Output Current (Continuous)	I_O	SX68001MH	2	A
		SX68002MH	1.5	A
		SX68003MH	2.5	A
Output Current (Pulsed)	I_{OP}	SX68001MH	3	A
		SX68002MH	2.25	A
		SX68003MH	3.75	A
Output Current for Regulator	I_{REG}		35	mA
Input Voltage	V_{IN}	LINx, HINx, \overline{FO} , SD, LS pins	-0.5 to 7	V
Maximum Allowable Power Dissipation*	P_D	$T_A = 25^\circ\text{C}$	3	W
Thermal Resistance (Junction to Case)*	$R_{\theta JC}$	All circuits operating	15	$^\circ\text{C/W}$
Thermal Resistance (Junction to Ambient)*	$R_{\theta JA}$	All circuits operating	41.7	$^\circ\text{C/W}$
Case Operating Temperature	T_{OP}		-20 to 100	$^\circ\text{C}$
Junction Temperature (MOSFET)	T_J		150	$^\circ\text{C}$
Storage Temperature	T_{stg}		-40 to 150	$^\circ\text{C}$

*Mounted on 1.6 mm thick CEM-3 PCB, with 35 μm thick copper layer, without overmolding, in still air.

Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main Supply Voltage	V_{BB}	SX68001MH	—	140	200	V
		SX68002MH	—	280	400	V
		SX68003MH	—	280	400	V
Logic Supply Voltage	V_{CC}	VCC to COM	13.5	—	16.5	V
Dead Time	t_{DEAD}		1.5	—	—	μs
Bootstrap Capacitor	C_{BOOT}		1	—	—	μF
Pull-up Resistor (\overline{FO} pin)	R_{FO}		3.3	—	10	k Ω
Capacitor (\overline{FO} pin)	C_{FO}		0.001	—	0.01	μF
Shunt Resistor (LS pin)	R_S	SX68001MH	0.45	—	—	Ω
		SX68002MH	0.6	—	—	Ω
		SX68003MH	0.36	—	—	Ω

Pin-out Diagram



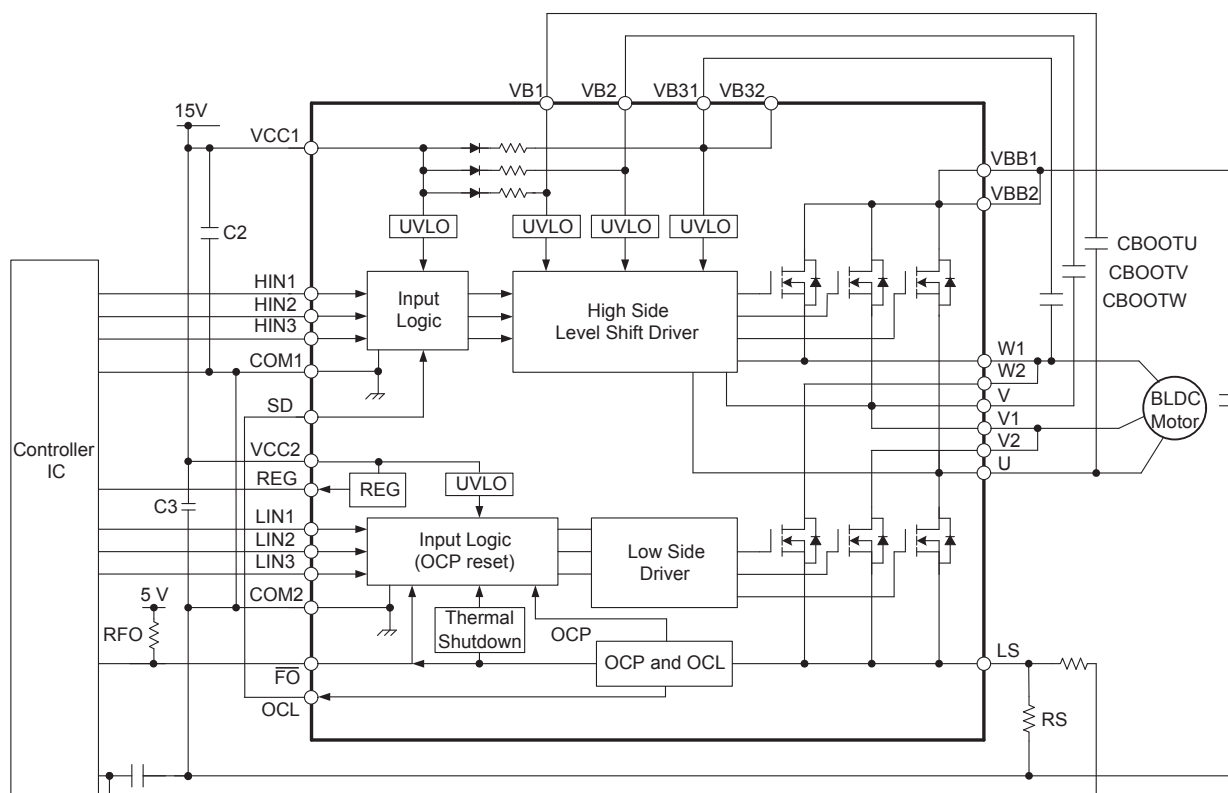
Terminal List Table

Number	Name	Function	Number	Name	Function
1	VB2	High-side bootstrap terminal (V phase)	14	COM2	Low-side GND terminal
2	V	Output of V-phase	15	VCC2	Low-side logic supply voltage
3	VCC1	High-side logic supply voltage	16	\overline{FO}	Fault signal output (open collector output)
4	COM1	High-side logic GND terminal	17	LS	Low-side MOSFET source terminal
5	HIN3	High-side input terminal (W-phase)	18	W2	Output of W phase (connect to W1)
6	HIN2	High-side input terminal (V-phase)	19	V2	Output of V phase (connect to V1)
7	HIN1	High-side input terminal (U-phase)	20	U	Output of U phase
8	SD	High-side shut down input	21	VB1	High-side bootstrap terminal (U phase)
9	OCL	Current limiter signal output (CMOS output)	22	VBB1	Main supply voltage 1 (connect VBB2 externally)
10	LIN3	Low-side input terminal (W phase)	23	V1	Output of V phase (connect to V2)
11	LIN2	Low-side input terminal (V phase)	24	W1	Output of W phase (connect to W2)
12	LIN1	Low-side input terminal (U phase)	25	VB31	High side bootstrap terminal (W phase)
13	REG	7.5 V regulator output	26	VBB2	Main supply voltage 2 (connect VBB1 externally)
			27	VB32	High side bootstrap terminal (W phase)

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature, T_A , of 25°C, unless otherwise stated.

Typical Application Circuit

Using current limiter function



To avoid malfunctions or permanent damage to the IC, observe the following guidelines for layout of the PCB:

- W1 and W2, as well as V1 and V2 must be externally connected to each other.
- If not using the Current Limiter (OCL) function, leave the OCL and SD pins open, but the SD pin should be connected to GND if significant external noise is observed.
- Place a pull-up resistor, RFO, between the 5 V or 3.3 V supply and the IC, selected according to anti-noise characteristics, even though a 1 M Ω pull-up resistor is built-in at $\overline{\text{FO}}$ pin. Note that connecting to the 5 V or 3.3 V supply without a pull-up resistor disables the TSD function (however, low-side UVLO protection and OCP function remain active).
- To avoid malfunctions resulting from noise interference, place a 0.001 to 0.01 μF ceramic capacitor (C1) between the $\overline{\text{FO}}$ and COM2 pins.
- To avoid malfunctions resulting from noise interference, the traces must be as short as possible between the IC and the bootstrap capacitors, CBOOTx ($\approx 1 \mu\text{F}$).
- One of the bootstrap capacitors for the W phase can be populated between pin 24 (W1) and pin 25 (VB31). Also, because pin 27 (VB32) and pin 25 are internally connected, pin 27 can be left open.
- To avoid malfunctions resulting from noise interference, place a 0.01 to 0.1 μF ceramic capacitor between the VCC1 and COM1 (C2), as well as the VCC2 and COM2 (C3) pins. Also, the traces between them must be as short as possible.
- To avoid malfunctions resulting from noise interference, the traces between the current sense resistor RS, which is placed between the LS and COM2 pins, and the IC must be as short and wide as possible.
- If the generated voltage on the LS pin exceeds 7 V, add a Zener diode between the LS and COM2 pins.

SX6800xMH ELECTRICAL CHARACTERISTICS Valid $T_A = 25^\circ\text{C}$; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Logic Supply Current	I_{CC}	$V_{CC} = 15\text{ V}$, $I_{REG} = 0\text{ A}$	–	4.6	8.5	mA
Bootstrap Supply Current	I_B	$V_B = 15\text{ V}$, $H_{IN} = 5\text{ V}$ per phase	–	140	400	μA
Input Voltage	V_{IH}	$V_{CC} = 15\text{ V}$, Output on	–	2	2.5	V
	V_{IL}	$V_{CC} = 15\text{ V}$, Output off	1	1.5	–	V
\overline{FO} Input Threshold Voltage	V_{FOIH}	$V_{CC} = 15\text{ V}$, Output on	–	2	2.5	V
	V_{FOIL}	$V_{CC} = 15\text{ V}$, Output off	1	1.5	–	V
Input Current	I_{IH}	$V_{CC} = 15\text{ V}$, $V_{IN} = 5\text{ V}$	–	230	500	μA
	I_{IL}	$V_{IN} = 0\text{ V}$	–	–	2	μA
High-Side Undervoltage Lock Out	V_{UVHL}	Between V_B and U, V, or W	9.0	10.0	11.0	V
	V_{UVHH}		9.5	10.5	11.5	V
Low-Side Undervoltage Lock Out	V_{UVLL}	Between V_{CC} and COM	10.0	11.0	12.0	V
	V_{UVLH}		10.5	11.5	12.5	V
\overline{FO} Terminal Output Voltage	V_{FOL}	$V_{CC} = 15\text{ V}$, $V_{FO} = 5\text{ V}$, $R_{FO} = 10\text{ k}\Omega$	0	–	0.5	V
	V_{FOH}		4.8	–	–	V
Overcurrent Limit Output Voltage	V_{OCLL}	$V_{CC} = 15\text{ V}$	0	–	0.5	V
	V_{OCLH}		4.5	–	5.5	V
Current Limit Reference Voltage	V_{LIM}	$V_{CC} = 15\text{ V}$	0.6175	0.65	0.6825	V
Overcurrent Protection Trip Voltage	V_{TRIP}	$V_{CC} = 15\text{ V}$	0.9	1.0	1.1	V
Overcurrent Protection Hold Time	t_p	$V_{CC} = 15\text{ V}$	20	25	–	μs
Overcurrent Protection Blanking Time	$t_{bk(ocp)}$	$V_{CC} = 15\text{ V}$	–	2	–	μs
Overcurrent Limit Blanking Time	$t_{bk(ocl)}$	$V_{CC} = 15\text{ V}$	–	2	–	μs
SD Terminal Blanking Time	$t_{bk(SD)}$	$V_{CC} = 15\text{ V}$	–	3.3	–	μs
Overtemperature Protection Activating and Releasing Temperature	T_{DH}	$V_{CC} = 15\text{ V}$, no heatsink and $I_{REG} = 0\text{ mA}$	135	150	165	$^\circ\text{C}$
	T_{DL}		105	120	135	$^\circ\text{C}$
Output Voltage for Regulator	V_{REG}	$I_{REG} = 35\text{ mA}$	6.75	7.5	8.25	V
Bootstrap Diode Leakage Current	I_{LBD}	SX68001MH $V_R = 250\text{ V}$	–	–	10	μA
		SX68002MH $V_R = 500\text{ V}$	–	–	10	μA
		SX68003MH $V_R = 500\text{ V}$	–	–	10	μA
Bootstrap Diode Forward Voltage	V_{FBD}	$I_F = 0.15\text{ A}$	–	1.0	1.3	V
Bootstrap Diode Series Resistor	R_{BD}		48	60	72	Ω
MOSFET Leakage Current	I_{DSS}	SX68001MH $V_{DS} = 250\text{ V}$	–	–	100	μA
		SX68002MH $V_{DS} = 500\text{ V}$	–	–	100	μA
		SX68003MH $V_{DS} = 500\text{ V}$	–	–	100	μA
MOSFET On State Resistance	$R_{DS(on)}$	SX68001MH $V_{CC} = 15\text{ V}$, $I_D = 1\text{ A}$, $V_{IN} = 5\text{ V}$	–	1.25	1.5	Ω
		SX68002MH $V_{CC} = 15\text{ V}$, $I_D = 0.75\text{ A}$, $V_{IN} = 5\text{ V}$	–	3.2	4.0	Ω
		SX68003MH $V_{CC} = 15\text{ V}$, $I_D = 1.25\text{ A}$, $V_{IN} = 5\text{ V}$	–	2.0	2.4	Ω
Diode Forward Voltage (MOSFET)	V_{SD}	SX68001MH $V_{CC} = 15\text{ V}$, $I_{SD} = 1\text{ A}$, $V_{IN} = 0\text{ V}$	–	1.1	1.5	V
		SX68002MH $V_{CC} = 15\text{ V}$, $I_{SD} = 0.75\text{ A}$, $V_{IN} = 0\text{ V}$	–	1.0	1.5	V
		SX68003MH $V_{CC} = 15\text{ V}$, $I_{SD} = 1.25\text{ A}$, $V_{IN} = 0\text{ V}$	–	1.0	1.5	V

SX68001MH SWITCHING CHARACTERISTICS Valid $T_A = 25^\circ\text{C}$; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-Side Switching Time	$t_{dH(on)}$	$V_{BB} = 150\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 1\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	800	–	ns
	t_{rH}		–	45	–	ns
	t_{rrH}		–	75	–	ns
	$t_{dH(off)}$		–	720	–	ns
	t_{fH}		–	40	–	ns
Low-Side Switching Time	$t_{dL(on)}$	$V_{BB} = 150\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 1\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	750	–	ns
	t_{rL}		–	50	–	ns
	t_{rrL}		–	70	–	ns
	$t_{dL(off)}$		–	660	–	ns
	t_{fL}		–	20	–	ns

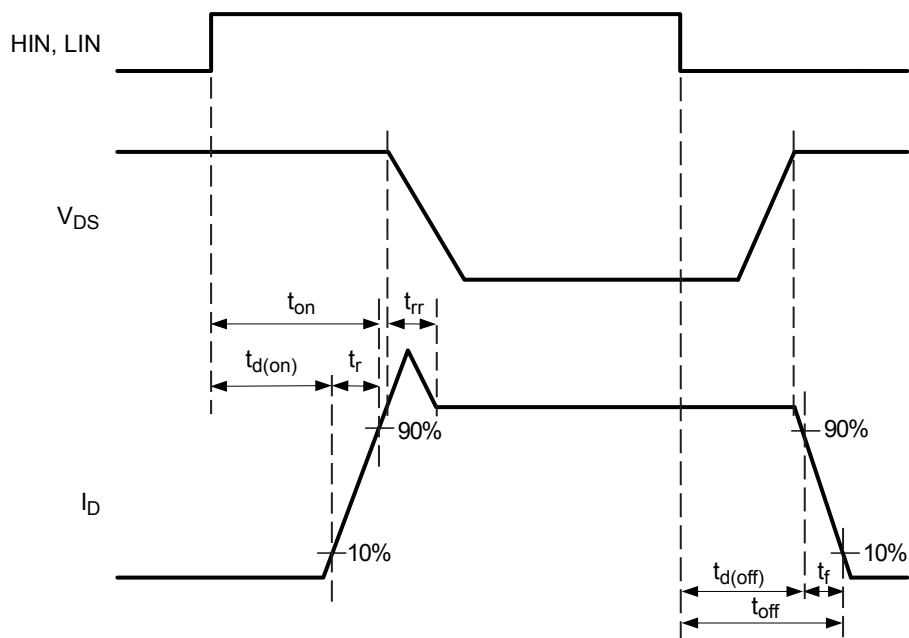
SX68002MH SWITCHING CHARACTERISTICS Valid $T_A = 25^\circ\text{C}$; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-Side Switching Time	$t_{dH(on)}$	$V_{BB} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 0.75\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	810	–	ns
	t_{rH}		–	60	–	ns
	t_{rrH}		–	120	–	ns
	$t_{dH(off)}$		–	815	–	ns
	t_{fH}		–	40	–	ns
Low-Side Switching Time	$t_{dL(on)}$	$V_{BB} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 0.75\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	760	–	ns
	t_{rL}		–	60	–	ns
	t_{rrL}		–	110	–	ns
	$t_{dL(off)}$		–	750	–	ns
	t_{fL}		–	30	–	ns

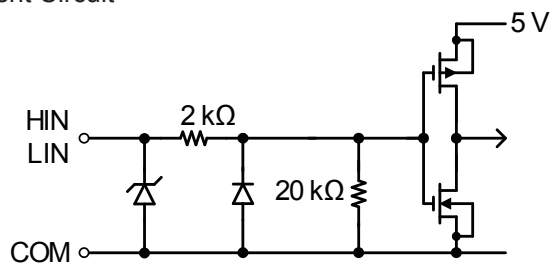
SX68003MH SWITCHING CHARACTERISTICS Valid $T_A = 25^\circ\text{C}$; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-Side Switching Time	$t_{dH(on)}$	$V_{BB} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 1.25\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	940	–	ns
	t_{rH}		–	100	–	ns
	t_{rrH}		–	135	–	ns
	$t_{dH(off)}$		–	975	–	ns
	t_{fH}		–	45	–	ns
Low-Side Switching Time	$t_{dL(on)}$	$V_{BB} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_D = 1.25\text{ A}$, $0\text{ V} < V_{IN} < 5\text{ V}$, see Switching Time Definition diagram	–	900	–	ns
	t_{rL}		–	105	–	ns
	t_{rrL}		–	135	–	ns
	$t_{dL(off)}$		–	905	–	ns
	t_{fL}		–	35	–	ns

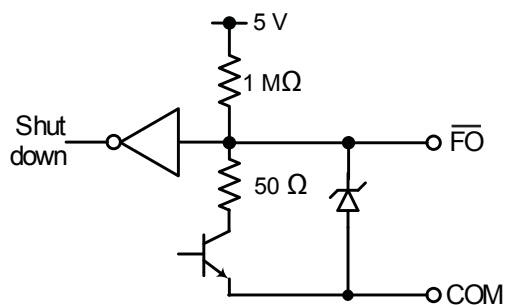
Switching Time Definition



HIN, LIN Internal Equivalent Circuit

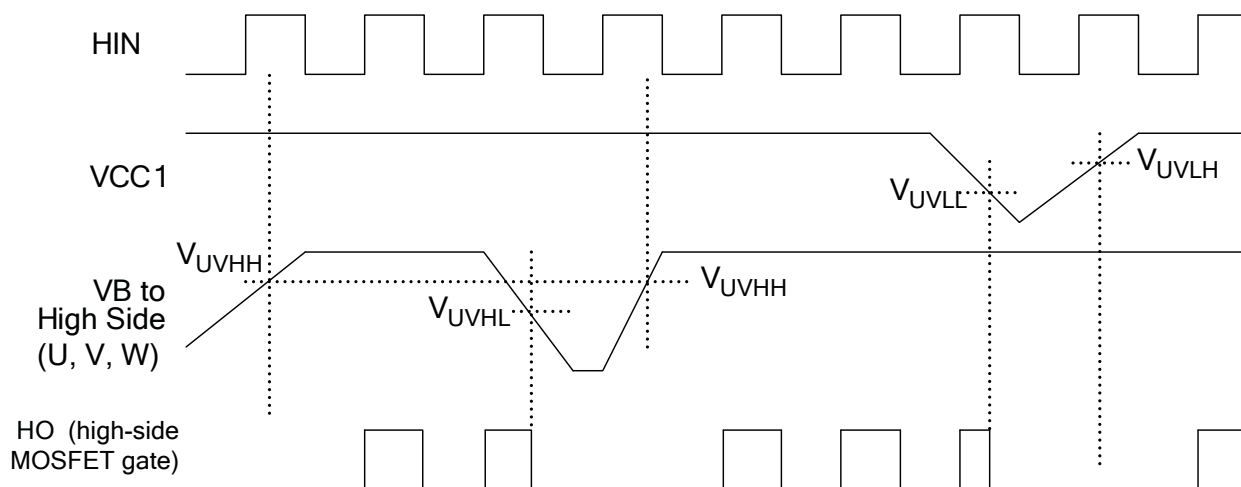


\overline{FO} Internal Equivalent Circuit

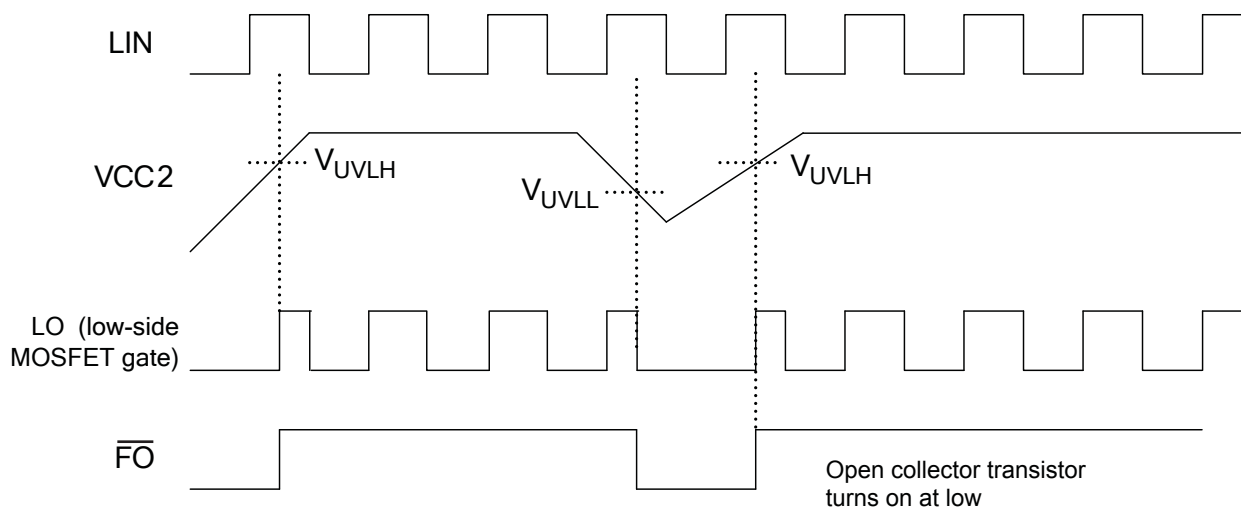


Protection Circuit Timing

UVLO Protection Circuit - High Side Timing



UVLO Protection Circuit - Low Side Timing

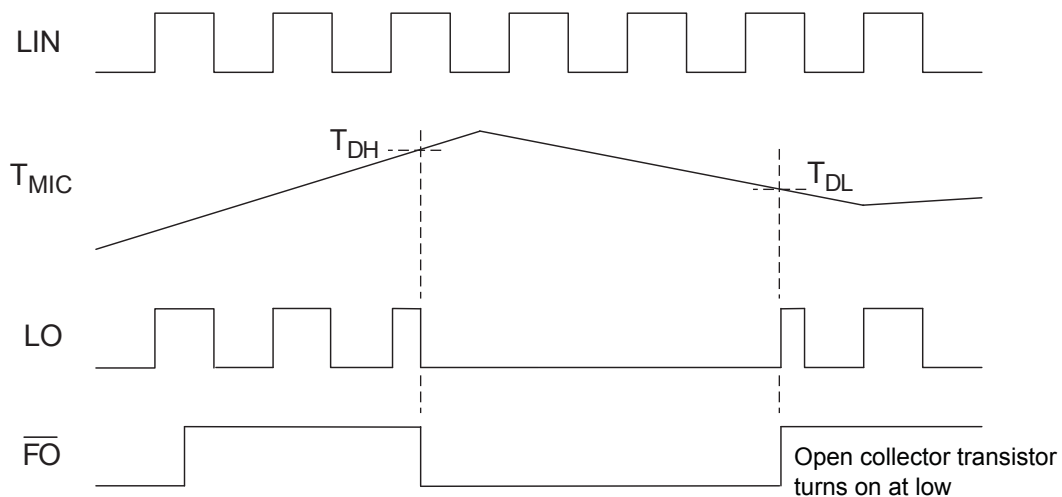


The diagram illustrates the timing of the OCP Release signal relative to other system signals. The signals shown are LIN, LO, LS, V_{TRIP} (1 V), and \overline{FO} . The \overline{FO} signal transitions from high to low at the start of the second LS pulse and back to high at the end of the second LS pulse. The OCP Release signal is shown as a horizontal line that transitions from high to low at the start of the second LS pulse and back to high at the end of the second LS pulse. The duration of the OCP Release signal is 25 μs .

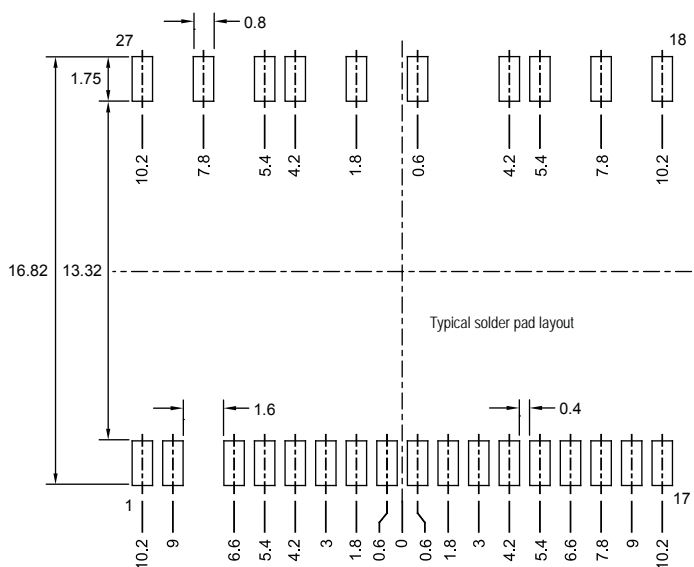
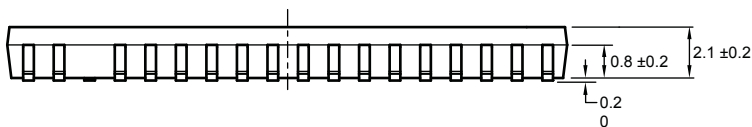
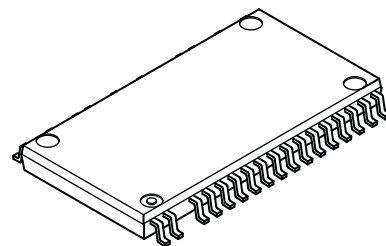
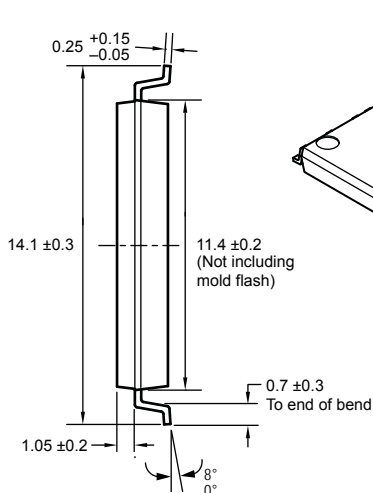
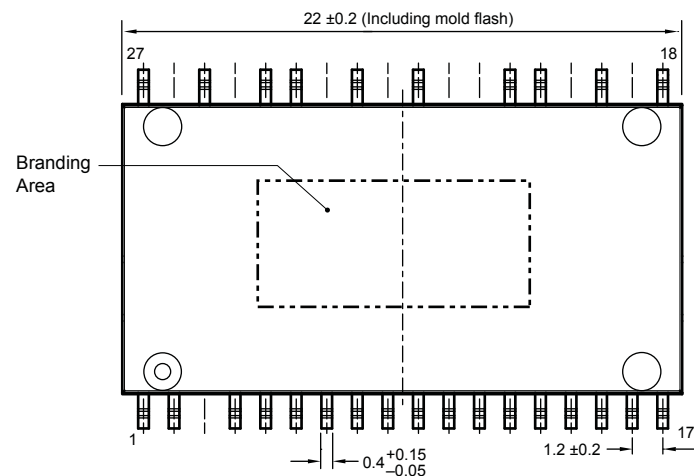
The timing diagram shows the following signals and their behavior:

- HIN**: High-side input signal.
- LIN**: Low-side input signal.
- HO**: High-side output signal. It transitions from high to low when **HIN** is high, and from low to high when **HIN** is low. The high-side gate shut-down time is 3.3 μs .
- LO**: Low-side output signal. It transitions from low to high when **LIN** is high, and from high to low when **LIN** is low. The low-side gate shut-down time is 3.3 μs .
- LS**: Low-side signal. It transitions from low to high when **LIN** is high, and from high to low when **LIN** is low. The pulse width is 2 μs .
- V_{TRIP} (1V)**: Trip voltage level, indicated by a dashed line.
- VOCL**: Output voltage level, indicated by a dashed line.
- OCL**: Output current level, indicated by a dashed line.
- SD**: Shutdown signal. It transitions from high to low when **LS** is high, and from low to high when **LS** is low. The shutdown time is 2 μs .
- FO**: Fault output signal. It transitions from high to low when **SD** is high, and from low to high when **SD** is low. The minimum delay between **SD** and **FO** is 20 μs .

TSD Protection Circuit Timing



Package Outline Drawing, SOP-27



Terminal core material: Cu
Terminal treatment: Solder plating (Sn 97.5%, Ag 2.5%)
Leadframe: LF1890

Dimensions in millimeters

Branding codes (exact appearance at manufacturer discretion):
1st line, type: SX6800xMH

2nd line, logo: SK lot: YMDDR

Where: Y is the last digit of the year of manufacture
M is the month (1 to 9, O, N, D)
DD is the day of the month (01 to 31)
R is a reference number

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5°C to 35°C) and the standard relative humidity (around 40% to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
260°±5°C 10 s
380°±5°C 5 s, using soldering iron

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1 MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

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In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

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