HARRIS SEMICONDUCTOR

ICM7211, ICM7212

4-Digit ICM7211 (LCD) and ICM7212 (LED) Display Drivers

December 1993

Features ICM7211 (LCD)

- **Four Digit Non-Multiplexed 7 Segment LCD Display Outputs With Backplane Driver**
- **Complete Onboard RC Oscillator to Generate Backplane Frequency**
- **Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master**
- **ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)**
- **ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface**
- **ICM7211 Decodes Binary to Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)**
- **ICM7211A Available in Surface Mount Package**

Features ICM7212AM (LED)

- **28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at >5mA Per Segment**
- **Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable**
- **ICM7212AM Device Provides Same Input Configuration and Output Decoding Options as the ICM7211AM**

Description

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

These devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226, and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The “A” versions will provide the “Code B” output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211 and ICM7212 family are packaged in a standard 40 lead plastic dual-in-line and 44 lead plastic MQFP packages and all inputs are fully protected against static discharge.

Ordering Information

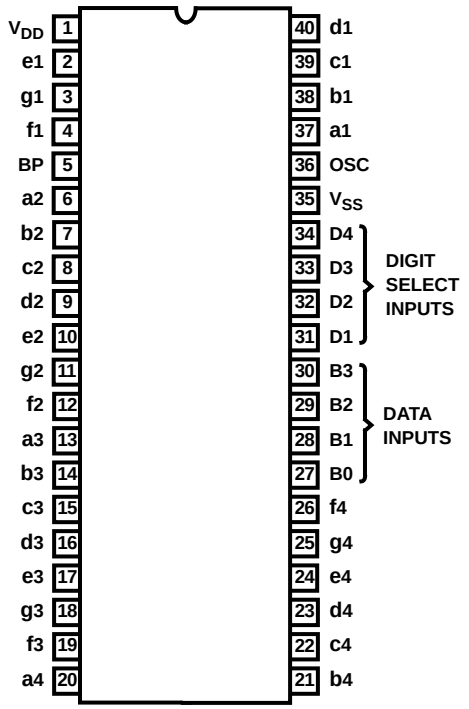
PART NUMBER	DISPLAY TYPE	DISPLAY DECODING	INPUT INTERFACING	DISPLAY DRIVE TYPE	TEMPERATURE RANGE	PACKAGE
ICM7211IPL	LCD	Hexadecimal	Multiplexed	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211MIPL	LCD	Hexadecimal	Microprocessor	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AIPL	LCD	Code B	Multiplexed	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AMIPL	LCD	Code B	Microprocessor	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AIM44	LCD	Code B	Multiplexed	Direct Drive	-40°C to +85°C	44 Lead MQFP Flatpack
ICM7211AMIM44	LCD	Code B	Microprocessor	Direct Drive	-40°C to +85°C	44 Lead MQFP Flatpack
ICM7212AMIPL	LED	Code B	Microprocessor	Common Anode	-40°C to +85°C	40 Lead Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

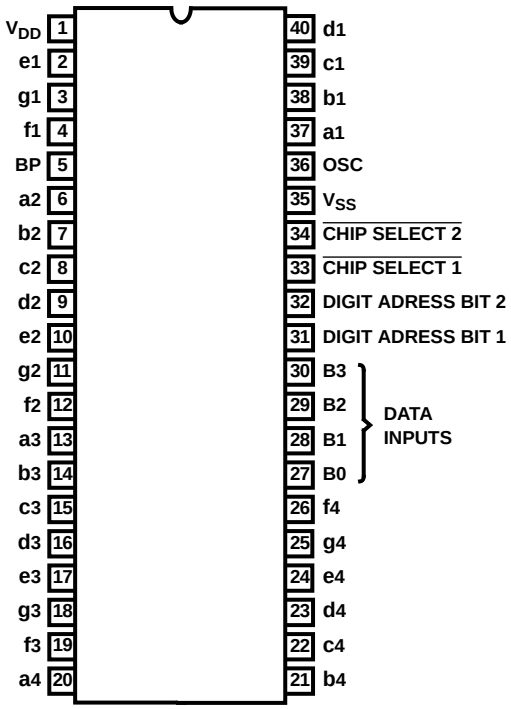
File Number **3158**

Pinouts

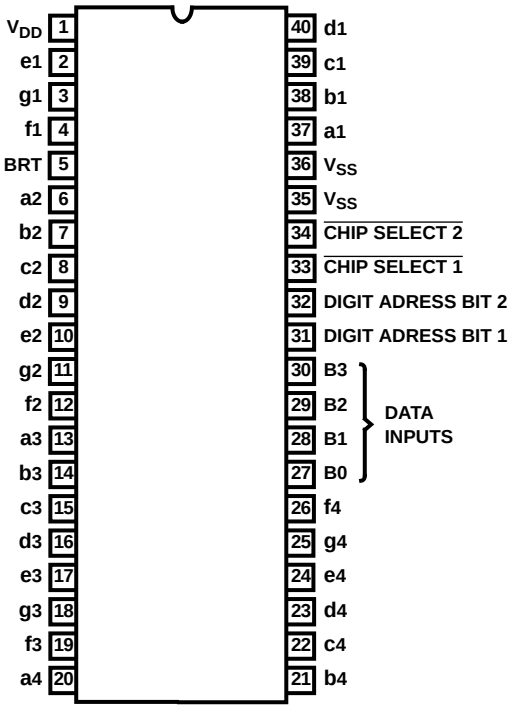
ICM7211, ICM7211A
(PDIP)
TOP VIEW



ICM7211M, ICM7211AM
(PDIP)
TOP VIEW

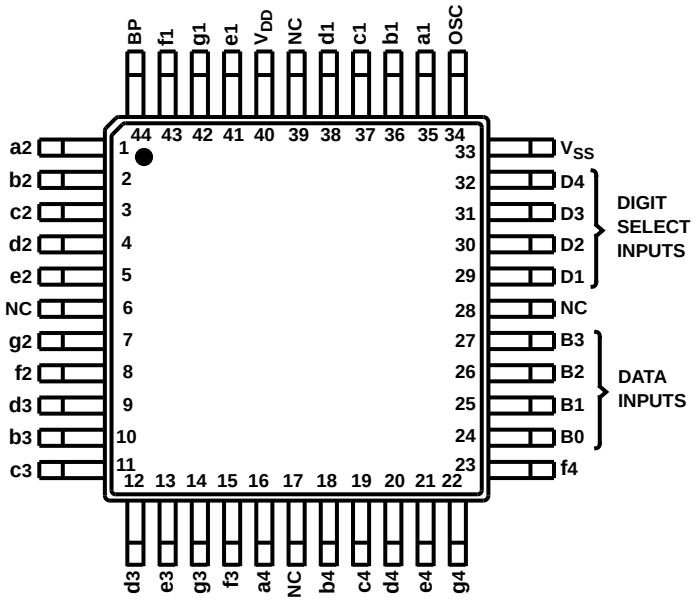


ICM7212AM
(PDIP)
TOP VIEW

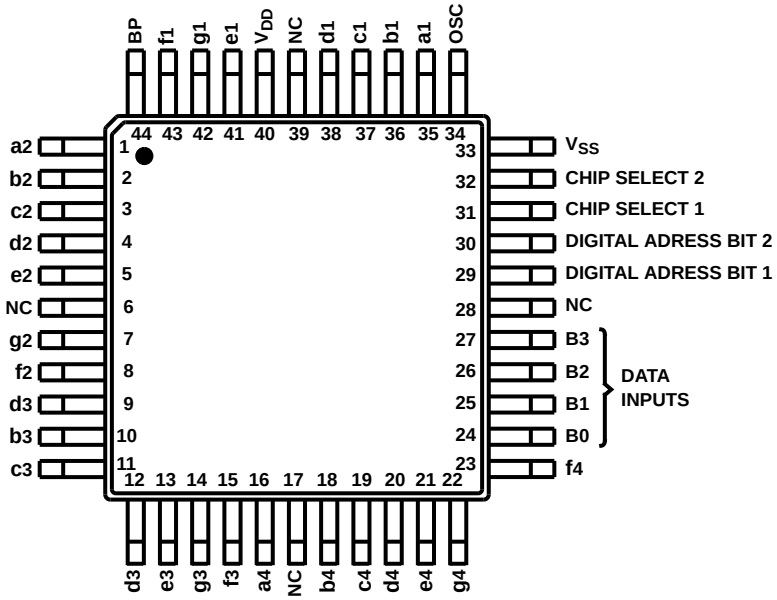


Pinouts (Continued)

ICM7211A
(PLASTIC FLATPACK)
TOP VIEW

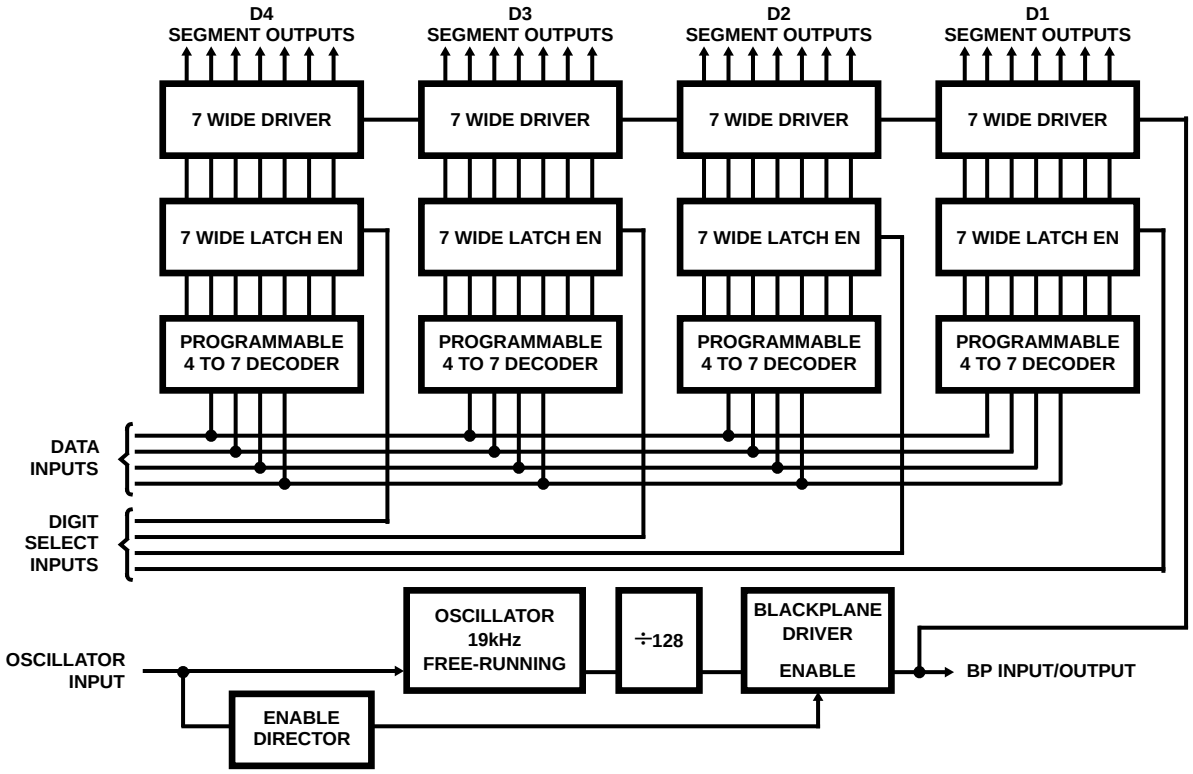


ICM7211AM
(PLASTIC FLATPACK)
TOP VIEW

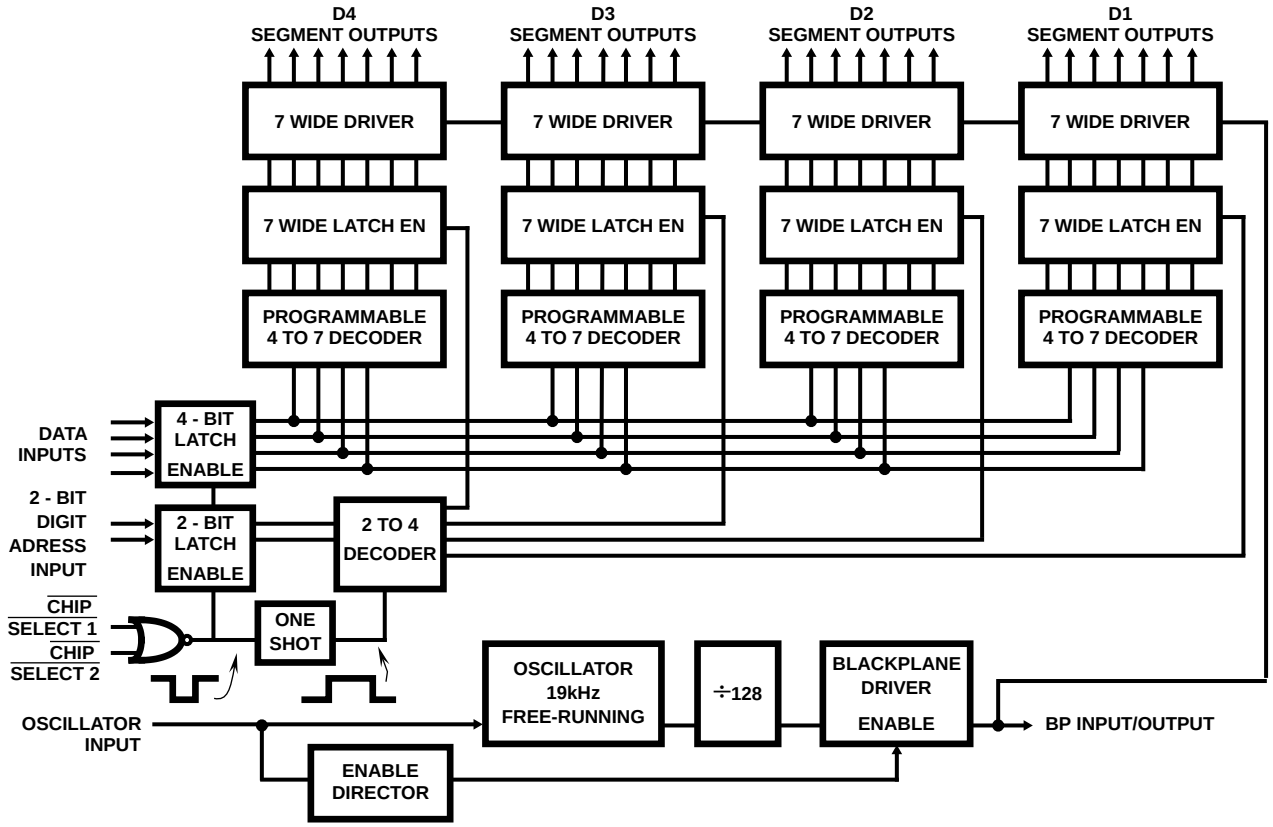


Functional Block Diagrams

ICM7211A

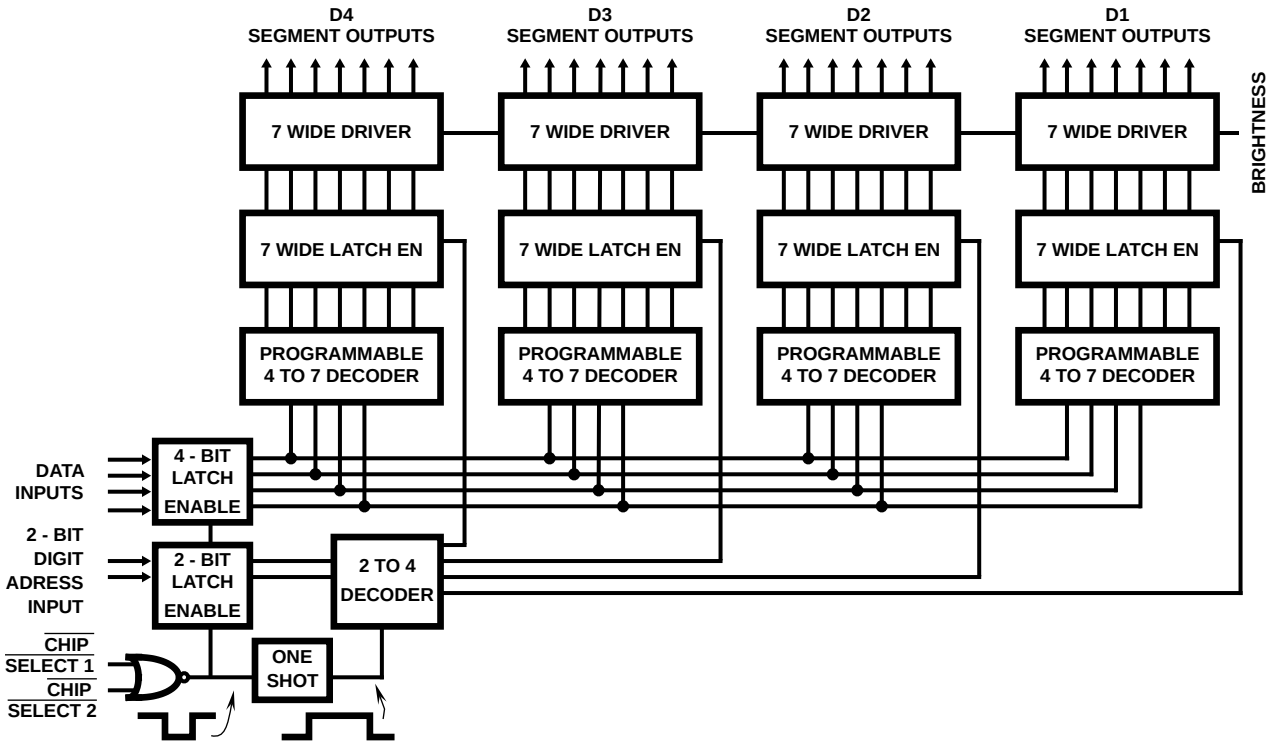


ICM7211AM



Functional Block Diagrams (Continued)

ICM7212AM



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Any Terminal) (Note 1) . . . V_{SS} - 0.3V to V_{DD}, + 0.3V
Storage Temperature Range . . . . . -55°C to +125°C
Lead Temperature (Soldering, 10s) . . . . . +300°C
Junction Temperature . . . . . +150°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	50°C/W
Plastic MQFP Package	80°C/W

Operating Temperature Range . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ICM7211 CHARACTERISTICS (LCD) V_{DD} = 5V 10%, T_A = +25°C, V_{SS} = 0V Unless Otherwise Specified.					
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		3	5	6	V
Operating Current, I_{DD}	Test circuit, Display blank	-	10	50	µA
Oscillator Input Current, I_{OSCI}	Pin 36	-	±2	±10	µA
Segment Rise/Fall Time, t_R, t_F	C_L = 200pF	-	0.5	-	µs
Backplane Rise/Fall Time, t_R, t_F	C_L = 5000pF	-	1.5	-	µs
Oscillator Frequency, f_{OSC}	Pin 36 Floating	-	19	-	kHz
Backplane Frequency, f_{BP}	Pin 36 Floating	-	150	-	Hz
ICM7212 CHARACTERISTICS (Common Anode LED)					
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		4	5	6	V
Operating Current Display Off, I_{STBY}	Pin 5 (Brightness), Pins 27-34 V_{SS}	-	10	50	µA
Operating Current, I_{DD}	Pin 5 at V_{DD}, Display all 8's	-	200	-	mA
Segment Leakage Current, I_{SLK}	Segment Off	-	±0.01	±1	µA
Segment On Current, I_{SEG}	Segment On, V_O = +3V	5	8	-	mA
INPUT CHARACTERISTICS (ICM7211 and ICM7212)					
Logical "1" Input Voltage, V_{IH}		4	-	-	V
Logical "0" Input Voltage, V_{IL}		-	-	1	V
Input Leakage Current, I_{ILK}	Pins 27-34	-	±0.01	±1	µA
Input Capacitance, C_{IN}	Pins 27-34	-	5		pF
BP/Brightness Input Leakage, I_{BPLK}	Measured at Pin 5 with Pin 36 at V_{SS}	-	±0.01	±1	µA
BP/Brightness Input Capacitance, C_{BPI}	All Devices	-	200	-	pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION					
Digit Select Active Pulse Width, t_{WH}	Refer to Timing Diagrams	1	-	-	µs
Data Setup Time, t_{DS}		500	-	-	ns
Data Hold Time, t_{DH}		200	-	-	ns
Inter-Digit Select Time, t_{IDS}		2	-	-	µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE					
Chip Select Active Pulse Width, t_{WL}	Other Chip Select either held active, or both driven together	200	-	-	ns
Data Setup Time, t_{DS}		100	-	-	ns
Data Hold Time, t_{DH}		10	0	-	ns
Inter-Chip Select Time, t_{ICS}		2	-	-	µs

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211 and ICM7212 be turned on first.

Input Definitions In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITIONS	FUNCTION	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V_{DD}	Oscillator Input	
		V_{SS}	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	

ICM7211 Multiplexed-Binary Input Configuration

INPUT	TERMINAL	CONDITIONS	FUNCTION
D1	31	V_{DD} = Inactive V_{SS} = Active	D1 Digit Select (Least Significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most Significant)

ICM7211M/ICM7212M Microprocessor Interface Input Configuration

INPUT	DESCRIPTION	TERMINAL	CONDITIONS	FUNCTION
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32	V_{DD} = Logical One V_{SS} = Logical Zero	
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either $\overline{Chip\ Select}$, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34	V_{DD} = Inactive V_{SS} = Active	

Timing Diagrams

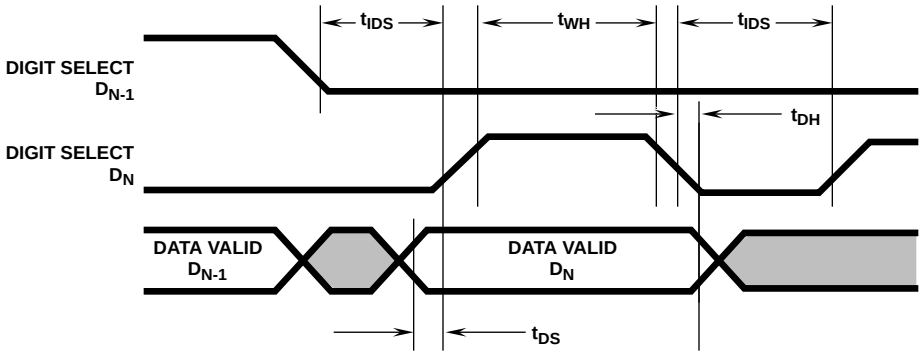


FIGURE 1. MULTIPLEXED INPUT

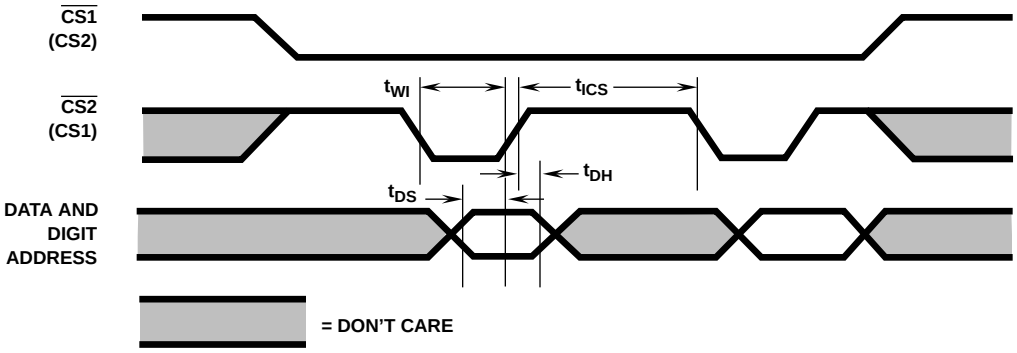


FIGURE 2. MICROPROCESSOR INTERFACE INPUT

Typical Performance Curves

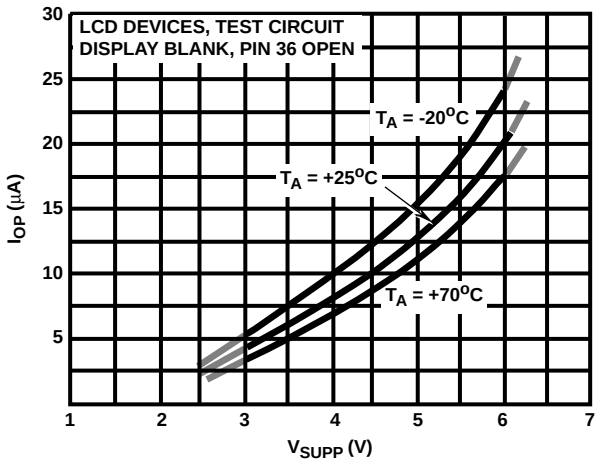


FIGURE 3. ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

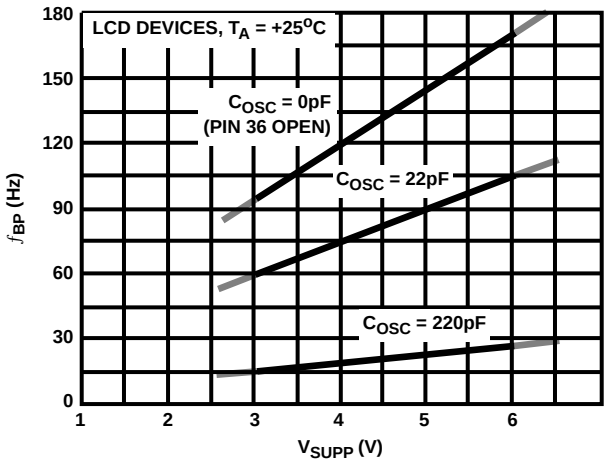


FIGURE 4. ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves (Continued)

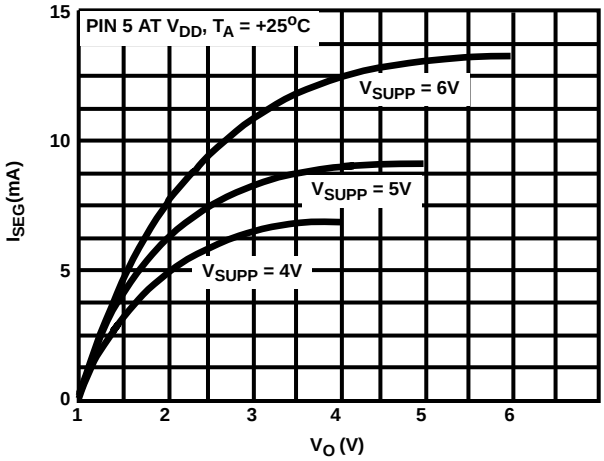


FIGURE 5. ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

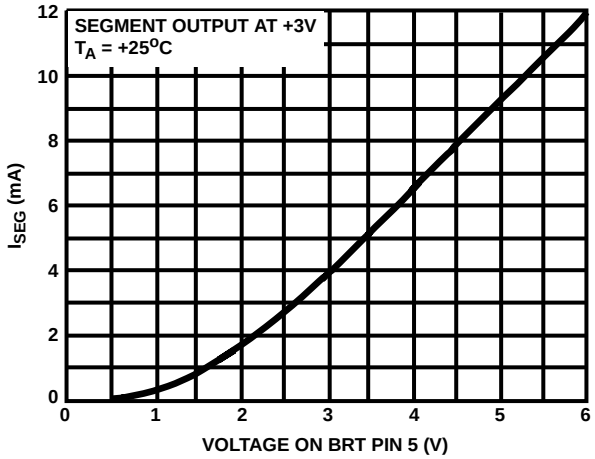


FIGURE 6. ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

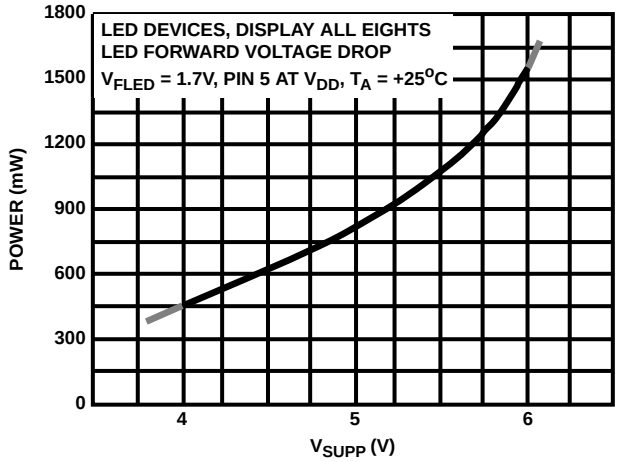


FIGURE 7. ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

Description Of Operation

LCD Devices

The LCD devices in the family (ICM7211, ICM7211A, ICM7211M, ICM7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n-channel and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the

larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5µs. The backplane output driver should handle the backplane to a display of 16 one-half inch characters. It is recommended, if more than four devices are to be slaved together, the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1 - 2µs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display type.

The onboard oscillator is designed to free run at approximately 19kHz at microampere current levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

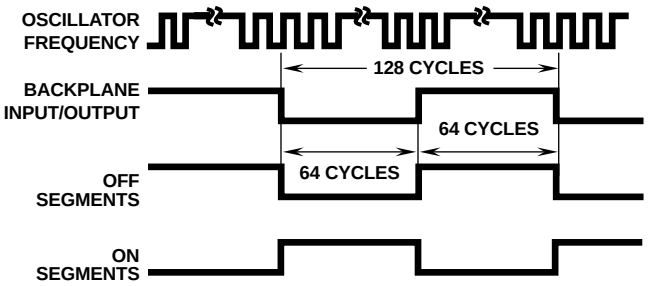


FIGURE 8. DISPLAY WAVEFORMS

LED Devices

The LED device in the family (ICM7212AM) provides outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRtrighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for “on” segments, and thus directly modulates the transistor’s “on” resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 9. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

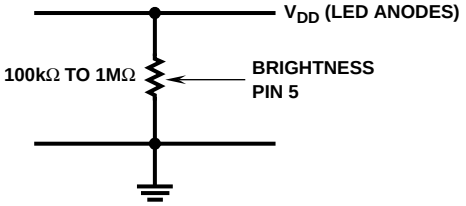


FIGURE 9. BRIGHTNESS CONTROL

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED device has two connections for V_{SS}; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1W at +25°C, derated linearly above +35°C to 500mW at +70°C (-15mW/°C above +35°C). Power dissipation for the device is given by:

$$P = (V_{SUPP} - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of “on” segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

Input Configurations and Output Codes

The standard devices in the ICM7211 and ICM7212 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211 and ICM7211M devices decode this binary input into a seven- segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, and ICM7212AM decode the binary input into seven-segment alphanumeric “Code B” output, i.e. 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will

correctly decode true BCD to a seven-segment decimal output.

TABLE 1. OUTPUT CODES

BINARY				HEXADECIMAL ICM7211 ICM7211M	CODE B ICM7211A ICM7212AM
B3	B2	B1	BO		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211 and ICM7211A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

The ICM7211M, ICM7211AM, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

An address of 00 writes into D4, DA2 = 0, DA1 = 1 writes into D3, DA2 = 1, DA1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 2, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

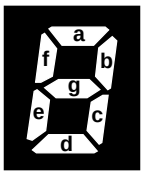


FIGURE 10. SEGMENT ASSIGNMENT

Test Circuit

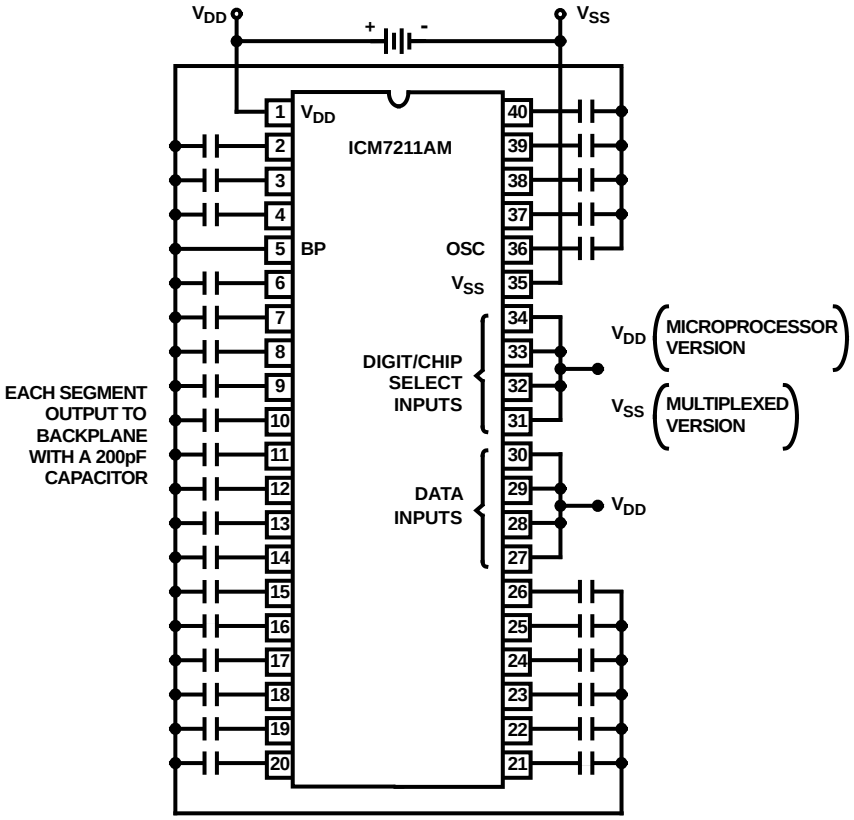


FIGURE 11.

Typical Applications

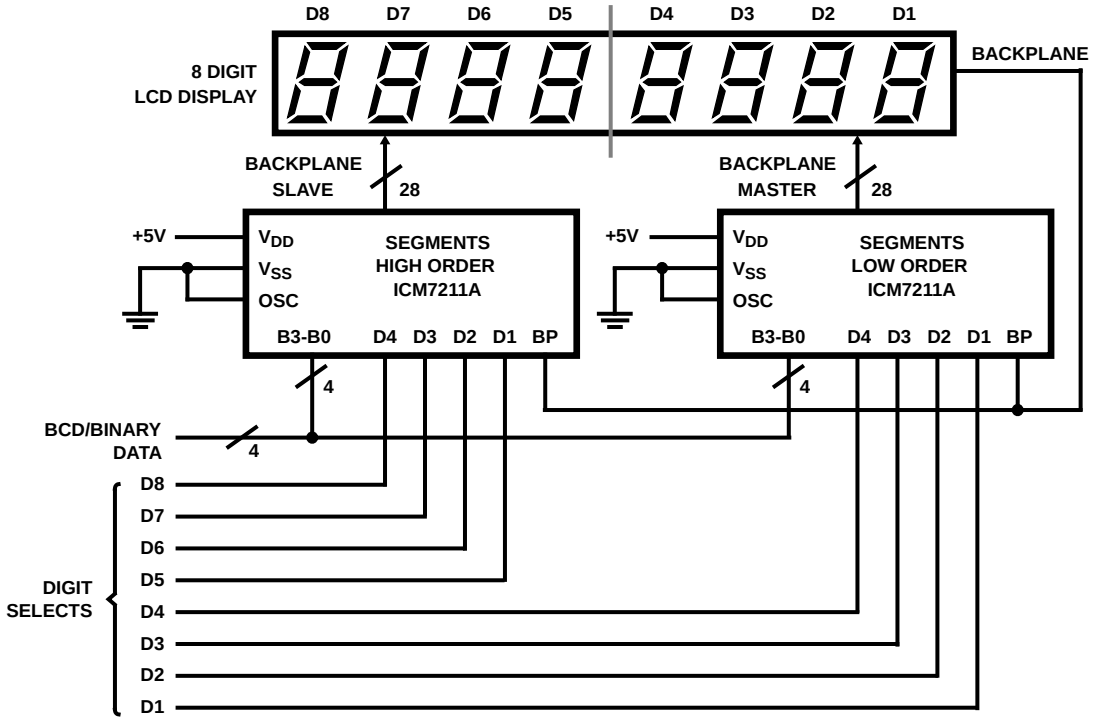


FIGURE 12. GANGED ICM7211's DRIVING 8-DIGIT LCD DISPLAY

Typical Applications (Continued)

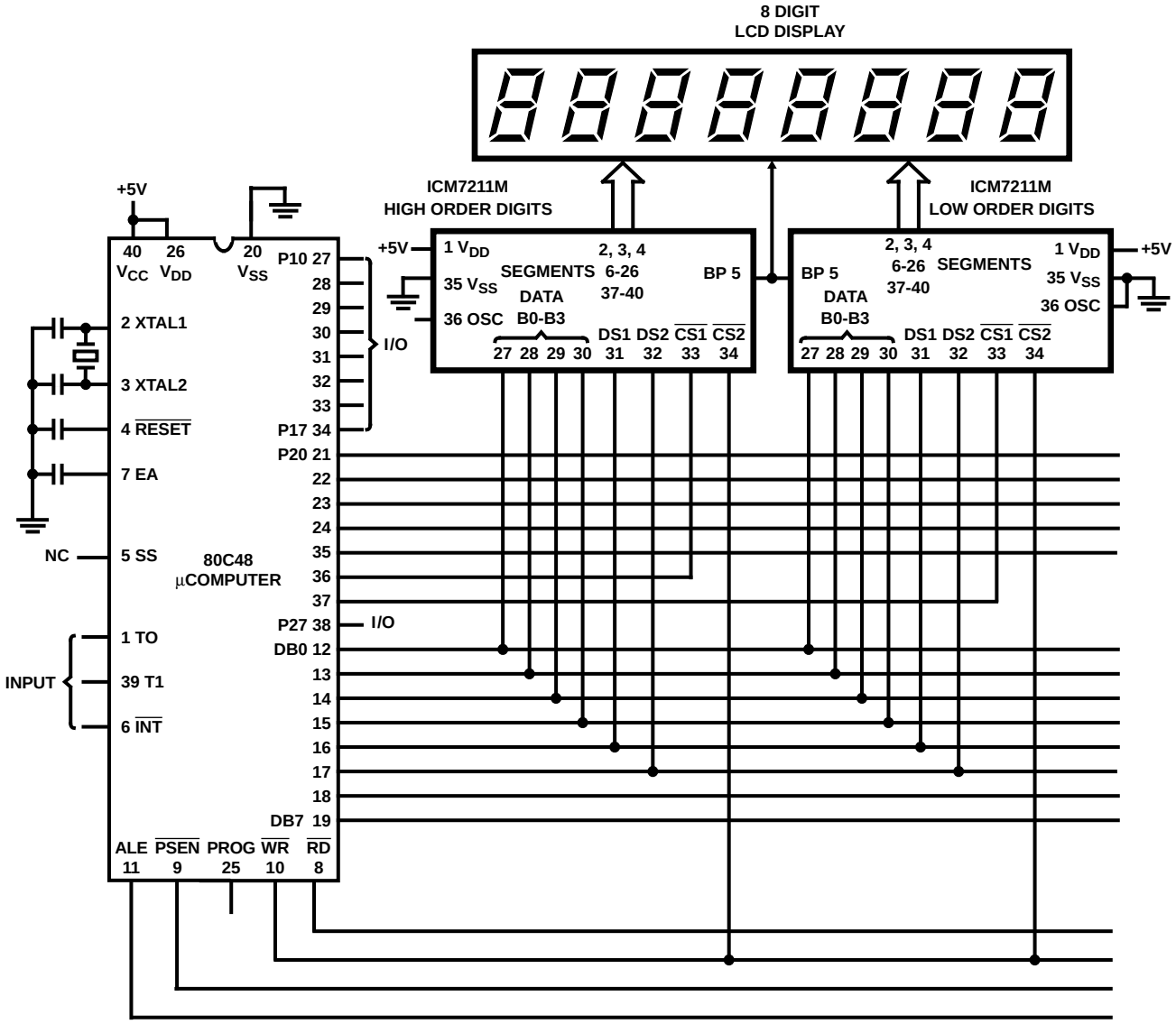


FIGURE 13. 80C48 MICROPROCESSOR INTERFACE