19-3069; Rev 4; 6/06

EVALUATION KIT AVAILABLE

IEEE 802.3af-Compliant Power-Over-Ethernet Interface/PWM Controller for Power Devices

General Description

The MAX5941A/MAX5941B integrate a complete power IC for powered devices (PD) in a power-over-ethernet (PoE) system. The MAX5941A/MAX5941B provide a PD interface and a compact DC-DC PWM controller suitable for flyback and forward converters in either isolated or nonisolated designs.

The MAX5941A/MAX5941B PD interface complies with the IEEE 802.3af standard, providing the PD with a detection signature, a classification signature, and an integrated isolation switch with programmable inrush current control. These devices also feature power-mode undervoltage lockout (UVLO) with wide hysteresis and power-good status outputs.

The MAX5941A/MAX5941B also integrate all the building blocks necessary for implementing DC-DC fixed-frequency isolated power supplies. These devices are a current-mode controller with an integrated high startup circuit suitable for isolated telecom/industrial voltage-range power supplies. A high-voltage startup circuit allows the PWM controller to draw power directly from the 18V to 67V input supply during startup. The switching frequency is internally trimmed to 275kHz ±10%, thus reducing magnetics and filter components. The MAX5941A allows an 85% operating duty cycle and can be used to implement flyback converters. The MAX5941B limits the operating duty cycle to less than 50% and can be used in single-ended forward converters. The MAX5941A/MAX5941B are designed to work with or without an external diode bridge in front of the PD.

The MAX5941A/MAX5941B are available in 16-pin SO packages.

Applications

IP Phones

Wireless Access Nodes

Internet Appliances

Computer Telephony

Security Cameras

Power Devices in Power-Over-Ethernet/ Power-Over-MDI

Typical Operating Circuit appears at end of data sheet.

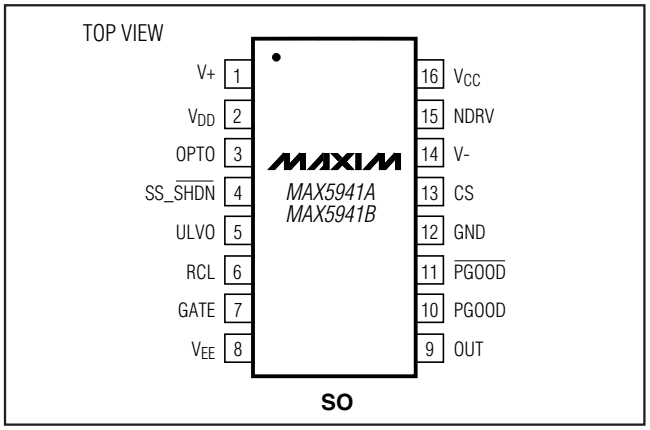
Features

- **Powered Device Interface**
  - **Fully Integrated IEEE 802.3af-Compliant PD Interface**
  - **PD Detection and Programmable Classification Signatures**
  - **Less than 10µA Leakage Current Offset During Detection**
  - **Integrated MOSFET for Isolation and Inrush Current Limiting**
  - **Gate Output Allows External Control of the Internal Isolation FET**
  - **Programmable Inrush Current Control**
  - **Programmable Undervoltage Lockout**
- **PWM Controller**
  - **Wide Input Range: 18V to 67V**
  - **Current-Mode Control**
  - **Leading-Edge Blanking**
  - **Internally Trimmed 275kHz ±10% Oscillator Soft-Start**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	MAX DUTY CYCLE (%)
MAX5941AESE	-40°C to +85°C	16 SO (S16M-6)	85
MAX5941ACSE	0°C to +70°C	16 SO (S16M-6)	85
MAX5941BESE	-40°C to +85°C	16 SO (S16M-6)	50
MAX5941BCSE	0°C to +70°C	16 SO (S16M-6)	50

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

IEEE 802.3af-Compliant Power-Over-Ethernet Interface/PWM Controller for Power Devices

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to V_{EE}, unless otherwise noted.)
GND .....-0.3V to +90V
OUT, $\overline{PGOOD}$ .....-0.3V to (GND + 0.3V)
RCL, GATE .....-0.3V to +12V
UVLO .....-0.3V to +8V
PGOOD to OUT .....-0.3V to (GND + 0.3V)
V+ to V- .....-0.3V to +90V
V_{DD} to V- .....-0.3V to +40V
V_{CC} to V- .....-0.3V to +12.5V
OPTO, NDRV, SS_$\overline{SHDN}$, CS to V- .....-0.3V to (V_{CC} + 0.3V)
Maximum Input/Output Current (Continuous)
OUT to V_{EE} 500mA
GND, RCL to V_{EE} 70mA
UVLO, $\overline{PGOOD}$, PGOOD to V_{EE} 20mA
GATE to V_{EE} 80mA
V_{DD}, V_{CC} 20mA
NDRV Continuous 25mA
NDRV (Pulsed for less than 1µs) .....±1A
Continuous Power Dissipation (T_A = +70°C)
16-Pin SO (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range
MAX5941_CSE .....0°C to +70°C
MAX5941_ESE .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OPEN, V- tied to OUT, V+ tied to GND, UVLO = V_{EE}, T_A = T_{MIN} to +T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PD INTERFACE							
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V, GND = V- = OUT = V+ (Note 2)				10	µA
Effective Differential Input Resistance	dR	V_{IN} = 1.4V up to 10.1V with 1V step, OUT = $\overline{PGOOD}$ = GND = OUT = V+ (Note 3)		550			kΩ
CLASSIFICATION MODE							
Classification Current Turn-Off Threshold	$V_{TH,CLSS}$	V_{IN} rising (Note 4)		20.8	21.8	22.5	V
Classification Current (Notes 5, 6)	I_{CLASS}	V_{IN} = 12.6V to 20V, R_{DISC} = 25.5kΩ	Class 0, R_{CL} = 10kΩ	0		2	mA
			Class 1, R_{CL} = 732Ω	9.17		11.83	
			Class 2, R_{CL} = 392Ω	17.29		19.71	
			Class 3, R_{CL} = 255Ω	26.45		29.55	
			Class 4, R_{CL} = 178Ω	36.6		41.4	
POWER MODE							
Operating Supply Voltage	V_{IN}	V_{IN} = (GND - V_{EE})				67	V
Operating Supply Current	I_{IN}	Measure at GND, not including R_{DISC}			0.4	1	mA
Default Power Turn-On Voltage	$V_{UVLO, ON}$	V_{IN} increasing, UVLO = V_{EE}		37.4	38.6	40.1	V
Default Power Turn-Off Voltage	$V_{UVLO, OFF}$	V_{IN} decreasing, UVLO = V_{EE}		30			V
Default Power Turn-On/Off Hysteresis	$V_{HYST, UVLO}$			7.4			V
External UVLO Programming Range	$V_{IN,EX}$	Set UVLO externally (Note 7)		12		67	V
UVLO External Reference Voltage	$V_{REF, UVLO}$	V_{UVLO} increasing		2.400	2.460	2.522	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OPEN, V- tied to OUT, V+ tied to GND, UVLO = V_{EE}, T_A = T_{MIN} to +T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UVLO External Reference Voltage Hysteresis	HYST	Ratio to $V_{REF,UVLO}$		19.2	20	20.9	%
UVLO Bias Current	I_{UVLO}	UVLO = 2.460V		-1.5		+1.5	µA
UVLO Input Ground Sense Threshold	$V_{TH,G,UVLO}$	(Note 8)		50		440	mV
UVLO Input Ground Sense Glitch Rejection		UVLO = V_{EE}			7		µs
Power Turn-Off Voltage, Undervoltage Lockout Deglitch Time	t_{OFF_DLY}	V_{IN}, V_{UVLO} falling (Note 9)		0.32			ms
Isolation Switch N-Channel MOSFET On-Resistance	R_{ON}	Output current = 300mA, V_{GATE} = 5.6V, measured between OUT and V_{EE}	T_A = +25°C (Note 11)		0.6	1.1	Ω
			T_A = +85°C		0.8	1.5	
Isolation Switch N-Channel MOSFET Off-Threshold Voltage	V_{GSTH}	OUT = GND, V_{GATE} - V_{EE}, output current < 1µA		0.5			V
GATE Pulldown Switch Resistance	R_G	Power-off mode, V_{IN} = 12V, UVLO = V_{EE}			38	80	Ω
GATE Charging Current	I_G	V_{GATE} = 2V		5	10	15	µA
GATE High Voltage	V_{GATE}	I_{GATE} = 1µA		5.58	5.76	5.93	V
PGOOD, $\overline{PGOOD}$ Assertion V_{OUT} Threshold	V_{OUTEN}	V_{OUT} - V_{EE}, $\lvert V_{OUT} - V_{EE} \rvert$ decreasing, V_{GATE} = 5.75V		1.15	1.23	1.31	V
		Hysteresis			70		mV
PGOOD, $\overline{PGOOD}$ Assertion V_{GATE} Threshold	V_{GSEN}	(GATE - V_{EE}) increasing, OUT = V_{EE}		4.62	4.76	4.91	V
		Hysteresis			80		mV
$\overline{PGOOD}$ Output Low Voltage		I_{SINK} = 2mA (Note 10)				0.4	V
PGOOD Output Low Voltage	V_{OLDCDC}	I_{SINK} = 2mA, OUT ≤ (GND - 5V) (Note 10)				0.2	V
PGOOD Leakage Current		GATE = high, GND - V_{OUT} = 67V (Note 10)				1	µA
$\overline{PGOOD}$ Leakage Current		GATE = V_{EE}, $\overline{PGOOD}$ - V_{EE} = 67V (Note 10)				1	µA

ELECTRICAL CHARACTERISTICS (PWM Controller)

(All voltages referenced to V-. V_{DD} = 13V, a 10µF capacitor connects V_{CC} to V-, V_{CS} = V-, V+ = 48V, 0.1µF capacitor connected to SS_$\overline{SHDN}$, NDRV = open circuit, OPTO = V-, T_A = T_{MIN} to +T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
V+ Supply Current	$I_{V+(NS)}$	V_{DD} = 0V, V+ = 67V, driver not switching		0.85	1.3	mA
	$I_{V+(S)}$	V+ = 67V, V_{DD} = 0V, V_{OPTO} = 4V, driver switching		1.4	2.6	
V+ Supply Current After Startup		V+ = 67V, V_{DD} = 13V, V_{OPTO} = 4V		11		µA
V_{DD} Supply Current	$I_{VDD(NS)}$	V_{DD} = 36V, driver not switching		0.9	1.3	mA
	$I_{VDD(S)}$	V_{DD} = 36V, driver switching, V_{OPTO} = 4V		1.9	2.7	

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ELECTRICAL CHARACTERISTICS (PWM Controller) (continued)

(All voltages referenced to V-. V_{DD} = 13V, a 10µF capacitor connects V_{CC} to V-, V_{CS} = V-, V+ = 48V, 0.1µF capacitor connected to SS_$\overline{SHDN}$, NDRV = open circuit, OPTO = V-, T_A = T_{MIN} to +T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Shutdown Current		$V_{SS_\overline{SHDN}}$ = 0V, V+ = 67V		190	290	µA
V_{DD} Shutdown Current		$V_{SS_\overline{SHDN}}$ = 0V		8	20	µA
PREREGULATORS/STARTUP						
V+ Input Voltage			18		67	V
V_{DD} Supply Voltage			13		36	V
INTERNAL REGULATORS						
V_{CC} Output Voltage		Powered from V+, I_{CC} = 7.5mA, V_{DD} = 0V	7.5	9.8	12	V
		Powered from V_{DD}, I_{CC} = 7.5mA	9.0	10.0	11.0	
V_{CC} Undervoltage Lockout	V_{CC_UVLO}	V_{CC} falling		6.6		V
OUTPUT DRIVER						
Peak Source Current		V_{CC} = 11V (externally forced)		570		mA
Peak Sink Current		V_{CC} = 11V (externally forced)		1000		mA
NDRV High-Side Driver Resistance	R_{OH}	V_{CC} = 11V, externally forced, NDRV sourcing 50mA		4	12	Ω
NDRV Low-Side Driver Resistance	R_{OL}	V_{CC} = 11V, externally forced, NDRV sinking 50mA		1.6	4	Ω
PWM COMPARATOR						
OPTO Input Bias Current		V_{OPTO} = $V_{SS_\overline{SHDN}}$	-1.00		+1.00	µA
OPTO Control Range			2		3	V
Slope Compensation	V_{SCOMP}	MAX5941A		26		mV/µs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature				150		°C
Thermal Hysteresis				25		°C
CURRENT LIMIT						
CS Threshold Voltage	V_{ILIM}	V_{OPTO} = 4V	419	465	510	mV
CS Input Bias Current		0V ≤ V_{CS} ≤ 2V, V_{OPTO} = 4V	-1		+1	µA
Current-Limit Comparator Propagation Delay		25mV overdrive on CS, V_{OPTO} = 4V		180		ns
CS Blanking Time		V_{OPTO} = 4V		70		ns
OSCILLATOR						
Clock Frequency Range		V_{OPTO} = 4V	235	275	314	kHz
Max Duty Cycle		MAX5941A, V_{OPTO} = 4V	75		85	%
		MAX5941B, V_{OPTO} = 4V	44		50	
SOFT-START						
SS Source Current	I_{SSO}	$V_{SS(\overline{SHDN})}$ = 0V	2.0	4.6	6.5	µA
SS Sink Current			1			mA
Peak Soft-Start Voltage Clamp		No external load	2.331	2.420	2.500	V
Shutdown Threshold		$V_{SS_\overline{SHDN}}$ falling (Note 11)	0.25	0.37	0.41	V
		$V_{SS_\overline{SHDN}}$ rising (Note 11)	0.53	0.59	0.65	

Note 1: All min/max limits for the PD interface are production tested at +85°C (extended grade)/+70°C (commercial grade). Limits at +25°C and -40°C are guaranteed by design. All PWM controller min/max limits are 100% production tested at +25°C and +85°C (extended grade)/+70°C (commercial grade). Limits at -40°C are guaranteed by design, unless otherwise noted.

Note 2: The input offset current is illustrated in Figure 1.

Note 3: Effective differential input resistance is defined as the differential resistance between GND and V_{EE} without any external resistance.

Note 4: Classification current is turned off whenever the IC is in power mode.

Note 5: See Table 2 in the *PD Classification Mode* section. R_{DISC} and R_{CL} must be 100ppm or better.

Note 6: See *Thermal Dissipation section* for details.

Note 7: When UVLO is connected to the midpoint of an external resistor-divider with a series resistance of 25.5kΩ (±1%), the turn-on threshold set point for the power mode is defined by the external resistor-divider. Make sure the voltage on the UVLO pin does not exceed its maximum rating of 8V when V_{IN} is at the maximum voltage.

Note 8: When the V_{UVLO} is below $V_{TH, G, UVLO,}$ the MAX5941 sets the turn-on voltage threshold internally ($V_{UVLO,ON}$).

Note 9: An input voltage or V_{UVLO} glitch below their respective thresholds shorter than or equal to t_{OFF_DLY} does not cause the MAX5941A/MAX5941B to exit power-on mode (as long as the input voltage remains above an operable voltage level of 12V).

Note 10: PGOOD references to OUT while $\overline{PGOOD}$ references to V_{EE}.

Note 11: Guaranteed by design.

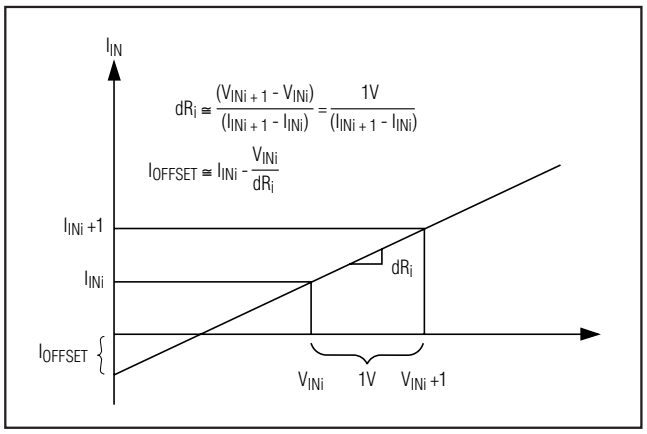

Figure 1. Effective Differential Input Resistance/Offset Current

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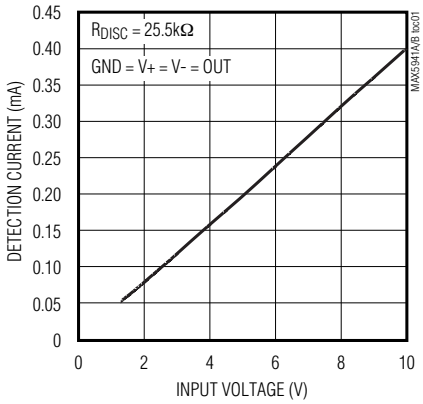
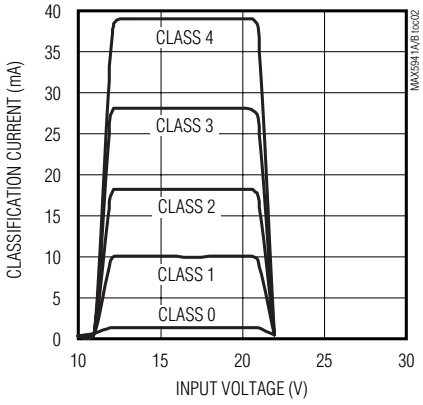
Typical Operating Characteristics

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OUT = OPEN, UVLO = V_{EE}, V_{DD} = 13V, NDRV floating, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE} (for graphs 1–11 in the *Typical Operating Characteristics*), all voltages are referenced to V- (for graphs 12–30 in the *Typical Operating Characteristics*), unless otherwise noted.)

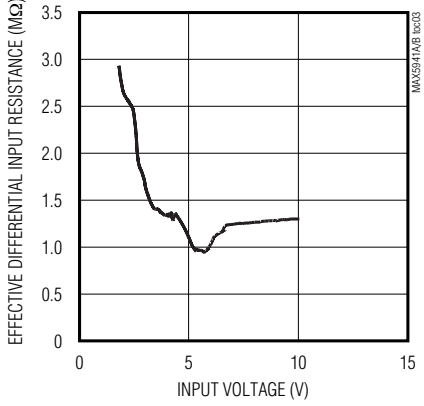
DETECTION CURRENT vs. INPUT VOLTAGE



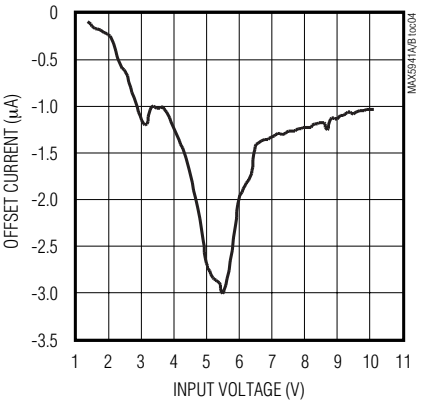
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



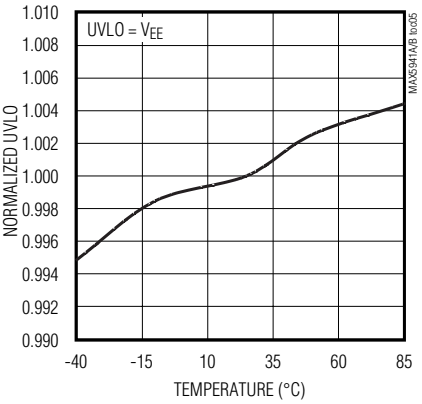
EFFECTIVE DIFFERENTIAL INPUT RESISTANCE vs. INPUT VOLTAGE



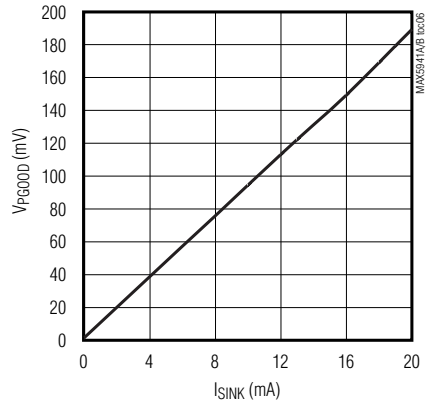
OFFSET CURRENT vs. INPUT VOLTAGE



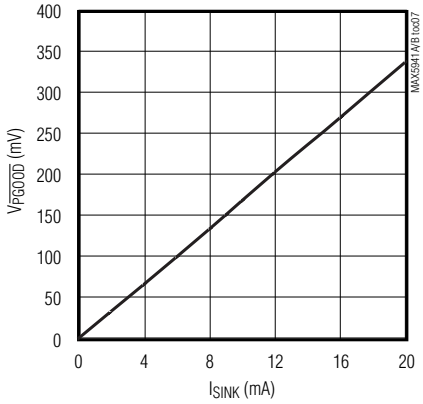
NORMALIZED UVLO vs. TEMPERATURE



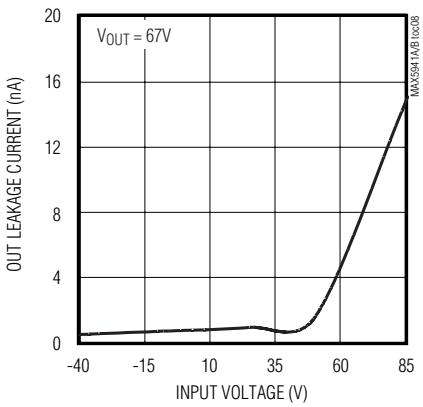
PGOOD OUTPUT LOW VOLTAGE vs. CURRENT



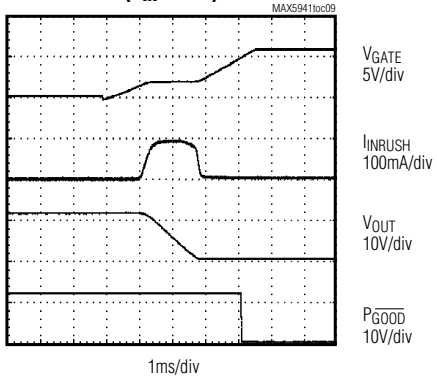
$\overline{PGOOD}$ OUTPUT LOW VOLTAGE vs. CURRENT



OUT LEAKAGE CURRENT vs. TEMPERATURE



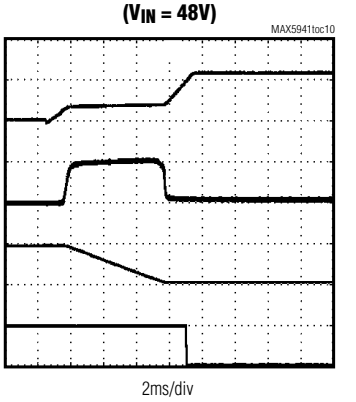
INRUSH CURRENT CONTROL (V_{IN} = 12V)



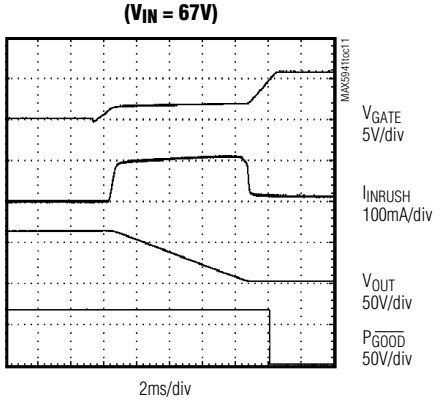
Typical Operating Characteristics (continued)

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OUT = OPEN, UVLO = V_{EE}, V_{DD} = 13V, NDRV floating, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE} (for graphs 1–11 in the *Typical Operating Characteristics*), all voltages are referenced to V- (for graphs 12–30 in the *Typical Operating Characteristics*), unless otherwise noted.)

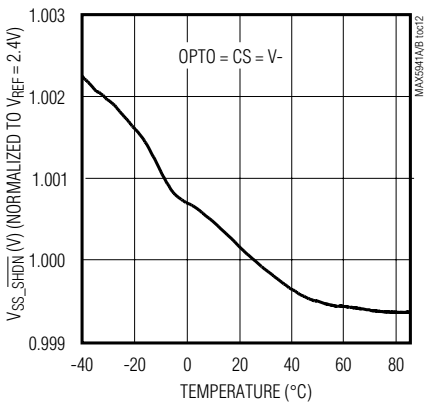
INRUSH CURRENT CONTROL (V_{IN} = 48V)



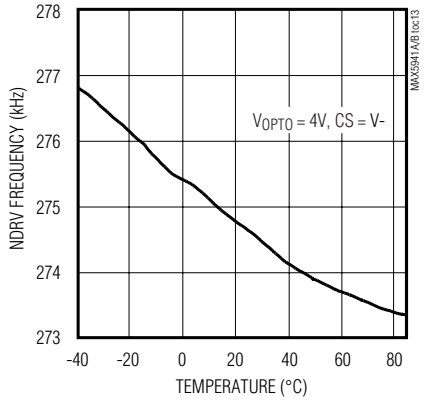
INRUSH CURRENT CONTROL (V_{IN} = 67V)



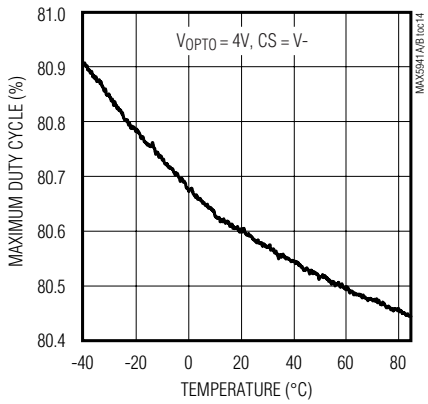
$V_{SS_\overline{SHDN}}$ vs. TEMPERATURE (AT THE END OF SOFT-START)



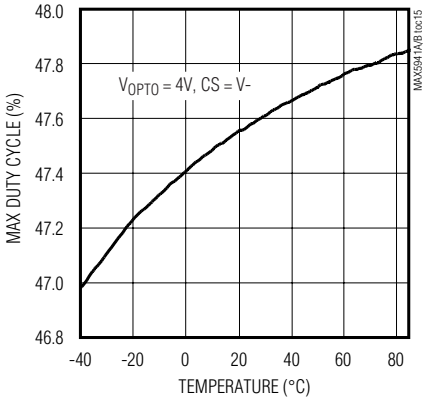
NDRV FREQUENCY vs. TEMPERATURE



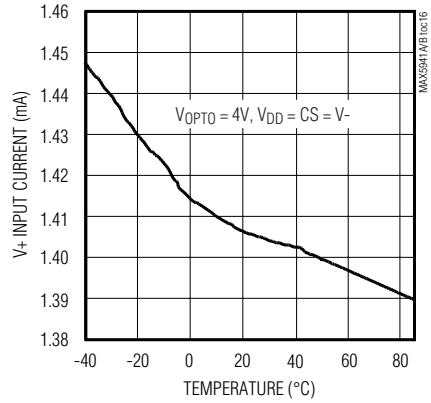
MAXIMUM DUTY CYCLE vs. TEMPERATURE



MAXIMUM DUTY CYCLE vs. TEMPERATURE



V+ SUPPLY CURRENT vs. TEMPERATURE

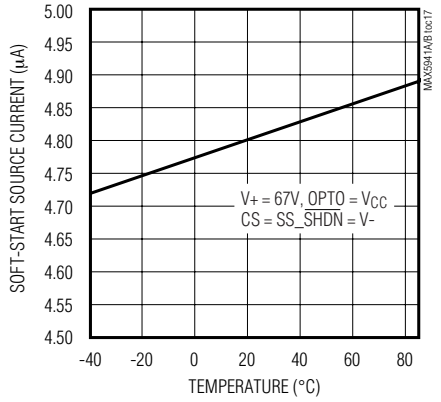


IEEE 802.3af-Compliant Power-Over-Ethernet Interface/PWM Controller for Power Devices

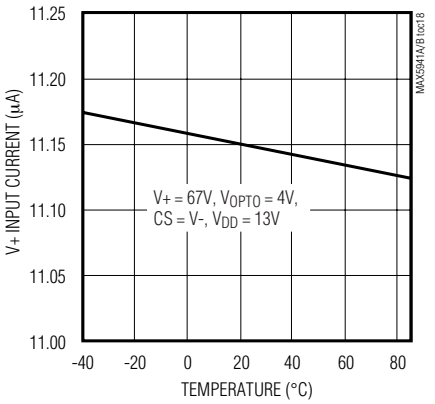
Typical Operating Characteristics (continued)

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OUT = OPEN, UVLO = V_{EE}, V_{DD} = 13V, NDRV floating, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE} (for graphs 1–11 in the *Typical Operating Characteristics*), all voltages are referenced to V- (for graphs 12–30 in the *Typical Operating Characteristics*), unless otherwise noted.)

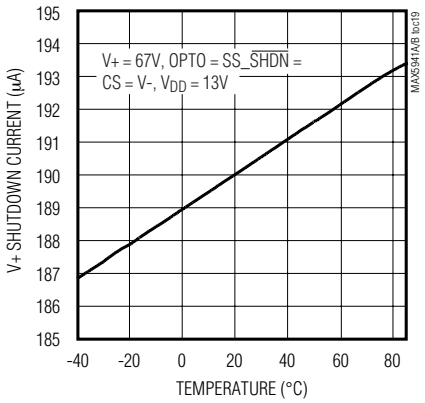
SOFT-START SOURCE CURRENT vs. TEMPERATURE



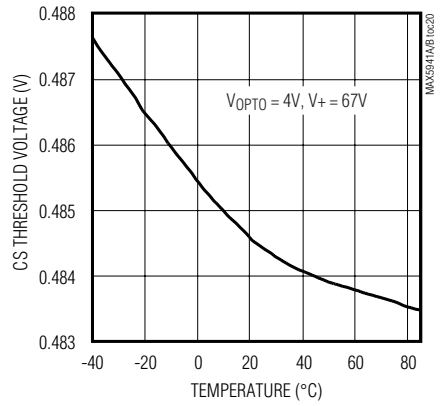
V+ INPUT CURRENT vs. TEMPERATURE (AFTER STARTUP)



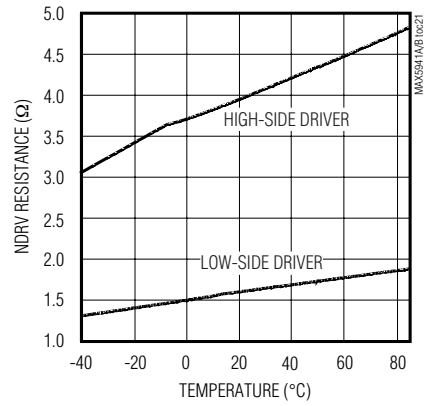
V+ SHUTDOWN CURRENT vs. TEMPERATURE



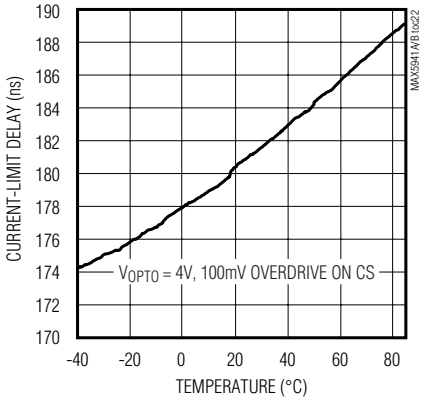
CS THRESHOLD VOLTAGE vs. TEMPERATURE



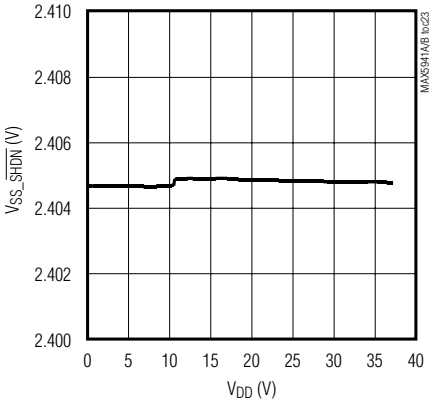
NDRV RESISTANCE vs. TEMPERATURE



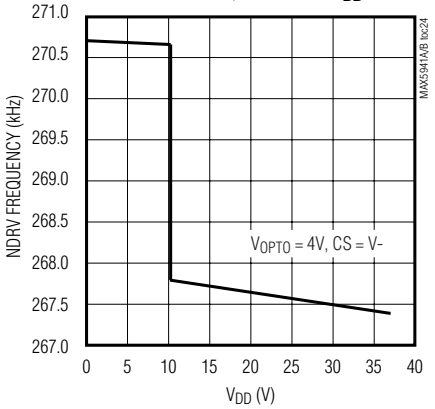
CURRENT-LIMIT DELAY vs. TEMPERATURE



$V_{SS_\overline{SHDN}}$ vs. V_{DD}



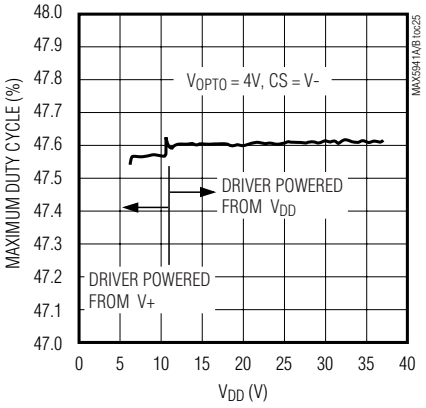
NDRV FREQUENCY vs. V_{DD}



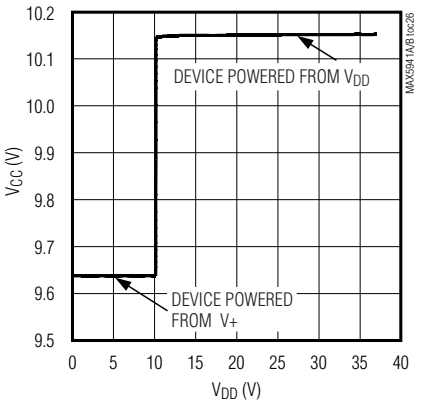
Typical Operating Characteristics (continued)

(V_{IN} = (GND - V_{EE}) = 48V, GATE = $\overline{PGOOD}$ = PGOOD = OUT = OPEN, UVLO = V_{EE}, V_{DD} = 13V, NDRV floating, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C. All voltages are referenced to V_{EE} (for graphs 1–11 in the *Typical Operating Characteristics*), all voltages are referenced to V- (for graphs 12–30 in the *Typical Operating Characteristics*), unless otherwise noted.)

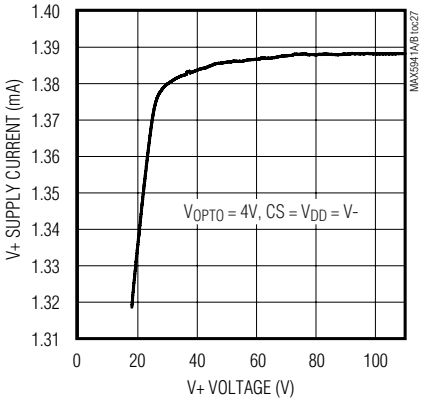
MAXIMUM DUTY CYCLE vs. V_{DD}



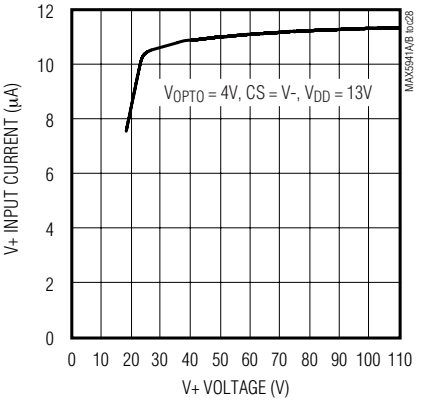
V_{CC} vs. V_{DD}



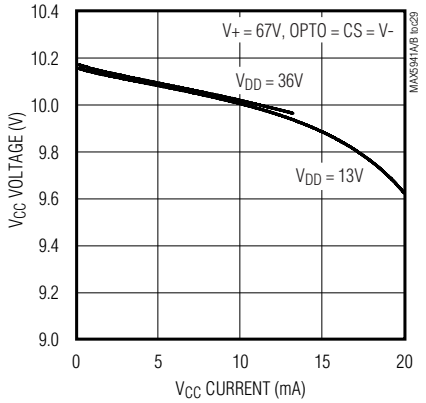
V+ SUPPLY CURRENT vs. V+ VOLTAGE



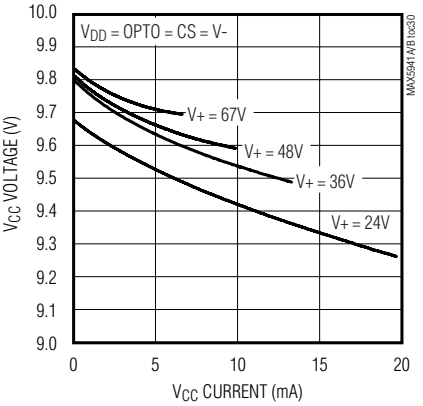
V+ INPUT CURRENT vs. VOLTAGE (AFTER STARTUP)



V_{CC} VOLTAGE vs. V_{CC} CURRENT



V_{CC} VOLTAGE vs. V_{CC} CURRENT



IEEE 802.3af-Compliant Power-Over-Ethernet Interface/PWM Controller for Power Devices

Pin Description

PIN	NAME	FUNCTION
1	V+	High-Voltage Startup Input. Referenced to V-. Connect directly to an input voltage range between 18V to 67V. Connects internally to a high-voltage linear regulator that generates V_{CC} during startup. Tie V+ to GND.
2	V_{DD}	Line Regulator Input. Referenced to V-. V_{DD} is the input to the linear regulator that generates V_{CC}. For supply voltages less than 36V, connect V_{DD} and V+ to the supply. For supply voltages greater than 36V, V_{DD} receives its power from the tertiary winding of the transformer and accepts voltages from 13V to 36V. Bypass V_{DD} to V- with a 4.7µF capacitor.
3	OPTO	Optocoupler Input. Referenced to V-. The control voltage range on this input is 2V to 3V.
4	SS_$\overline{SHDN}$	Soft-Start Timing Capacitor Connection. Referenced to V-. Ramp time to full current limit is approximately 0.45ms/nF. Bypass with a minimum 10nF capacitor to V-. A 2.4V reference voltage appears across the capacitor. Disable the PWM controller by pulling SS_$\overline{SHDN}$ below 0.25V. Tie to PGOOD to enable PWM controller automatically from the PD interface.
5	UVLO	Undervoltage Lockout Programming Input for Power Mode. Referenced to V_{EE}. When UVLO is above its threshold, the device enters the power mode. Connect UVLO to V_{EE} to use the default undervoltage lockout threshold. Connect UVLO to an external resistor-divider to define a threshold externally. The series resistance value of the external resistors must add to 25.5kΩ (±1%) and replaces the detection resistor. To keep the device in undervoltage lockout, pull UVLO between $V_{TH,G,UVLO}$ and $V_{REF,UVLO}$.
6	RCL	Classification Setting. Referenced to V_{EE}. Add a resistor from RCL to V_{EE} to set a PD class (see Tables 1 and 2).
7	GATE	Gate of Internal N-Channel Power MOSFET. Referenced to V_{EE} . GATE sources 10µA when the device enters the power mode. Connect an external 100V ceramic capacitor from GATE to V_{OUT} to program the inrush current. Pull GATE to V_{EE} to turn off the internal MOSFET. The detection and classification functions operate normally when GATE is pulled to V_{EE}.
8	V_{EE}	Negative Input Power. Source of the integrated isolation N-channel power MOSFET. Connect V_{EE} to -48V.
9	OUT	Output Voltage. Referenced to V_{EE}. Drain of the integrated isolation N-channel power MOSFET. Connect OUT to V-.
10	PGOOD	Power-Good Indicator Output, Active High, Open Drain. PGOOD is referenced to OUT. PGOOD goes high impedance when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, PGOOD is pulled to OUT (given that V_{OUT} is at least 5V below GND). Connect PGOOD directly (no external pullup required) to SS_$\overline{SHDN}$ to enable/disable the PWM controller.
11	$\overline{PGOOD}$	Power-Good Indicator Output, Active Low, Open Drain. $\overline{PGOOD}$ is referenced to V_{EE}. $\overline{PGOOD}$ is pulled to V_{EE} when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, $\overline{PGOOD}$ goes high impedance.
12	GND	Ground. Referenced to V_{EE}. GND is the positive input power. Connect to V+.
13	CS	Current-Sense Input. Referenced to V-. Turns power switch off if V_{CS} rises above 465mV for cycle-by-cycle current limiting. CS is also the feedback for the current-mode controller. CS connects to the PWM controller through a leading-edge blanking circuit.
14	V-	V- is the ground terminal of the PWM Controller. Connect to OUT.
15	NDRV	Gate Drive. Referenced to V-. Drives a high-voltage external N-channel power MOSFET.
16	V_{CC}	Regulated IC Supply. Referenced to V-. Provides power for MAX5941_. V_{CC} is regulated from V_{DD} during normal operation and from V+ during startup. Bypass V_{CC} with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor to V-.

Table 1. PD Power Classification/R_{CL} Selection

CLASS	USAGE	R_{CL} (Ω)	MAXIMUM POWER USED BY PD (W)
0	Default	10k	0.44 to 12.95
1	Optional	732	0.44 to 3.84
2	Optional	392	3.84 to 6.49
3	Optional	255	6.49 to 12.95
4	Not allowed	178	Reserved*

**Class 4 reserved for future use.*

Detailed Description

The MAX5941A/MAX5941B integrate a complete power IC for powered devices (PDs) in a power-over-ethernet (PoE) system. The MAX5941A/MAX5941B provide PD interface and a compact DC-DC PWM controller suitable for flyback and forward converters in either isolated or nonisolated designs.

The MAX5941A/MAX5941B powered device (PD) interface complies with the IEEE 802.3af standard, providing the PD with a detection signature, a classification signature, and an integrated isolation switch with programmable inrush current control. These devices also feature power-mode undervoltage lockout (UVLO) with wide hysteresis, and power-good status outputs.

An integrated MOSFET provides PD isolation during detection and classification. The MAX5941A/MAX5941B guarantee a leakage current offset of less than 10µA during the detection phase. A programmable current limit prevents high inrush current during power-on. The devices feature power-mode UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to ensure glitch-free transition between detection, classification, and power-on/off phases. The MAX5941A/MAX5941B provide both active-high (PGOOD) and active-low ($\overline{PGOOD}$) outputs. Both devices offer an adjustable UVLO threshold with a default value compliant to the IEEE 802.3af standard. The MAX5941A/MAX5941B are designed to work with or without an external diode bridge in front of the PD.

Use the MAX5941A/MAX5941B PWM current-mode controllers to design flyback- or forward-mode power supplies. Current-mode operation simplifies control-loop design while enhancing loop stability. An internal high-voltage startup regulator allows the device to connect directly to the input supply without an external startup resistor. Current from the internal regulator starts the controller. Once the tertiary winding voltage is established, the internal regulator is switched off and bias current for running the PWM controller is derived from the tertiary winding. The internal oscillator is set to 275kHz and trimmed to ±10%. This permits the use of small magnetic components to minimize board space. Both the MAX5941A and MAX5941B can be used in power supplies providing multiple output voltages. A functional diagram of the PWM controller is shown in Figure 4. Typical applications circuits for forward and flyback topologies are shown in Figure 5 and Figure 6, respectively.

Powered Device Interface

Operating Modes

The powered device (PD) front-end section of the MAX5941A/MAX5941B operates in three different modes: PD detection signature, PD classification, and PD power, depending on its input voltage (V_{IN} = GND - V_{EE}). All voltage thresholds are designed to operate with or without the optional diode bridge while still complying with the IEEE 802.3af standard (see Application Circuit 1).

Detection Mode ($1.4V \le V_{IN} \le 10.1V$)

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum), and then records the current measurements at the two points. The PSE then computes $\Delta V/\Delta I$ to ensure the presence of the 25.5kΩ signature resistor. In this mode, most of the MAX5941A/MAX5941B internal circuitry is off and the offset current is less than 10µA.

If the voltage applied to the PD is reversed, install protection diodes on the input terminal to prevent internal damage to the MAX5941A/MAX5941B (see Figure 7). Since the PSE uses a slope technique ($\Delta V/\Delta I$) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode ($12.6V \le V_{IN} \le 20V$)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. The IEEE 802.3af standard defines five different classes as shown in Table 1. An external resistor (R_{CL}) connected from RCL to V_{EE} sets the classification current.

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Table 2. Setting Classification Current

CLASS	R_{CL} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af PD CLASSIFICATION CURRENT SPECIFICATION (mA)	
			MIN	MAX	MIN	MAX
0	10k	12.6 to 20	0	4	0	4
1	732	12.6 to 20	9	12	9	12
2	392	12.6 to 20	17	20	17	20
3	255	12.6 to 20	26	30	26	30
4	178	12.6 to 20	36	42	36	44

**V_{IN} is measured across the MAX5941 input pins (V_{EE} and GND), which does not include the diode bridge voltage drop.*

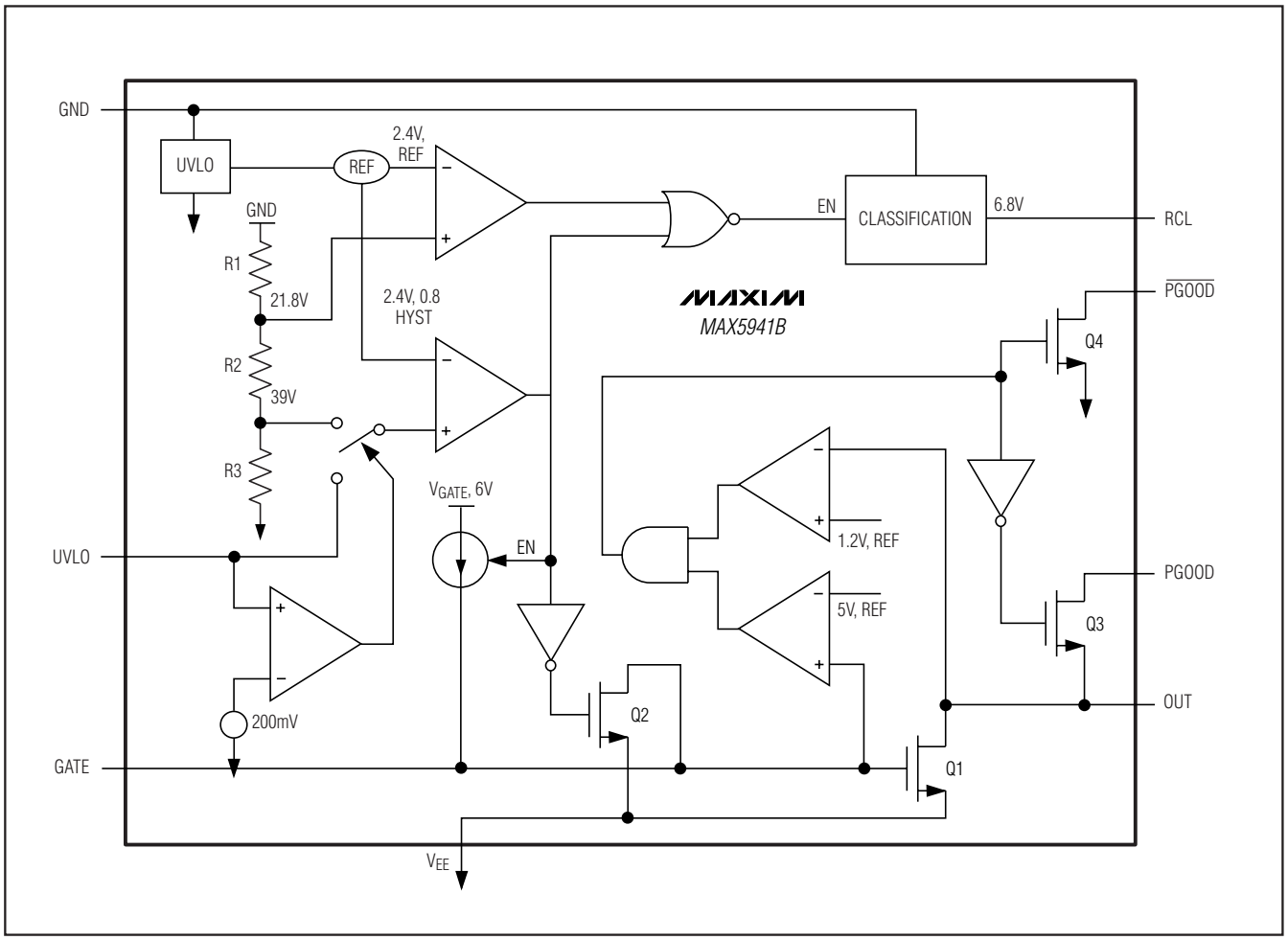

Figure 2. Powered Device Interface Block Diagram

The PSE determines the class of a PD by applying a voltage at the PD input and measures the current sourced out of the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5941A/MAX5941B exhibit a current characteristic with values indicated in Table 2. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by the 25.5kΩ detection signature resistor and the supply current of the MAX5941A/MAX5941B so that the total current drawn by the PD is within the IEEE 802.3af standard figures. The classification current is turned off whenever the device is in power mode.

Power Mode

During power mode, when V_{IN} rises above the undervoltage lockout threshold ($V_{UVLO,ON}$), the MAX5941A/ MAX5941B gradually turn on the internal N-channel MOSFET Q1 (see Figure 2). The MAX5941A/ MAX5941B charge the gate of Q1 with a constant current source (10µA, typ). The drain-to-gate capacitance of Q1 limits the voltage rise rate at the drain of MOSFET, thereby limiting the inrush current. To reduce the inrush current, add external drain-to-gate capacitance (see the *Inrush Current* section). When the drain of Q1 is within 1.2V of its source voltage and its gate-to-source voltage is above 5V, the MAX5941A/MAX5941B assert the PGOOD/$\overline{PGOOD}$ outputs. The MAX5941A/MAX5941B have a wide UVLO hysteresis and turn-off deglitch time to compensate for the high impedance of the twisted-pair cable.

Undervoltage Lockout

The MAX5941A/MAX5941B operate up to a 67V supply voltage with a default UVLO turn-on set at 39V and a UVLO turn-off set at 30V. Adjust the UVLO threshold using a resistor-divider connected to UVLO (see Figure 3). When the input voltage is above the UVLO threshold ($V_{UVLO,ON}$), the IC is in power mode and the MOSFET is on. When the input voltage goes below the UVLO threshold ($V_{UVLO,OFF}$) for more than t_{OFF_DLY}, the MOSFET turns off.

To adjust the UVLO threshold, connect an external resistor-divider from GND to UVLO and from UVLO to V_{EE}. Use the following equations to calculate R1 and R2 for a desired UVLO threshold:

$$R2 = 25.5k\Omega \times \frac{V_{REF,UVLO}}{V_{IN,EX}}$$

$$R1 = 25.5k\Omega - R2$$

where $V_{IN,EX}$ is the desired UVLO threshold. Since the resistor-divider replaces the 25.5kΩ PD detection resistor, ensure that the sum of R1 and R2 equals 25.5kΩ ±1%. When using the external resistor-divider, the MAX5941 has an external reference voltage hysteresis of 20% (typ). In other words, when UVLO is programmed externally, the turn-off threshold is 80% (typ) of the new UVLO turn-on threshold.

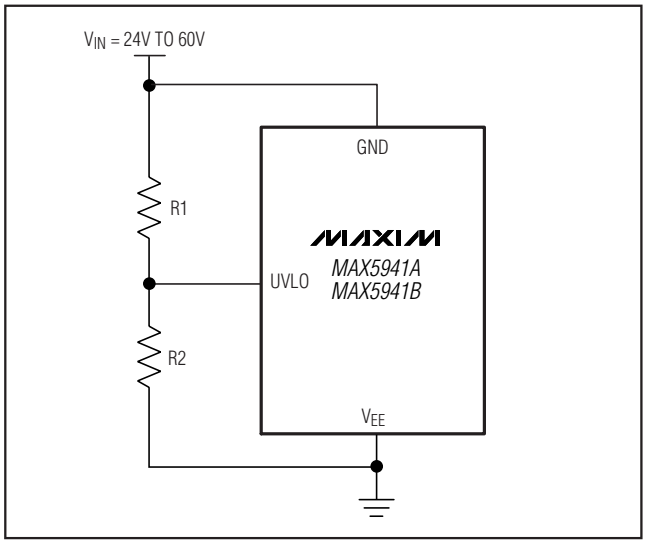

Figure 3. Setting Undervoltage Lockout with an External Resistor-Divider

Inrush Current Limit

The MAX5941A/MAX5941B charge the gate of the internal MOSFET with a constant current source (10µA, typ). The drain-to-gate capacitance of the MOSFET limits the voltage rise rate at the drain, thereby limiting the inrush current. Add an external capacitor from GATE to OUT to further reduce the inrush current. Use the following equation to calculate the inrush current:

$$I_{INRUSH} = I_G \times \frac{C_{OUT}}{C_{GATE}}$$

The recommended inrush current for a PoE application is 100mA.

PGOOD/$\overline{PGOOD}$ Outputs

PGOOD is an open-drain, active-high logic output. PGOOD goes high impedance when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, PGOOD is pulled to V_{OUT} (given that V_{OUT} is at least 5V below GND). Connect PGOOD to SS_$\overline{SHDN}$ to enable the PWM controller. No external pullup resistor is required.

$\overline{PGOOD}$ is an open-drain, active-low logic output. $\overline{PGOOD}$ is pulled to V_{EE} when V_{OUT} is within 1.2V of V_{EE} and when GATE is 5V above V_{EE}. Otherwise, $\overline{PGOOD}$ goes high impedance.

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Thermal Dissipation

During classification mode, if the PSE applies the maximum DC voltage, the maximum voltage drop from GND to V_{RCL} will be 13V. If the maximum classification current of 42mA flows through the MAX5941A/MAX5941B, then the maximum DC power dissipation will be close to 546mW, which is slightly higher than the maximum DC power dissipation of the IC at maximum operating temperature. However, according to the IEEE 802.3af standard, the duration of the classification mode is limited to 75ms (max). The MAX5941A/MAX5941B handles the maximum classification power dissipation for the maximum duration time without sustaining any internal damage. If the PSE violates the IEEE 802.3af standard by exceeding the 75ms maximum classification duration, it may cause internal damage to the IC.

PWM Controller

Current-Mode Control

The MAX5941A/MAX5941B offer current-mode control operation with added features such as leading-edge blanking with dual internal path that only blanks the sensed current signal applied to the input of the PWM comparator. The current-limit comparator monitors the CS pin at all times and provides cycle-by-cycle current limit without being blanked. The leading-edge blanking of the CS signal prevents the PWM comparator from prematurely terminating the on cycle. The CS signal contains a leading-edge spike that is the result of the MOSFET gate charge current, capacitive and diode reverse recovery current of the power circuit. Since this leading-edge spike is normally lower than the current limit comparator threshold, current limiting is not blanked and cycle-by-cycle current limiting is provided under all conditions.

Use the MAX5941A in discontinuous flyback applications where wide line voltage and load current variation is expected. Use the MAX5941B for single transistor forward converters where the maximum duty cycle must be limited to less than 50%.

Under certain conditions, it may be advantageous to use a forward converter with greater than 50% duty cycle. For those cases, use the MAX5941A. The large duty cycle results in much lower operating primary RMS currents through the MOSFET switch and in most cases a smaller output filter inductor. The major disadvantage to this is that the MOSFET voltage rating must be higher and that slope compensation must be provided to stabilize the inner current loop. The MAX5941A provides internal slope compensation.

Optocoupled Feedback

Isolated voltage feedback is achieved by using an optocoupler and a shunt regulator as shown in Figure 5. The output voltage set-point accuracy is a function of the accuracy of the shunt regulator and feedback resistor-divider tolerance.

Internal Regulators

The internal regulators of the MAX5941A/MAX5941B enable initial startup without a lossy startup resistor and regulate the voltage at the output of a tertiary (bias) winding to provide power for the IC. At startup, V+ is regulated down to V_{CC} to provide bias for the device. The V_{DD} regulator then regulates from the output of the tertiary winding to V_{CC}. This architecture allows the tertiary winding to have only a small filter capacitor at its output thus eliminating the additional cost of a filter inductor.

When designing the tertiary winding, calculate the number of turns so the minimum reflected voltage is always higher than 12.7V. The maximum reflected voltage must be less than 36V.

To reduce power dissipation, the high-voltage regulator is disabled when the V_{DD} voltage reaches 12.7V. This greatly reduces power dissipation and improves efficiency. If V_{CC} falls below the undervoltage lockout threshold (V_{CC} = 6.6V), the low-voltage regulator is disabled, and soft-start is reinitiated. In undervoltage lockout the MOSFET driver output (NDRV) is held low.

If the input voltage range is between 13V and 36V, V+ and V_{DD} may be connected to the line voltage provided that the maximum power dissipation is not exceeded. This eliminates the need for a tertiary winding.

PWM Controller Undervoltage Lockout, Soft-Start, and Shutdown

The soft-start feature of the MAX5941A/MAX5941B allows the load voltage to ramp up in a controlled manner, thus eliminating output voltage overshoot.

While the controller is in undervoltage lockout, the capacitor connected to the SS_$\overline{SHDN}$ pin is discharged. Upon coming out of undervoltage lockout, an internal current source starts charging the capacitor to initiate the soft-start cycle. Use the following equation to calculate total soft-start time:

$$t_{startup} = 0.45\frac{ms}{nF} \times C_{SS}$$

where C_{SS} is the soft-start capacitor as shown in Figure 5.

Operation begins when $V_{SS_\overline{SHDN}}$ ramps above 0.6V. When soft-start has completed, $V_{SS_\overline{SHDN}}$ is regulated

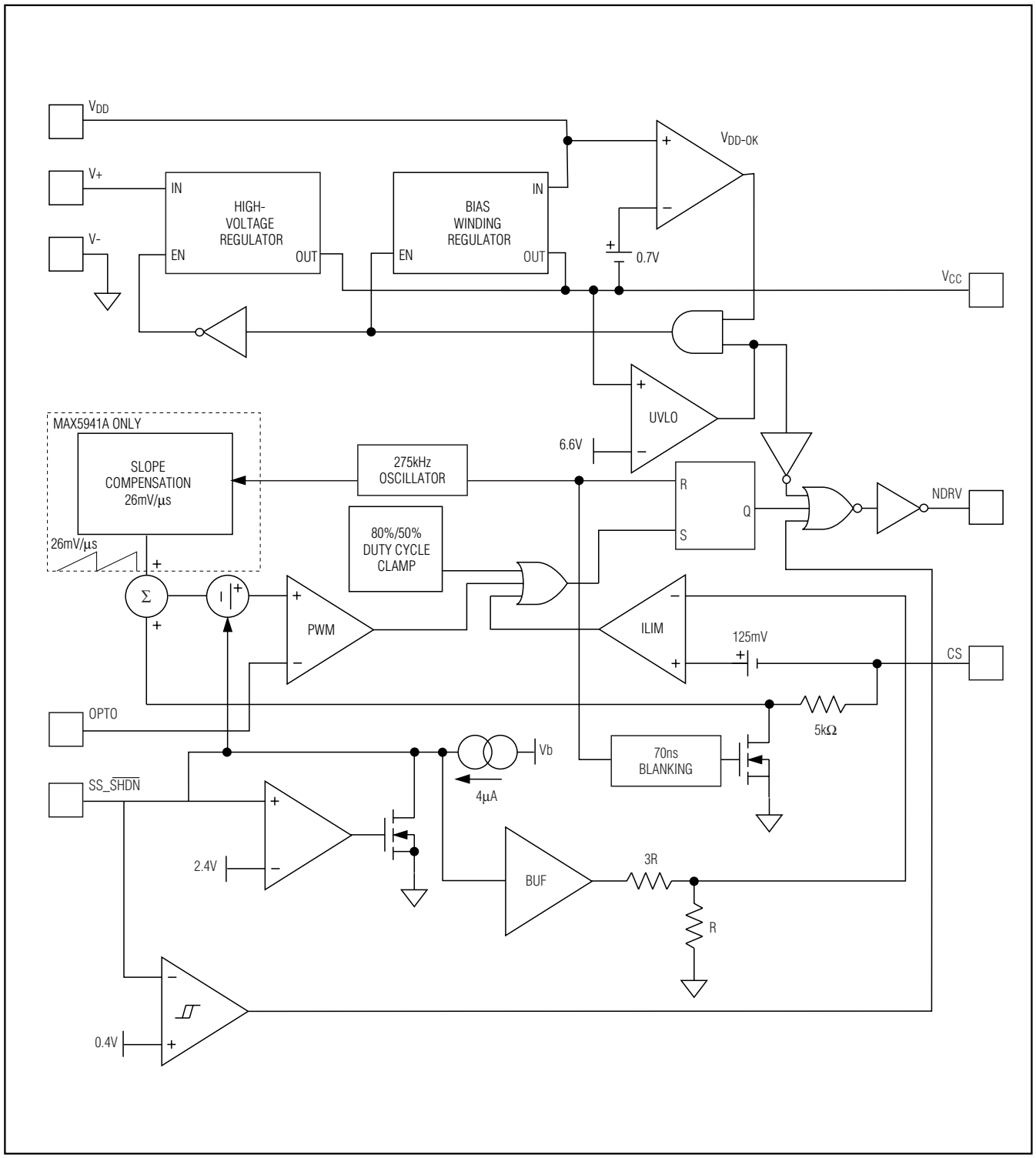

Figure 4. MAX5941A/MAX5941B PWM Controller Functional Diagram

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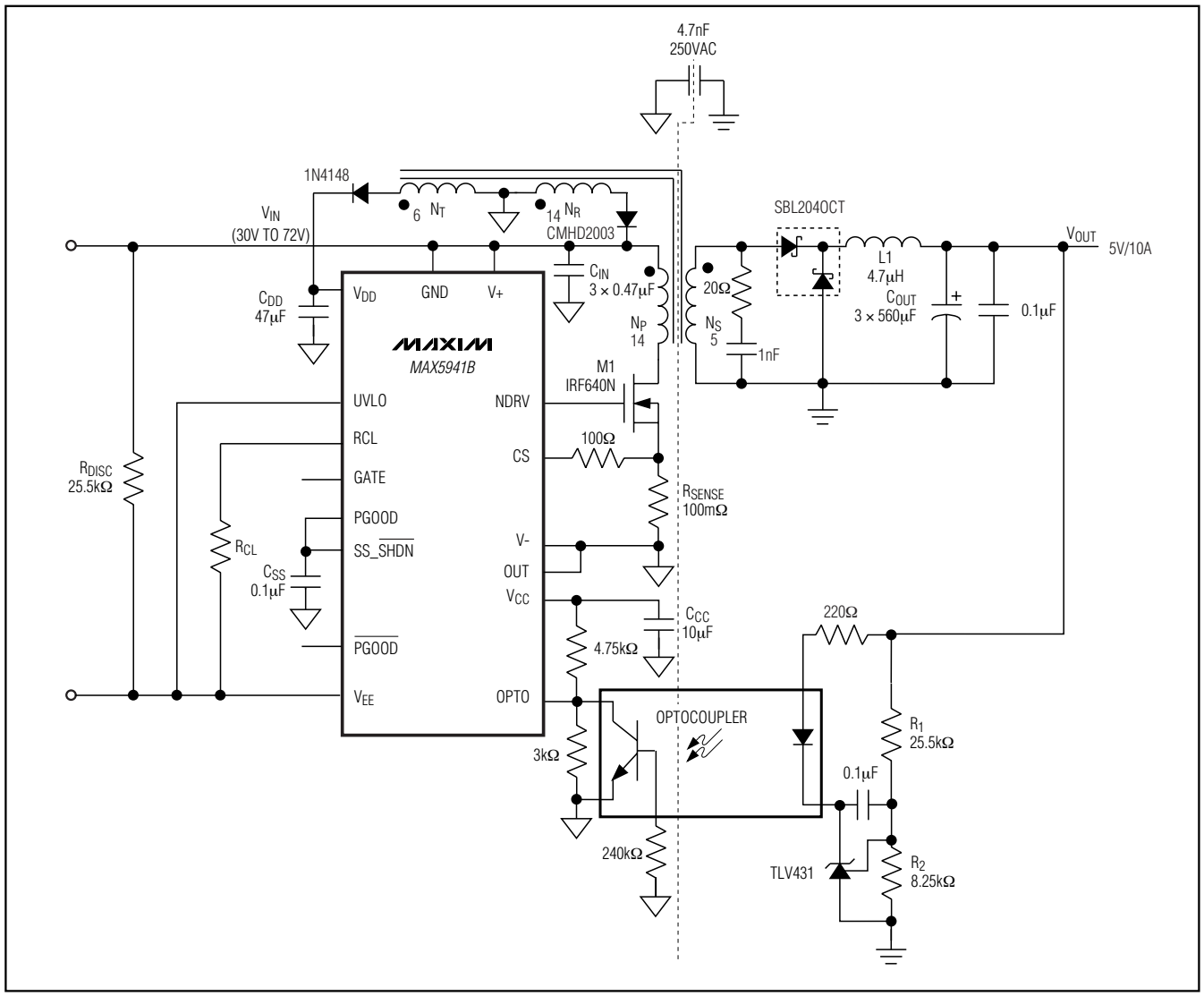

Figure 5. Forward Converter

to 2.4V, the internal voltage reference. Pull $V_{SS_\overline{SHDN}}$ below 0.25V to disable the controller.

Undervoltage lockout shuts down the controller when V_{CC} is less than 6.6V. The regulators for V+ and the reference remain on during shutdown.

Current-Sense Comparator

The current-sense (CS) comparator and its associated logic limit the peak current through the MOSFET. Current is sensed at CS as a voltage across a sense resistor between the source of the MOSFET and GND. To reduce switching noise, connect CS to the external MOSFET source through a 100Ω resistor or an RC low-pass filter (Figures 5, 6). Select the current-sense resistor, R_{SENSE}, according to the following equation:

$$R_{SENSE} = 0.465V / I_{LimPrimary}$$

where $I_{LimPrimary}$ is the maximum peak primary-side current.

When V_{CS} > 465mV, the power MOSFET switches off. The propagation delay from the time the switch current reaches the trip level to the driver turn-off time is 170ns.

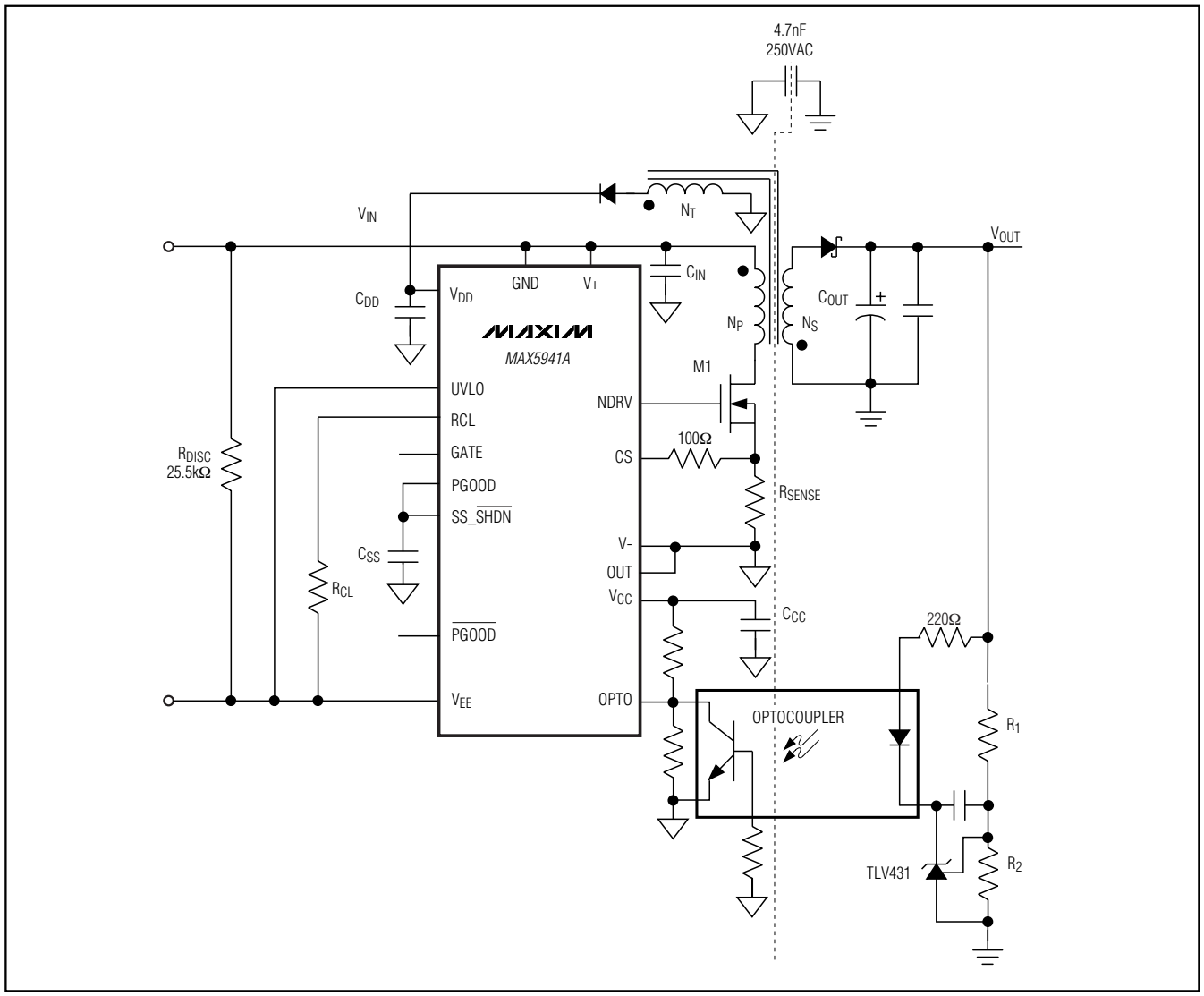

Figure 6. Flyback Converter

PWM Comparator and Slope Compensation

An internal 275kHz oscillator determines the switching frequency of the controller. At the beginning of each cycle, NDRV switches the N-channel MOSFET on. NDRV switches the external MOSFET off after the maximum duty cycle has been reached, regardless of the feedback.

The MAX5941B uses an internal ramp generator for slope compensation. The internal ramp signal is reset at the beginning of each cycle and slews at 26mV/µs.

The PWM comparator uses the instantaneous current, the error voltage, the internal reference, and the slope compensation (MAX5941A only) to determine when to switch the N-channel MOSFET off. In normal operation, the N-channel MOSFET turns off when:

$$I_{PRIMARY} \times R_{SENSE} > V_{OPTO} - V_{REF} - V_{SCOMP}$$

where $I_{PRIMARY}$ is the current through the N-channel MOSFET, V_{REF} is the 2.4V internal reference, and V_{SCOMP} is a ramp function starting at zero and slewing at 26mV/µs (MAX5941A only). When using the MAX5941A in a forward-converter configuration, the following condition must be met to avoid control-loop subharmonic oscillations:

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$$\frac{N_S}{N_P} \times \frac{k \times R_{SENSE} \times V_{OUT}}{L} = 26mV/\mu s$$

where k = 0.75 to 1, and N_S and N_P are the number of turns on the secondary and primary side of the transformer, respectively. L is the output filter inductor. This makes the output inductor current downslope as referenced across R_{SENSE} equal to the slope compensation. The controller responds to transients within one cycle when this condition is met.

N-Channel MOSFET Gate Driver

NDRV drives an N-channel MOSFET. NDRV sources and sinks large transient currents to charge and discharge the MOSFET gate. To support such switching transients, bypass V_{CC} with a ceramic capacitor. The average current as a result of switching the MOSFET is the product of the total gate charge and the operating frequency. It is this current plus the DC quiescent current that determines the total operating current.

Applications Information

Design Example

The following is a general procedure for designing a forward converter (Figure 5) using the MAX5941B:

1) Determine the requirements.
2) Set the output voltage.
3) Calculate the transformer primary to secondary winding turns ratio.
4) Calculate the reset to primary winding turns ratio.
5) Calculate the tertiary to primary winding turns ratio.
6) Calculate the current-sense resistor value.
7) Calculate the output inductor value.
8) Select the output capacitor.

The circuit in Figure 5 was designed as follows:

1) 30V ≤ V_{IN} ≤ 67V, V_{OUT} = 5V, I_{OUT} = 10A, V_{RIPPLE} ≤ 50mV. Turn-on threshold is set at 38.6V.
2) To set the output voltage, calculate the values of resistors R1 and R2 according to the following equation:

$$\frac{V_{REF}}{V_{OUT}} = \frac{R_2}{R_1 + R_2}$$

where V_{REF} is the reference voltage of the shunt regulator, and R_1 and R_2 are the resistors shown in Figures 5 and 6.

3) The turns ratio of the transformer is calculated based on the minimum input voltage and the lower limit of the maximum duty cycle for the MAX5941B (44%). To enable the use of MOSFETs with drain-source breakdown voltages of less than 200V, use the MAX5941B with the 50% maximum duty cycle. Calculate the turns ratio according to the following equation:

$$\frac{N_S}{N_P} \geq \frac{V_{OUT} + (V_{D1} \times D_{MAX})}{D_{MAX} \times V_{IN_MIN}}$$

where:

N_S/N_P = Turns ratio (N_S is the number of secondary turns and N_P is the number of primary turns).

V_{OUT} = Output voltage (5V).

V_{D1} = Voltage drop across D1 (typically 0.5V for power Schottky diodes).

D_{MAX} = Minimum value of maximum operating duty cycle (44%).

V_{IN_MIN} = Minimum Input voltage (30V).

In this example:

$$\frac{N_S}{N_P} \geq \frac{5V + (0.5V \times 0.44)}{0.44 \times 30V} = 0.395$$

Choose N_P based on core losses and DC resistance. Use the turns ratio to calculate N_S, rounding up to the nearest integer. In this example, N_P = 14 and N_S = 6.

For a forward converter, choose a transformer with a magnetizing inductance in the neighborhood of 200µH. Energy stored in the magnetizing inductance of a forward converter is not delivered to the load and must be returned back to the input; this is accomplished with the reset winding.

The transformer primary to secondary leakage inductance should be less than 1µH. Note that all leakage energy will be dissipated across the MOSFET. Snubber circuits may be used to direct some or all of the leakage energy to be dissipated across a resistor.

To calculate the minimum duty cycle (D_{MIN}), use the following equation:

$$D_{MIN} = \frac{V_{OUT}}{V_{IN_MAX} \times \frac{N_S}{N_P} - V_{D1}} = 17.7$$

where V_{IN_MAX} is the maximum input voltage (67V).

4) The reset winding turns ratio (N_R/N_P) needs to be low enough to guarantee that the entire energy in the transformer is returned to V+ within the off cycle at the maximum duty cycle. Use the following equation to determine the reset winding turns ratio:

$$N_R \le N_P \times \frac{1-D_{MAX}'}{D_{MAX}'}$$

where:

N_R/N_P = Reset winding turns ratio.

D_{MAX}' = Maximum value of maximum duty cycle:

$$N_R \le 14 \times \frac{1-0.5}{0.5} = 14$$

Round N_R to the nearest smallest integer.

The turns ratio of the reset winding (N_R/N_P) determines the peak voltage across the N-channel MOSFET.

Use the following equation to determine the maximum drain-source voltage across the N-channel MOSFET:

$$V_{DSMAX} \ge V_{IN_MAX} \times \left(1 + \frac{N_P}{N_R}\right)$$

V_{DSMAX} = Maximum MOSFET drain-source voltage.

V_{IN_MAX} = Maximum input voltage:

$$V_{DSMAX} \ge 67V \times \left(1 + \frac{14}{14}\right) = 134V$$

Choose MOSFETs with appropriate avalanche power ratings to absorb any leakage energy.

5) Choose the tertiary winding turns ratio (N_T/N_P) so that the minimum input voltage provides the minimum operating voltage at V_{DD} (13V). Use the following equation to calculate the tertiary winding turns ratio:

$$\frac{V_{DDMIN} + 0.7}{V_{IN_MIN}} \times N_P \le N_T \le \frac{V_{DDMAX} + 0.7}{V_{IN_MAX}} \times N_P$$

where:

V_{DDMIN} is the minimum V_{DD} supply voltage (13V).

V_{DDMAX} is the maximum V_{DD} supply voltage (30V).

V_{IN_MIN} is the minimum input voltage (30V).

V_{IN_MAX} is the maximum input voltage (67V in this design example).

N_P is the number of turns of the primary winding.

N_T is the number of turns of the tertiary winding:

$$\frac{13.7}{30} \times 14 \le N_T \le \frac{36.7}{67} \times 14$$
$$6.39 \le N_T \le 7.67$$

Choose $N_T = 7$.

6) Choose R_{SENSE} according to the following equation:

$$R_{SENSE} \le \frac{V_{ILIM}}{\frac{N_S}{N_P} \times 1.2 \times I_{OUTMAX}}$$

where:

V_{ILIM} is the current-sense comparator trip threshold voltage (0.465V).

N_S/N_P is the secondary side turns ratio (5/14 in this example).

I_{OUTMAX} is the maximum DC output current (10A in this example):

$$R_{SENSE} \le \frac{0.465V}{\frac{6}{14} \times 1.2 \times 10} = 90.4m\Omega$$

7) Choose the inductor value so that the peak ripple current (LIR) in the inductor is between 10% and 20% of the maximum output current:

$$L \ge \frac{(V_{OUT} + V_D) \times (1-D_{MIN})}{2 \times LIR \times 275kHz \times I_{OUTMAX}}$$

where V_D is the output Schottky diode forward voltage drop (0.5V) and LIR is the ratio of inductor ripple current to DC output current:

$$L \ge \frac{(5.5) \times (1-0.198)}{0.4 \times 275kHz \times 10A} = 4.01\mu H$$

8) The size and ESR of the output filter capacitor determine the output ripple. Choose a capacitor with a low ESR to yield the required ripple voltage.

Use the following equations to calculate the peak-to-peak output ripple:

$$V_{RIPPLE} = \sqrt{V_{RIPPLE,ESR}^2 + V_{RIPPLE,C}^2}$$

Table 3. Component Suppliers

COMPONENT	SUPPLIERS	WEBSITE
Power FETS	International Rectifier	www.irf.com
	Fairchild	www.fairchildsemi.com
	Vishay-Siliconix	www.vishay.com/brands/siliconix/main.html
Current-Sense Resistors	Dale-Vishay	www.vishay.com/brands/dale/main.html
	IRC	www.irctt.com/pages/index.cfm
Diodes	ON Semi	www.onsemi.com
	General Semiconductor	www.gensemi.com
	Central Semiconductor	www.centralsemi.com
Capacitors	Sanyo	www.sanyo.com
	Taiyo Yuden	www.t-yuden.com
	AVX	www.avxcorp.com
Magnetics	Coiltronics	www.cooperet.com
	Coilcraft	www.coilcraft.com
	Pulse Engineering	www.pulseeng.com

where:

V_{RIPPLE} is the combined RMS output ripple due to $V_{RIPPLE,ESR}$, the ESR ripple, and $V_{RIPPLE,C}$, the capacitive ripple. Calculate the ESR ripple and capacitive ripple as follows:

$$V_{RIPPLE,ESR} = I_{RIPPLE} \times ESR$$

$$V_{RIPPLE,C} = I_{RIPPLE}/(2 \times \pi \times 275kHz \times C_{OUT})$$

Layout Recommendations

All connections carrying pulsed currents must be very short, be as wide as possible, and have a ground plane as a return path. The inductance of these connections must be kept to a minimum due to the high di/dt of the currents in high-frequency switching power converters.

Current loops must be analyzed in any layout proposed, and the internal area kept to a minimum to reduce radiated EMI. Ground planes must be kept as intact as possible.

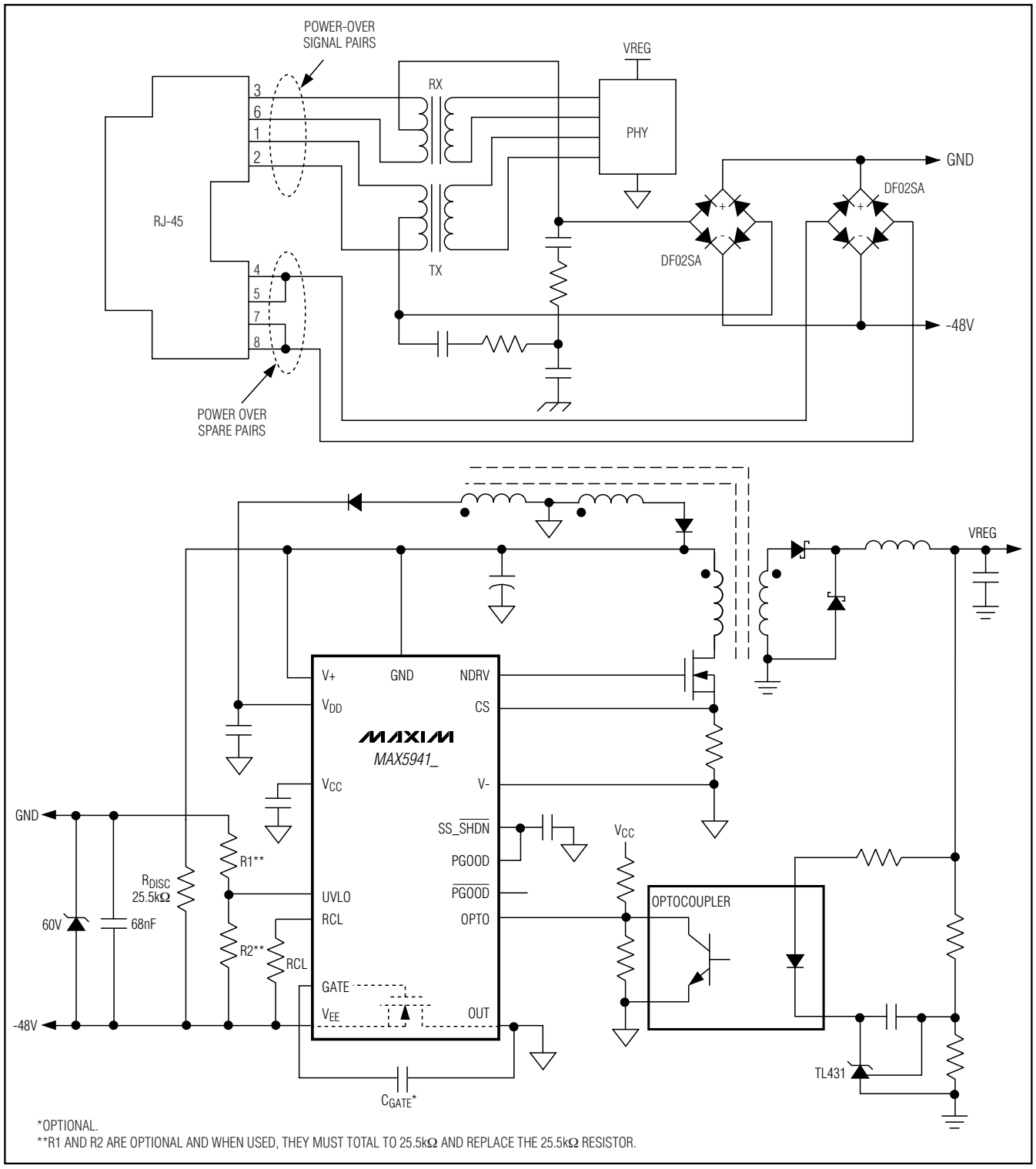

Figure 7. PD with Power-Over-Ethernet (Power Is Provided by Either the Signal Pairs or the Spare Pairs)

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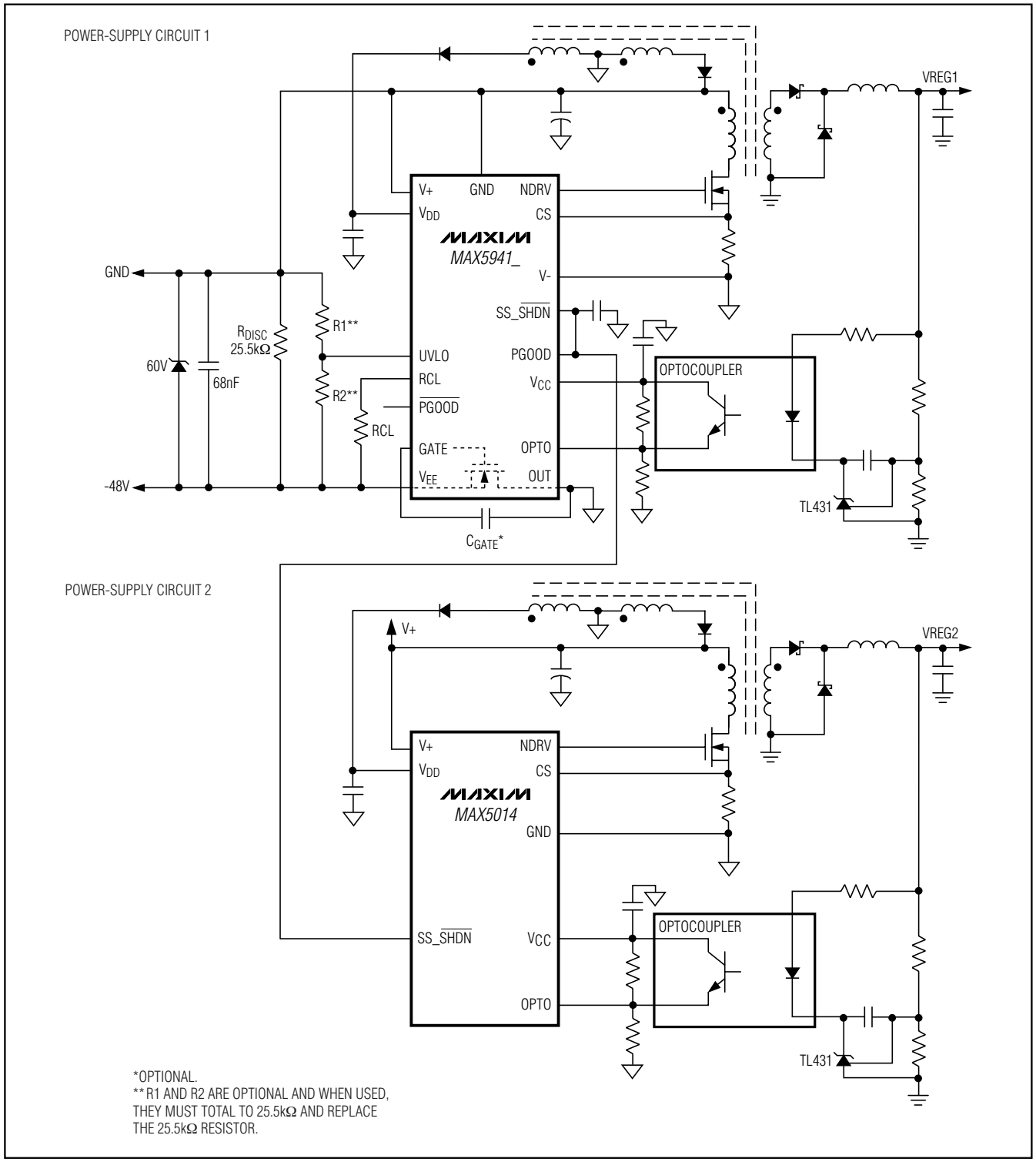
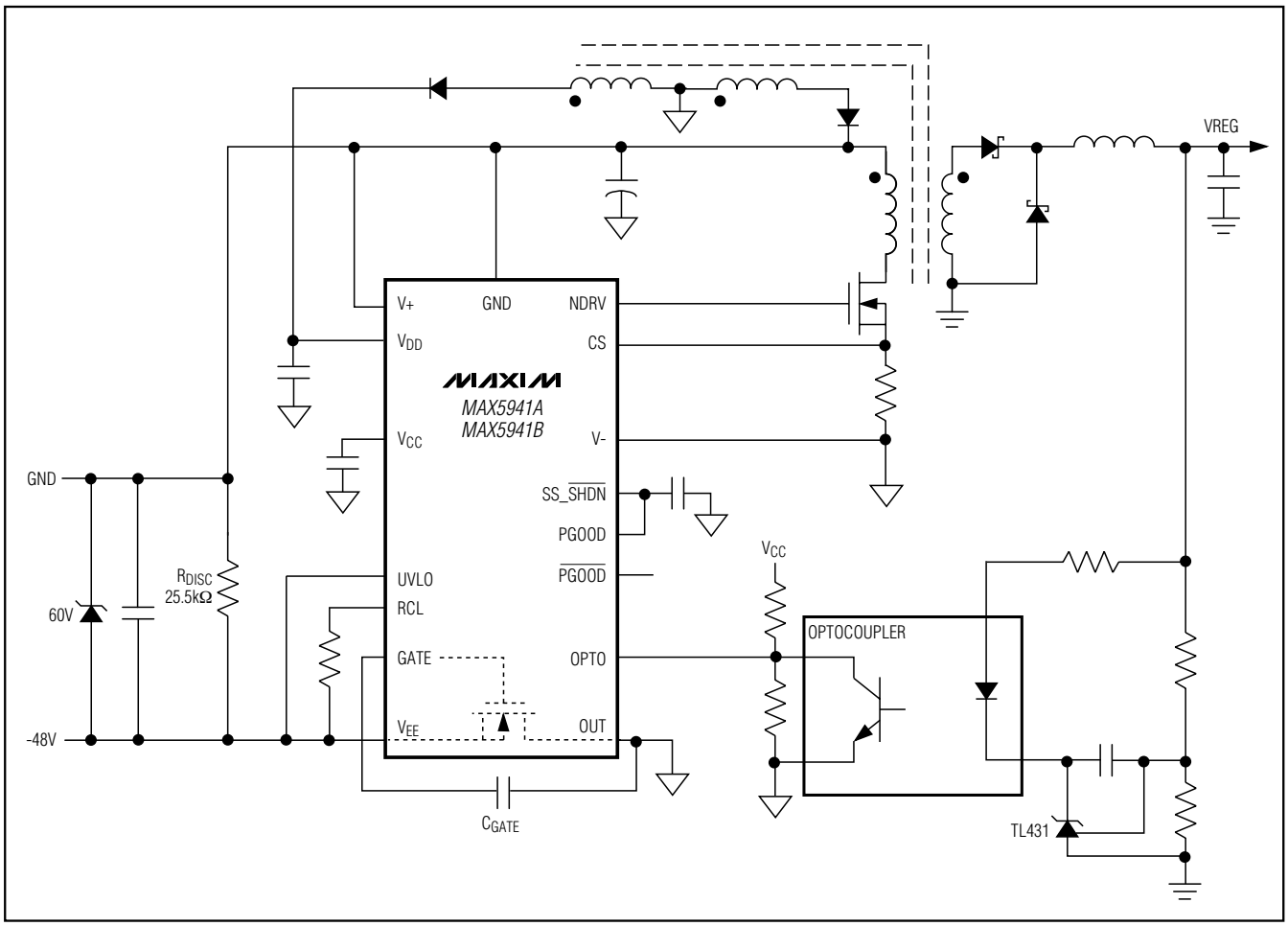


Figure 8. Power-Supply Circuit 1 Enabling PWM Controller of a Second Power Circuit

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 4232

PROCESS: BiCMOS

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Package Information

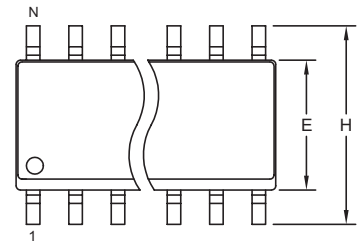
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

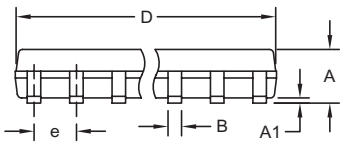
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

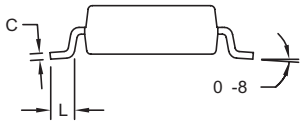
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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