M64895BGP

I²C BUS FREQUENCY SYNTHESIZER FOR TV/VTR

REJ03F0018–0100Z
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Description

The M64895BGP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using I²C BUS control. It contains the prescaler with operating up to 1.3 GHz, 4 band drivers and tuning. amplifier for direct tuning.

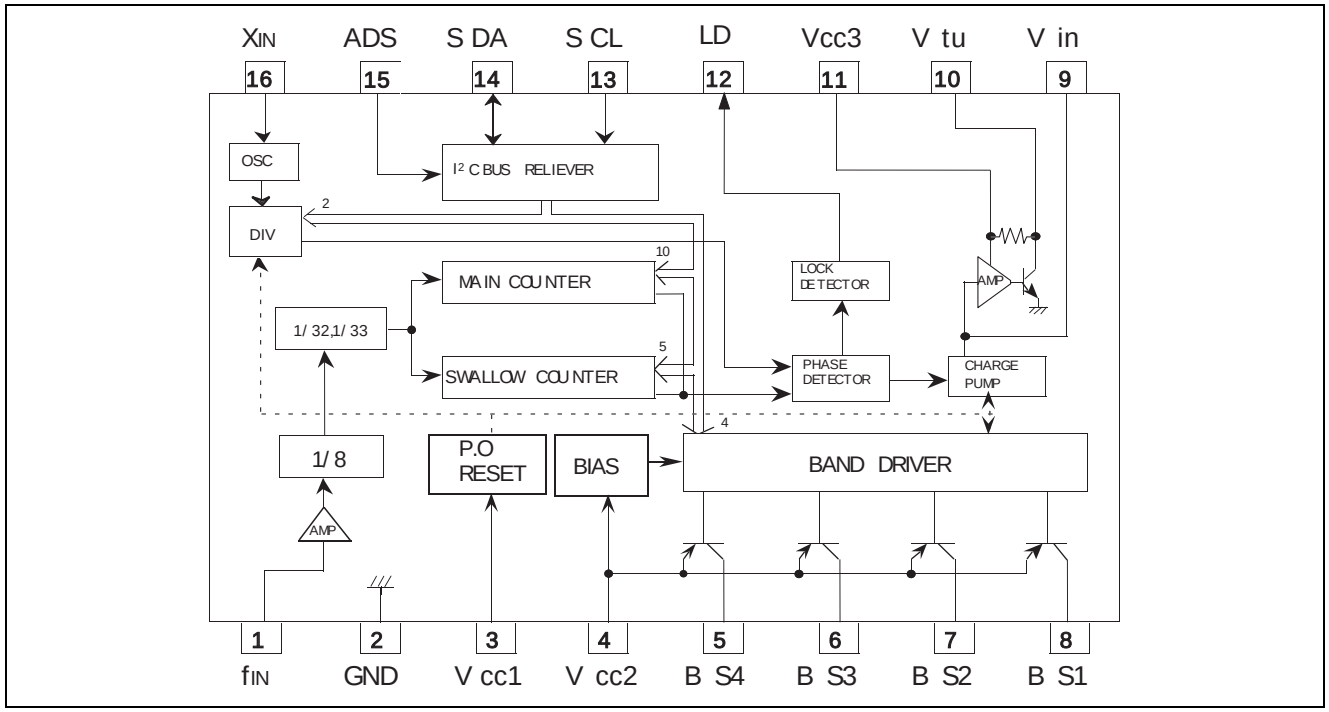
Features

- 4 integrated PNP band drivers (Io = 40 mA, Vsat = 0.2 V typ@Vcc 1 to 13.2 V)
- Built in tuning Amplifier for direct tuning.
- Low power dissipation (Icc = 20 mA, Vcc = 5 V)
- Built-in prescaler with input amplifier (fmax = 1.3 GHz)
- PLL lock/unlock status display output (Built-in pull up resistor)
- I²C bus control (write mode only)
- X 3type of tuning steps (Division ratio 1/512, 1/640, 1/1024) with 4 MHz X'tal
- Programmable chip address
- Small package (16 Pin SSOP)

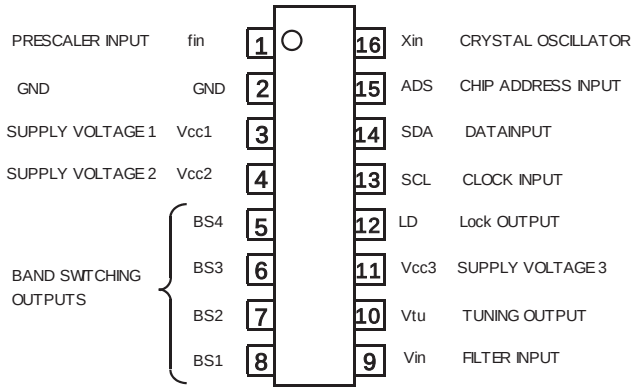
Application

- TV, VCR tuners

Block Diagram



Pin Configuration (TOP VIEW)



OUTLINE 16P2Z

Pin Description

Symbol	Pin No.	Pin name	Function
fin	1	Prescaler input	Input for the VCO frequency.
GND	2	GND	Ground to 0 V
Vcc1	3	Power supply voltage 1	Power supply voltage terminal. 5.0 V+/–0.5 V
Vcc2	4	Power supply voltage 2	Power supply for band switching. Vcc1 to 13.2 V
BS4 BS3 BS2 BS1	5 6 7 8	Band switching outputs	PNP open collector method is used. When the band switching data is “H”, the output is “ON”. When it is “L”, the output is “OFF”.
Vin	9	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f1/N) is ahead compared to the reference frequency (fref), the “source” current state becomes active. If it is lag, the “sink” current becomes active. If the phases are the same, the high impedance state becomes active.
Vtu	10	Tuning output	This supplies the tuning voltage.
Vcc3	11	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35 V
LD/f_{test}	12	Lock detect/Test port	Lock detector is output. Programmable freq. Divider output and reference freq. output is selected by the test mode.
SCL	13	Clock input	Data is read into the shift register when the clock signal falls.
SDA	14	Data input	Input for band SW and programmable frequency. divider set falls.
ADS	15	Address switching input	Chip address sets it up with the input condition of terminal.
X in	16	This is connected to theCrystal oscillator.	4.0 MHz crystal oscillator connected.

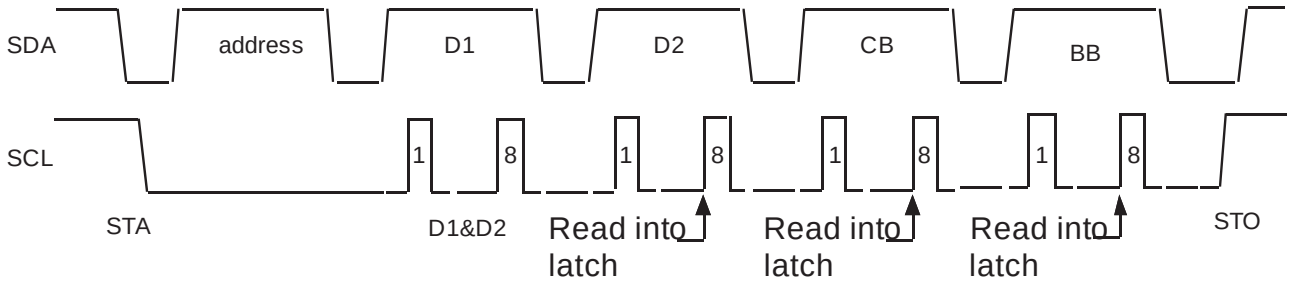
Method of setting DATA

The input information of chip address and data of 2 or 4 bytes are received in I^2C bus receiver. It shows a de definition of bus protocol admitted in the following.

1_STA CA CB BB STO
2_STA CA D1 D2 STO
3_STA CA CB BB D1 D2 STO
4_STA CA D1 D2 CB BB STO

STA: Start condition
STO: Stop condition
CA: Chip address
CB: Control data byte
BB: Band S.W. data byte
D1: Divider data byte
D2: Divider data byte

The information of 5 bytes required for circuit operation are chip address, control data and band S.W.data of 2 bytes and divider data of 2 bytes. After the chip address input, 2 or 4 bytes can be received. Function bit contained the first and the third data byte to distinguish between divider data and control data band S.W. data, and ”0” goes ahead of divider data and “1” goes ahead of control data, band S.W. data,
The timing reading data show in under figure. Divider data uses 15 bits is read in at the rise of the eighth bit clock signal of the second byte divider data (D2). Control data (CB) and band SW-data (BB) is each read in the rise of eighth bits clock signal.



Write mode format

	Byte	MSB								LSB
1	Address Byte	1	1	0	0	0	MA1	MA0	0	A
2	Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	A
3	Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	A
4	Control Byte 1	1	CP	T2	T1	T0	RSa	RSb	OS	A
5	Band SW Byte	X	X	X	X	BS4	BS3	BS2	BS1	A

Mode data set up method

X: Random, 0 or 1. normal "0"

MA1, MAO: programmable Address Bit

Address input voltage	MA1	MA
0 to 0.1 *Vcc1	0	0
Always valid	0	1
0.4*Vcc1 to 0.6*Vcc1	1	0
0.9*Vcc1 to Vcc1	1	1

N14 to NO: How to set dividing ratio of the programmable the divider

Dividing ratio N = N14 (2^{14} = 16384) +… +N0 (2^{0} = 1)

Therefore, the rage of division N is 1,024 to 32,768

(Example) frvco = fref*8*N

= 3.90625 * 8 * N

= 31.25 * N (kHz)

CP: Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70µA	Test
1	270µA	Normal

T2, T1, T0: Setting up for the test mode

T2	T1	T0	Charge pump	12 pin condition	Mode
0	0	X	Normal operation	Lock output	Normal operation
0	1	X	High impedance	Lock output	Test
1	1	0	Sink	Lock output	Test
1	1	1	Source	Lock output	Test
1	0	0	High impedance	fref output	Test
1	0	1	High impedance	f1/N output	Test

RSa, RSb: Set up for the reference Frequency division ratio

RSa	RSb	division ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS: Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

Power on rest operation (Initial state the power is turned ON)

BS4 to BS1 :OFF

Charge pump : High impedance

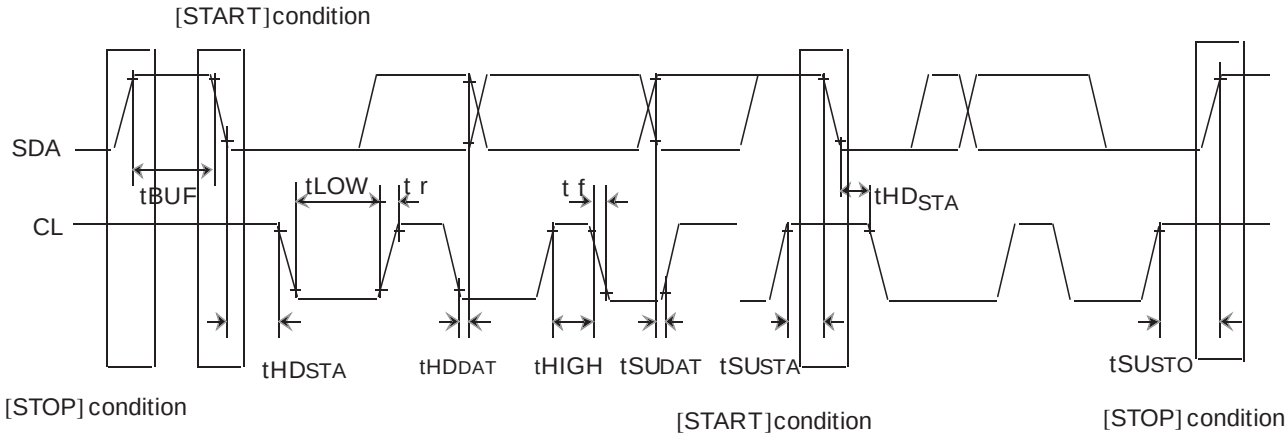
Tuning amplifier : OFF

Charge pump current : 270 μA

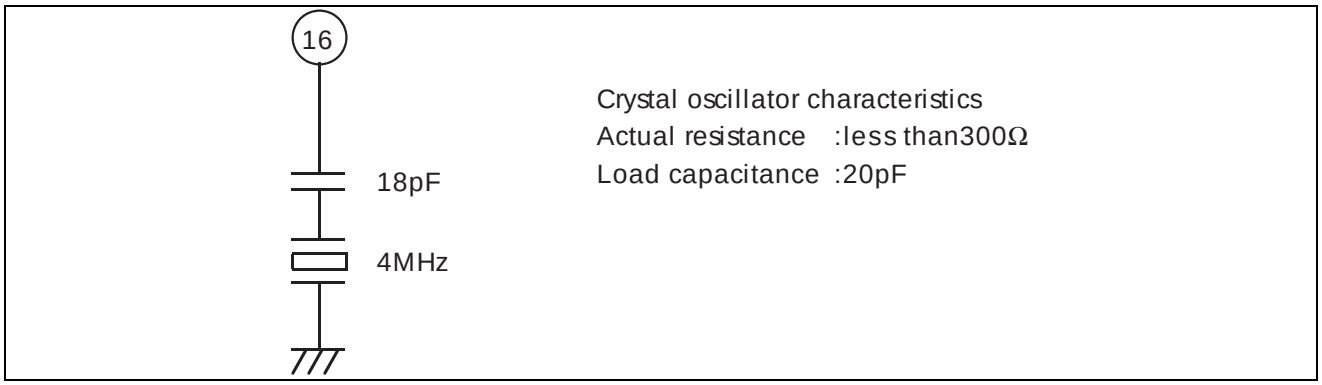
Frequency division ratio : 1/1024

Lock detector : H

Timing diagram



Crystal oscillator connection diagram



Absolute maximum ratings

(Ta = –20°C to 75°C unless otherwise noted)

Parameter	Symbols	Max. ratings	Units	Conditions
Standby voltage1	Vcc1	6.0	V	Pin3
Standby voltage2	Vcc2	14.4	V	Pin4
Standby voltage3	Vcc3	36.0	V	Pin11
Input voltage	VI	6.0	V	Not to exceed Vcc1
Output voltage	Vo	6.0	V	Pin 12
Voltage applied when the band output current is OFF	V_{BSOFF}	14.4	V	
Band output current	I_{BSON}	50.0	mA	Per 1 band output circuit
ON the time when the band output is ON	t_{BSON}	10	sec	50 mA per 1 band output circuit 3 circuits are pin at same time,
Power dissipation	Pd	350	mW	Ta = 75°C
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Recommended operating conditions

(Ta = –20°C to 75°C unless otherwise noted)

Parameter	Symbols	Ratings	Units	Conditions
Standby voltage1	Vcc1	4.5 to 5.5	V	
Standby voltage2	Vcc2	5.0 to 13.2	V	
Standby voltage3	Vcc3	30 to 35	V	
Operating frequency (1)	fopr1	4.0	MHz	Crystal oscillation circuit
Operating frequency (2)	fopr2	80 to 1300	MHz	
Band output current 5 to 8	I_{BDL}	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical Characteristics

(Ta = –20°C to 75°C, Vcc1 = 5.0 V Vcc = 12 V, Vcc3 = 33 V, unless otherwise noted)

Parameters	Symbol	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
Input terminals							
“H” input voltage	VIH	13 to 14		3.0	—	Vcc1+0.3	V
“L” input voltage	VIL	13 to 14		—	—	1.5	V
“H” input current	IIH	13 to 14	Vcc1 = 5.5 V, Vi = 4.0 V	—	—	10	µA
“L” input current	IIL	13/14	Vcc1 = 5.5 V, Vi = 0.4 V	—	–4/–14	–10/–30	µA
SDA output							
“L” output voltage	VOL	14	Vcc1 = 5.5 V, Ic = 3 mA	—	—	0.4	V
Leak current	ILO	14	Vcc1 = 5.5 V, Ic = 5.5 V	—	—	10	µA
Band SW							
Output voltage	V_{BS}	5 to 8	Vcc2 = 12 V, Io = −40 mA	11.6	11.8	—	V
Leak current	$I_{OIK}1$	5 to 8	Vcc2 = 12 V, Band SW is OFF Vo = 0 V	—	—	–10	µA
Tuning output							
Output voltage “H”	VtoH	10	Vcc3 = 33 V	32.5	—	—	V
Output voltage “L”	VtoL	10	Vcc3 = 33 V	—	0.2	0.4	V
Charge pump			Vcc1 = 5.0 V, Vo = 2.5 V				
“H” output current	I_{OH}	9	Vcc1 = 5.0 V, Vo = 2.5 V	—	±270	±370	µA
“L” output current	I_{OL}	9	Vcc1 = 5.0 V, Vo = 2.5 V	—	±70	±110	µA
Leak current	I_{cpLK}	9	Vcc1 = 5.5 V	—	—	±50	nA
Supply current 1	$I_{CC}1$	3		—	20	30	mA
Supply current 2			Vcc2 = 12 V				
4circuits OFF	$I_{CC}2A$	4		—	—	0.3	mA
1 circuits ON,			Vcc2 = 12 V				
Output open	$I_{CC}2B$	4	Vcc2 = 12 V, Io = –40 mA	—	6.0	8.0	mA
Output current 40 mA	$I_{CC}2C$	4	Vcc2 = 33 V, Output ON	—	46.0	48.0	mA
Supply current 3	$I_{CC}3$	11		—	3.0	4.0	mA

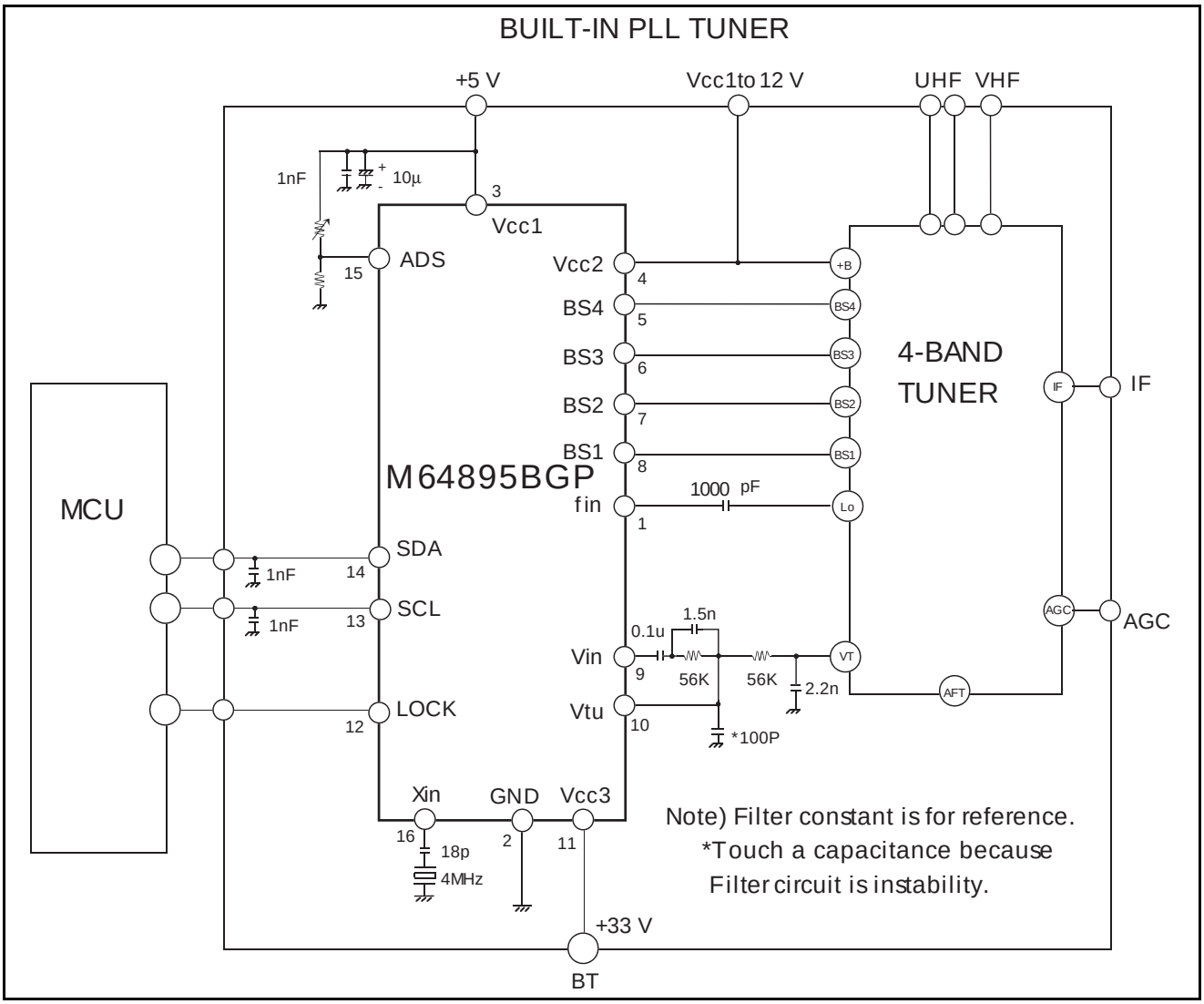
Note: The typical values are at Vcc1 = 5.0 V, Vcc 2 = 12 V, Vcc3 = 33 V, Ta = +25°C

Switching characteristics

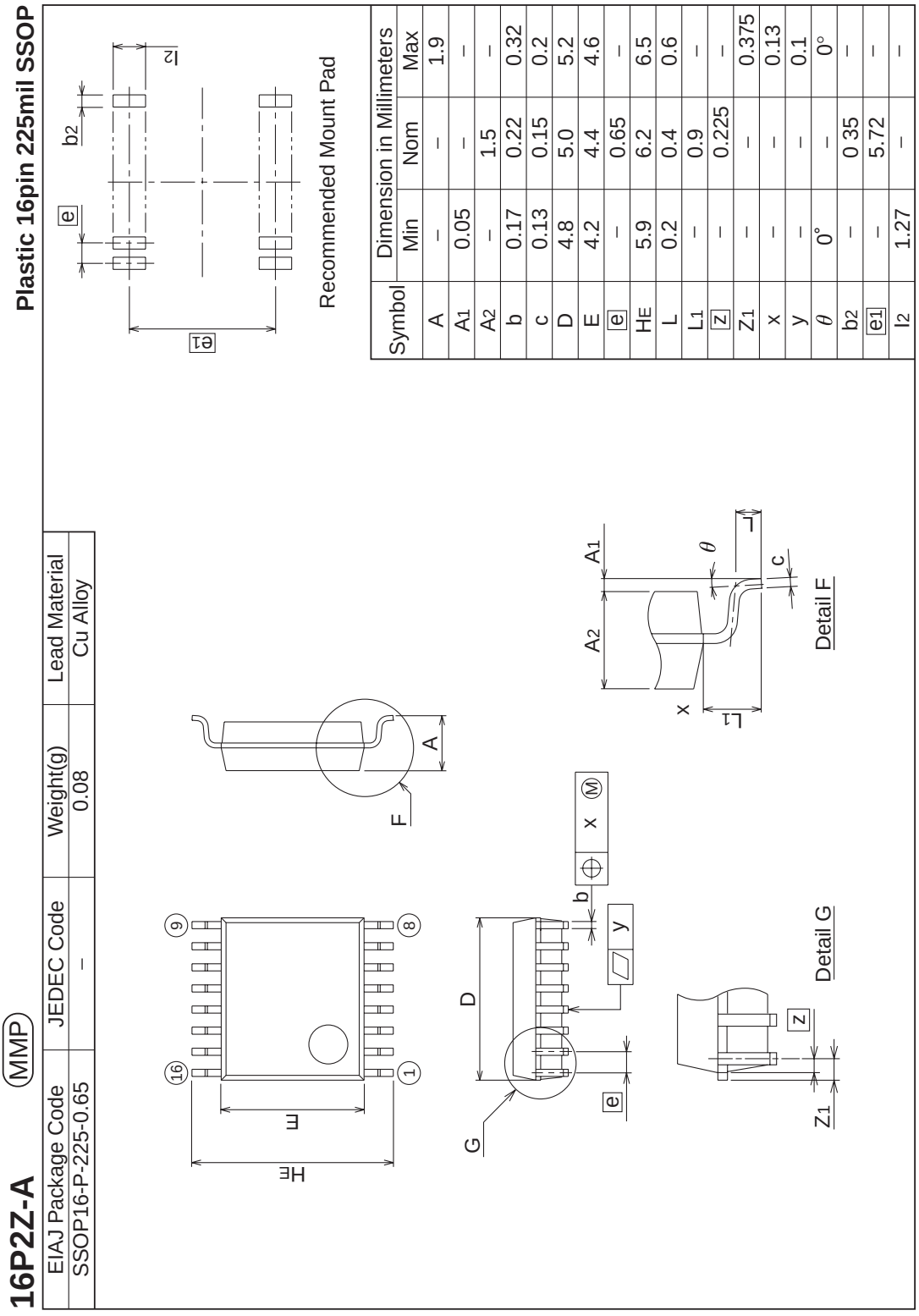
(Ta = –20°C to 75°C, Vcc1 = 5.0 V, Vcc = 12 V, Vcc3 = 33 V, unless otherwise noted)

Parameter	Symbol	Test pin	Test conditions		Limits			Unit used
					Min	Typ	Max	
Prescaler operating frequency	fopr	1	Vcc1 = 4.5 to 5.5 V Vin = Vinmin to Vinmax		80	—	1300	MHz
Operating input voltage	Vin	1	Vcc1 = 4.5 to 5.5 V	80 to 100 MHz	–24	—	4	dBm
				100 to 200 MHz	–27	—	4	
				200 to 800 MHz	–30	—	4	
				800 to 1000 MHz	–27	—	4	
				1000 to 1300 MHz	–18	—	4	
Clock pulse frequency	f_{SCL}	13	Vcc1 = 4.5 to 5.5 V		0	—	100	kHz
Bus free time	t_{BUF}	14	Vcc1 = 4.5 to 5.5 V		4.7	—	—	µs
Data hold time	t_{HDSTA}	13	Vcc1 = 4.5 to 5.5 V		4	—	—	µs
SCL low hold time	t_{LOW}	13	Vcc1 = 4.5 to 5.5 V		4.7	—	—	µs
SCL high hold time	t_{HIGH}	13	Vcc1 = 4.5 to 5.5 V		4	—	—	µs
Set up time	t_{SUSTA}	13, 14	Vcc1 = 4.5 to 5.5 V		4.7		—	µs
Data hold time	t_{HDDAT}	13, 14	Vcc1 = 4.5 to 5.5 V		0	—	—	s
Data set up time	t_{SUDAT}	13, 14	Vcc1 = 4.5 to 5.5 V		250	—	—	ns
Rise time	tR	13, 14	Vcc1 = 4.5 to 5.5 V		—	—	1000	ns
Fall time	tF	13, 14	Vcc1 = 4.5 to 5.5 V		—	—	300	ns
Set up time	t_{SUSTO}	13, 14	Vcc1 = 4.5 to 5.5 V		4	—	—	µs

Application example



Package Dimensions



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