

M64895BGP

I²C BUS FREQUENCY SYNTHESIZER FOR TV/VTR

REJ03F0018-0100Z

Rev.1.0

Aug.27.2003

Description

The M64895BGP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using I²C BUS control. It contains the prescaler with operating up to 1.3 GHz, 4 band drivers and tuning amplifier for direct tuning.

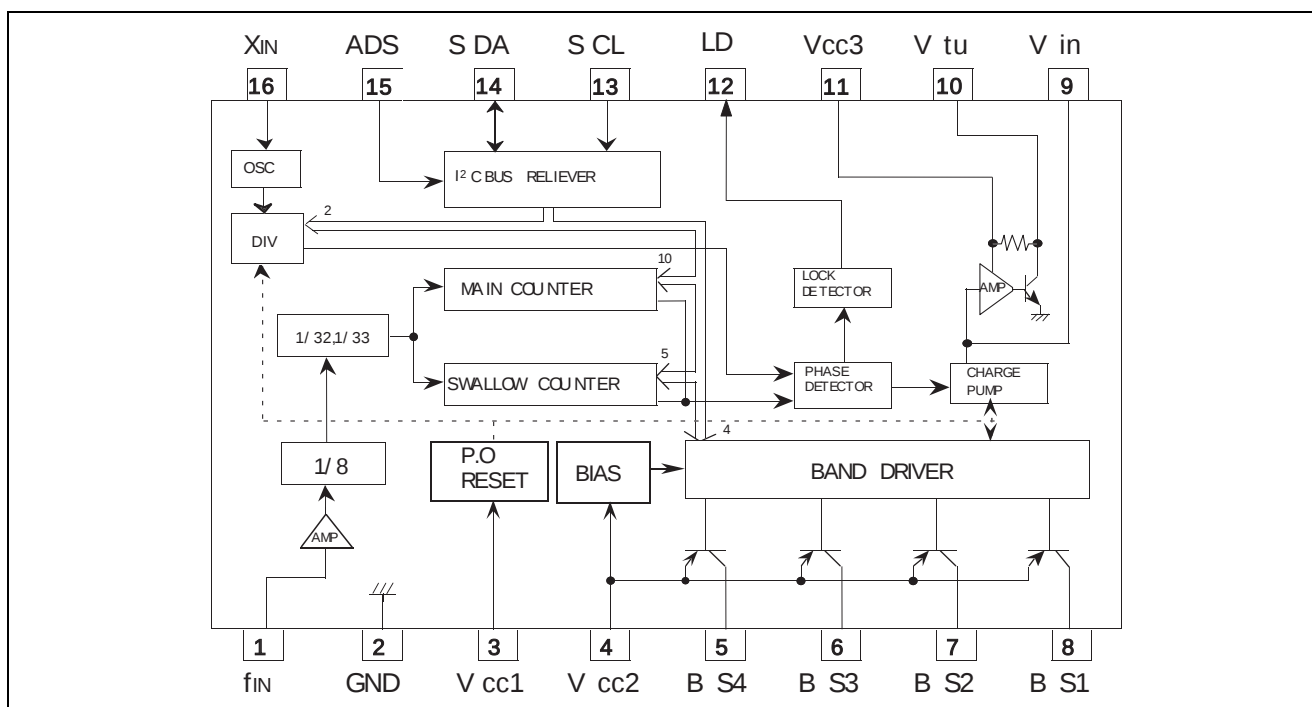
Features

- 4 integrated PNP band drivers ($I_o = 40 \text{ mA}$, $V_{sat} = 0.2 \text{ V typ@Vcc 1 to 13.2 V}$)
- Built in tuning Amplifier for direct tuning.
- Low power dissipation ($I_{cc} = 20 \text{ mA}$, $V_{cc} = 5 \text{ V}$)
- Built-in prescaler with input amplifier ($f_{max} = 1.3 \text{ GHz}$)
- PLL lock/unlock status display output (Built-in pull up resistor)
- I²C bus control (write mode only)
- X 3type of tuning steps (Division ratio 1/512, 1/640, 1/1024) with 4 MHz X'tal
- Programmable chip address
- Small package (16 Pin SSOP)

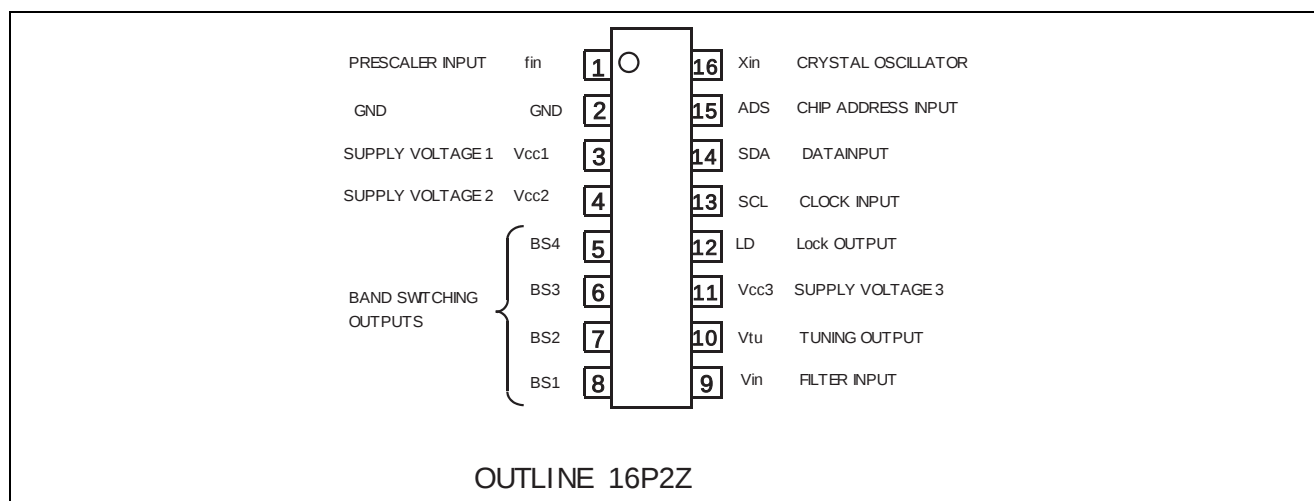
Application

- TV, VCR tuners

Block Diagram



Pin Configuration (TOP VIEW)



Pin Description

Symbol	Pin No.	Pin name	Function
fin	1	Prescaler input	Input for the VCO frequency.
GND	2	GND	Ground to 0 V
Vcc1	3	Power supply voltage 1	Power supply voltage terminal. 5.0 V+/-0.5 V
Vcc2	4	Power supply voltage 2	Power supply for band switching. Vcc1 to 13.2 V
BS4	5	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is "ON". When it is "L", the output is "OFF".
BS3	6		
BS2	7		
BS1	8		
Vin	9	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f_1/N) is ahead compared to the reference frequency (f_{ref}), the "source" current state becomes active. If it is lag, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
Vtu	10	Tuning output	This supplies the tuning voltage.
Vcc3	11	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35 V
LD/ f_{test}	12	Lock detect/Test port	Lock detector is output. Programmable freq. Divider output and reference freq. output is selected by the test mode.
SCL	13	Clock input	Data is read into the shift register when the clock signal falls.
SDA	14	Data input	Input for band SW and programmable frequency. divider set falls.
ADS	15	Address switching input	Chip address sets it up with the input condition of terminal.
X in	16	This is connected to the Crystal oscillator.	4.0 MHz crystal oscillator connected.

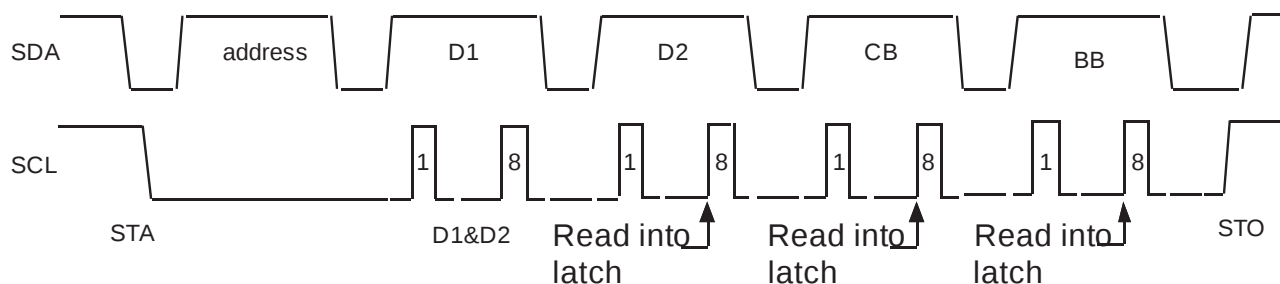
Method of setting DATA

The input information of chip address and data of 2 or 4 bytes are received in I²C bus receiver. It shows a definition of bus protocol admitted in the following.

1_STA	CA CB BB STO	STA: Start condition
2_STA	CA D1 D2 STO	STO: Stop condition
3_STA	CA CB BB D1 D2 STO	CA: Chip address
4_STA	CA D1 D2 CB BB STO	CB: Control data byte
		BB: Band S.W. data byte
		D1: Divider data byte
		D2: Divider data byte

The information of 5 bytes required for circuit operation are chip address, control data and band S.W. data of 2 bytes and divider data of 2 bytes. After the chip address input, 2 or 4 bytes can be received. Function bit contained the first and the third data byte to distinguish between divider data and control data band S.W. data, and "0" goes ahead of divider data and "1" goes ahead of control data, band S.W. data,

The timing reading data show in under figure. Divider data uses 15 bits is read in at the rise of the eighth bit clock signal of the second byte divider data (D2). Control data (CB) and band SW-data (BB) is each read in the rise of eighth bits clock signal.



Write mode format

Byte	MSB									LSB
1 Address Byte	1	1	0	0	0	MA1	MA0	0		A
2 Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8		A
3 Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0		A
4 Control Byte 1	1	CP	T2	T1	T0	RSa	RSb	OS		A
5 Band SW Byte	X	X	X	X	BS4	BS3	BS2	BS1		A

Mode data set up method

X: Random, 0 or 1. normal “0”

MA1, MA0: programmable Address Bit

Address input voltage	MA1	MA
0 to 0.1 *Vcc1	0	0
Always valid	0	1
0.4*Vcc1 to 0.6*Vcc1	1	0
0.9*Vcc1 to Vcc1	1	1

N14 to N0: How to set dividing ratio of the programmable the divider

Dividing ratio $N = N_{14} (2^{14} = 16384) + \dots + N_0 (2^0 = 1)$

Therefore, the range of division N is 1,024 to 32,768

(Example) $f_{rvco} = f_{ref} * 8 * N$

$= 3.90625 * 8 * N$

$= 31.25 * N \text{ (kHz)}$

CP: Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70μA	Test
1	270μA	Normal

T2, T1, T0: Setting up for the test mode

T2	T1	T0	Charge pump	12 pin condition	Mode
0	0	X	Normal operation	Lock output	Normal operation
0	1	X	High impedance	Lock output	Test
1	1	0	Sink	Lock output	Test
1	1	1	Source	Lock output	Test
1	0	0	High impedance	f _{ref} output	Test
1	0	1	High impedance	f _{1/N} output	Test

RSa, RSb: Set up for the reference Frequency division ratio

RSa	RSb	division ratio
1	1	1/512
0	1	1/1024
X	0	1/640

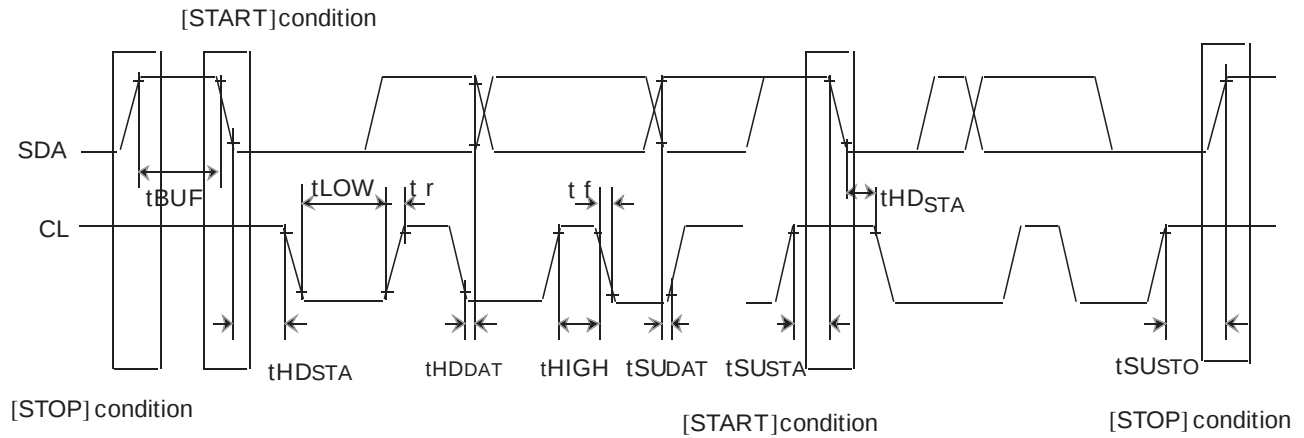
OS: Set up the tuning amplifier

OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

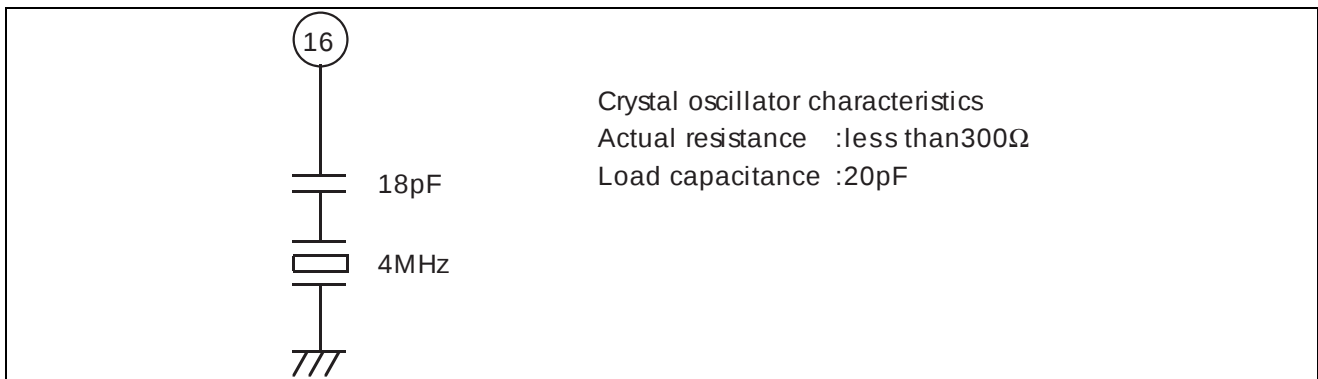
Power on rest operation (Initial state the power is turned ON)

BS4 to BS1 :OFF
Charge pump : High impedance
Tuning amplifier : OFF
Charge pump current : 270 μ A
Frequency division ratio : 1/1024
Lock detector : H

Timing diagram



Crystal oscillator connection diagram



Absolute maximum ratings

(Ta = -20°C to 75°C unless otherwise noted)

Parameter	Symbols	Max. ratings	Units	Conditions
Standby voltage1	Vcc1	6.0	V	Pin3
Standby voltage2	Vcc2	14.4	V	Pin4
Standby voltage3	Vcc3	36.0	V	Pin11
Input voltage	VI	6.0	V	Not to exceed Vcc1
Output voltage	Vo	6.0	V	Pin 12
Voltage applied when the band output current is OFF	V _{BSOFF}	14.4	V	
Band output current	I _{BSON}	50.0	mA	Per 1 band output circuit
ON the time when the band output is ON	t _{BSON}	10	sec	50 mA per 1 band output circuit 3 circuits are pin at same time,
Power dissipation	Pd	350	mW	Ta = 75°C
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

Recommended operating conditions

(Ta = -20°C to 75°C unless otherwise noted)

Parameter	Symbols	Ratings	Units	Conditions
Standby voltage1	Vcc1	4.5 to 5.5	V	
Standby voltage2	Vcc2	5.0 to 13.2	V	
Standby voltage3	Vcc3	30 to 35	V	
Operating frequency (1)	fopr1	4.0	MHz	Crystal oscillation circuit
Operating frequency (2)	fopr2	80 to 1300	MHz	
Band output current 5 to 8	I _{BDL}	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical Characteristics

(Ta = -20°C to 75°C, Vcc1 = 5.0 V Vcc = 12 V, Vcc3 = 33 V, unless otherwise noted)

Parameters	Symbol	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
Input terminals							
“H” input voltage	V _{IH}	13 to 14		3.0	—	V _{cc1} +0.3	V
“L” input voltage	V _{IL}	13 to 14		—	—	1.5	V
“H” input current	I _{IH}	13 to 14	V _{cc1} = 5.5 V, V _i = 4.0 V	—	—	10	μA
“L” input current	I _{IL}	13/14	V _{cc1} = 5.5 V, V _i = 0.4 V	—	−4/−14	−10/−30	μA
SDA output							
“L” output voltage	V _{OL}	14	V _{cc1} = 5.5 V, I _c = 3 mA	—	—	0.4	V
Leak current	I _{LO}	14	V _{cc1} = 5.5 V, I _c = 5.5 V	—	—	10	μA
Band SW							
Output voltage	V _{BS}	5 to 8	V _{cc2} = 12 V, I _o = −40 mA	11.6	11.8	—	V
Leak current	I _{OIK1}	5 to 8	V _{cc2} = 12 V, Band SW is OFF V _o = 0 V	—	—	−10	μA
Tuning output							
Output voltage “H”	V _{toH}	10	V _{cc3} = 33 V	32.5	—	—	V
Output voltage “L”	V _{toL}	10	V _{cc3} = 33 V	—	0.2	0.4	V
Charge pump			V _{cc1} = 5.0 V, V _o = 2.5 V				
“H” output current	I _{OH}	9	V _{cc1} = 5.0 V, V _o = 2.5 V	—	±270	±370	μA
“L” output current	I _{OL}	9	V _{cc1} = 5.0 V, V _o = 2.5 V	—	±70	±110	μA
Leak current	I _{cpLK}	9	V _{cc1} = 5.5 V	—	—	±50	nA
Supply current 1	I _{CC1}	3		—	20	30	mA
Supply current 2			V _{cc2} = 12 V				
4circuits OFF	I _{CC2A}	4		—	—	0.3	mA
1 circuits ON,			V _{cc2} = 12 V				
Output open	I _{CC2B}	4	V _{cc2} = 12 V, I _o = −40 mA	—	6.0	8.0	mA
Output current 40 mA	I _{CC2C}	4	V _{cc2} = 33 V, Output ON	—	46.0	48.0	mA
Supply current 3	I _{CC3}	11		—	3.0	4.0	mA

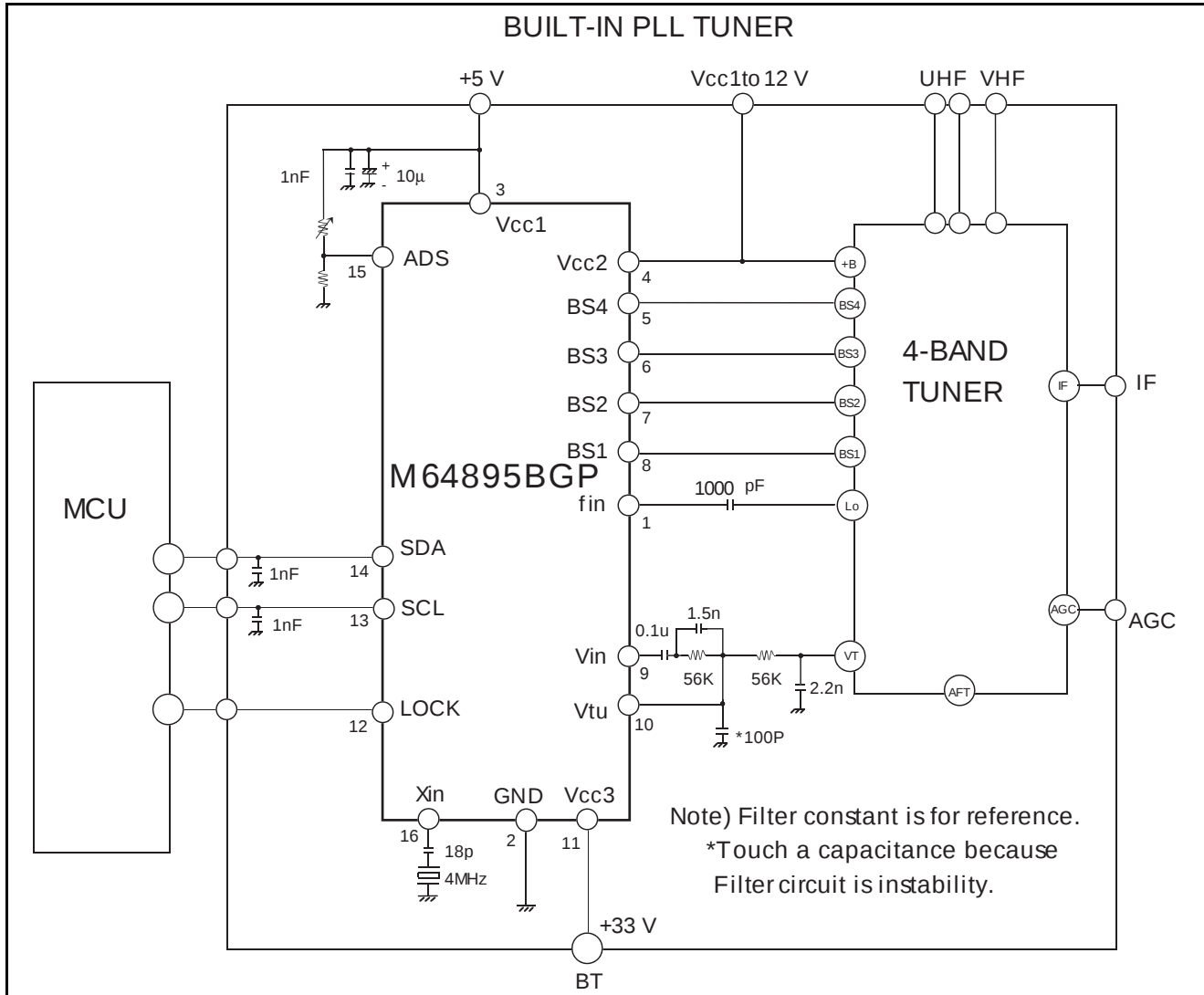
Note: The typical values are at Vcc1 = 5.0 V, Vcc 2 = 12 V, Vcc3 = 33 V, Ta = +25°C

Switching characteristics

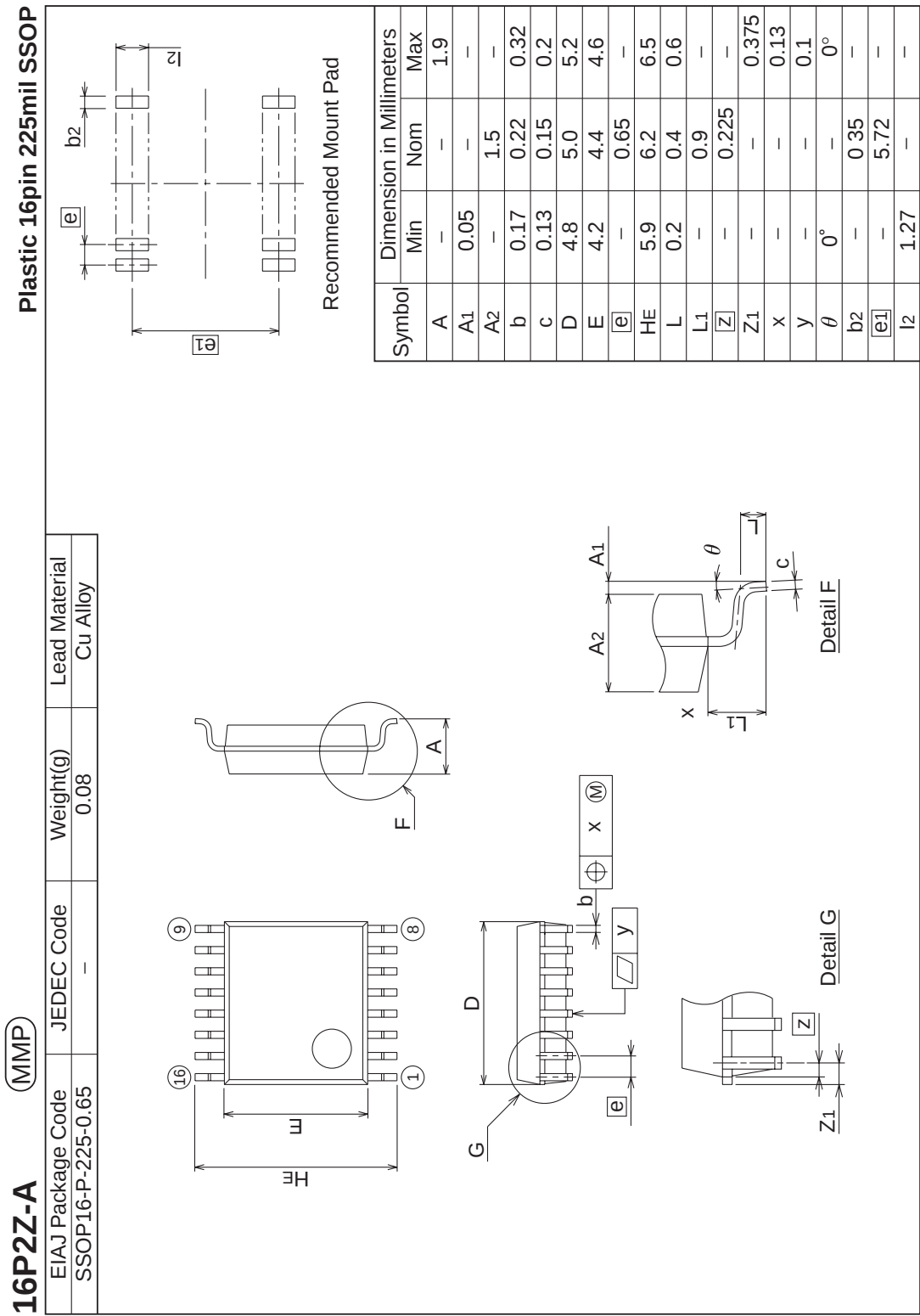
(Ta = -20°C to 75°C, Vcc1 = 5.0 V, Vcc = 12 V, Vcc3 = 33 V, unless otherwise noted)

Parameter	Symbol	Test pin	Test conditions	Limits			Unit used	
				Min	Typ	Max		
Prescaler operating frequency	fopr	1	Vcc1 = 4.5 to 5.5 V Vin = Vinmin to Vinmax	80	—	1300	MHz	
Operating input voltage	Vin	1	Vcc1 = 4.5 to 5.5 V	80 to 100 MHz	−24	—	4	dBm
				100 to 200 MHz	−27	—	4	
				200 to 800 MHz	−30	—	4	
				800 to 1000 MHz	−27	—	4	
				1000 to 1300 MHz	−18	—	4	
Clock pulse frequency	fSCL	13	Vcc1 = 4.5 to 5.5 V	0	—	100	kHz	
Bus free time	tBUF	14	Vcc1 = 4.5 to 5.5 V	4.7	—	—	μs	
Data hold time	tHDSTA	13	Vcc1 = 4.5 to 5.5 V	4	—	—	μs	
SCL low hold time	tLOW	13	Vcc1 = 4.5 to 5.5 V	4.7	—	—	μs	
SCL high hold time	tHIGH	13	Vcc1 = 4.5 to 5.5 V	4	—	—	μs	
Set up time	tSUSTA	13, 14	Vcc1 = 4.5 to 5.5 V	4.7		—	μs	
Data hold time	tHDDAT	13, 14	Vcc1 = 4.5 to 5.5 V	0	—	—	s	
Data set up time	tSUDAT	13, 14	Vcc1 = 4.5 to 5.5 V	250	—	—	ns	
Rise time	tR	13, 14	Vcc1 = 4.5 to 5.5 V	—	—	1000	ns	
Fall time	tF	13, 14	Vcc1 = 4.5 to 5.5 V	—	—	300	ns	
Set up time	tSUSTO	13, 14	Vcc1 = 4.5 to 5.5 V	4	—	—	μs	

Application example



Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001