MC144110
MC144111

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DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

The MC144110 and MC144111 are low-cost six-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

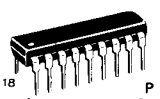
Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 volt supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 volts.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS μP
- Wide Operating Voltage Range: 4.5 to 15 Volts
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

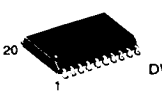
CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

DIGITAL-TO-ANALOG CONVERTERS WITH SERIAL INTERFACE

MC144110

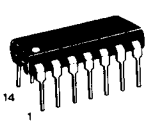


P SUFFIX
PLASTIC DIP
CASE 707

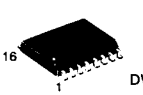


DW SUFFIX
SOG
CASE 751D

MC144111

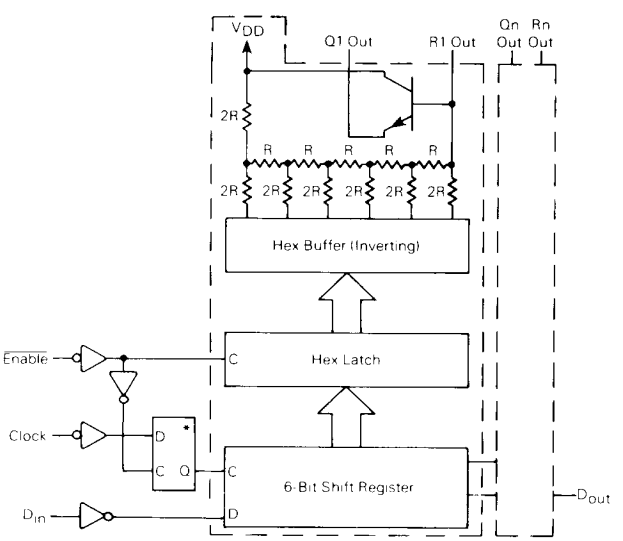


P SUFFIX
PLASTIC DIP
CASE 646



DW SUFFIX
SOG
CASE 751G

BLOCK DIAGRAM



ORDERING INFORMATION

MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

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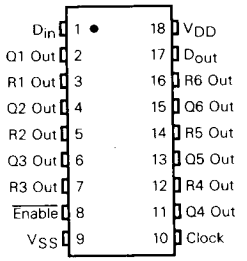
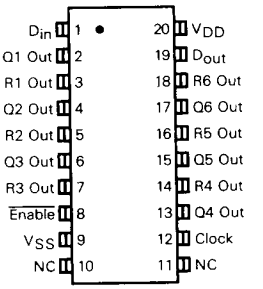
PIN ASSIGNMENTS

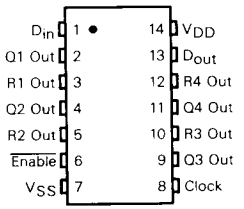
MC144110P



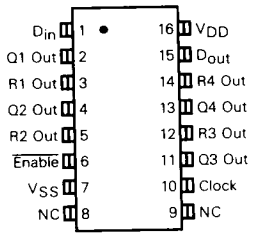
MC144110DW



MC144111P



MC144111DW



NC = No Connection

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Power Dissipation (Per Output) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_{OH}	 30 50 10 20	mW
Power Dissipation (Per Package) T_A = 70°C, MC144110 MC144111 T_A = 85°C, MC144110 MC144111	P_D	 100 150 25 50	mW
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 0° to 85°C unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	Min	Max	Unit
V_{IH}	High-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5 10 15	3.0 3.5 4.0	– – –	V
V_{IL}	Low-Level Input Voltage (D_{in}, $\overline{Enable}$, Clock)		5 10 15	– – –	0.8 0.8 0.8	V
I_{OH}	High-Level Output Current (D_{out})	$V_{out} = V_{DD} - 0.5$ V	5	− 200	–	μA
I_{OL}	Low-Level Output Current (D_{out})	V_{out} = 0.5 V	5	200	–	μA
I_{DD}	Quiescent Supply Current	I_{out} = 0 μA MC144110 MC144111	15 15	– –	12 8	mA
I_{in}	Input Leakage Current (D_{in}, $\overline{Enable}$, Clock)	$V_{in} = V_{DD}$ or 0 V	15	–	± 1	μA
V_{nonl}	Nonlinearity Voltage (Rn Out)	See Figure 1	5 10 15	– – –	100 200 300	mV
V_{step}	Step Size (Rn Out)	See Figure 2	5 10 15	19 39 58	137 274 411	mV
V_{offset}	Offset Voltage from V_{SS}	D_{in} = $00, See Figure 1	–	–	1	LSB
I_E	Emitter Leakage Current	$V_{Rn\ Out}$ = 0 V	15	–	10	μA
h_{FE}	DC Current Gain	I_E = 0.1 to 10.0 mA T_A = 25°C	–	40	–	–
V_{BE}	Base to Emitter Voltage Drop	I_E = 1.0 mA	–	0.4	0.7	V

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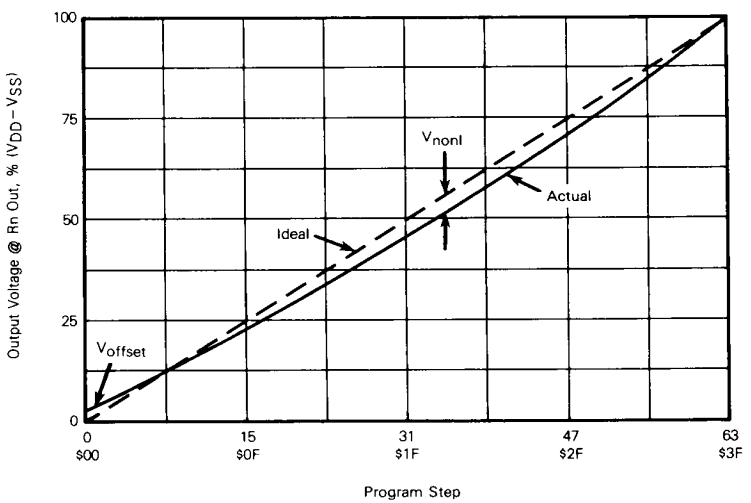
SWITCHING CHARACTERISTICS (Voltages Referenced to V_{SS}, $T_A = 0$ to 85°C, $C_L = 50$ pF, Input $t_r = t_f = 20$ ns Unless Otherwise Indicated)

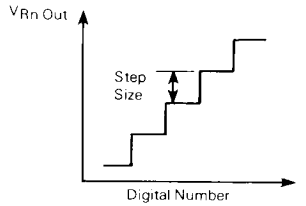
Symbol	Parameter	V_{DD}	Min	Max	Unit
t_{wH}	Positive Pulse Width, Clock (Figures 3 and 4)	5	2	–	µs
		10	1.5	–	
		15	1	–	
t_{wL}	Negative Pulse Width, Clock (Figures 3 and 4)	5	5	–	µs
		10	3.5	–	
		15	2	–	
t_{su}	Setup Time, $\overline{Enable}$ to Clock (Figures 3 and 4)	5	5	–	µs
		10	3.5	–	
		15	2	–	
t_{su}	Setup Time, D_{in} to Clock (Figures 3 and 4)	5	1000	–	ns
		10	750	–	
		15	500	–	
t_h	Hold Time, Clock to $\overline{Enable}$ (Figures 3 and 4)	5	5	–	µs
		10	3.5	–	
		15	2	–	
t_h	Hold Time, Clock to D_{in} (Figures 3 and 4)	5	5	–	µs
		10	3.5	–	
		15	2	–	
t_r, t_f	Input Rise and Fall Times	5-15	–	2	µs
C_{in}	Input Capacitance	5-15	–	7.5	pF

FIGURE 1 — D/A TRANSFER FUNCTION



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of linearity of the actual transfer function from the best-fit straight line. It is normally specified in parts of an LSB.

FIGURE 2 — DEFINITION OF STEP SIZE



$$\text{Step size} = \frac{V_{DD}}{64} \pm 0.75\frac{V_{DD}}{64}$$

(For any adjacent pair of digital numbers)

FIGURE 3 — SERIAL INPUT, POSITIVE CLOCK

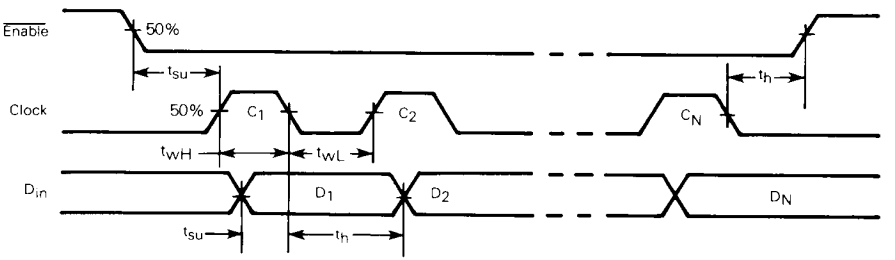
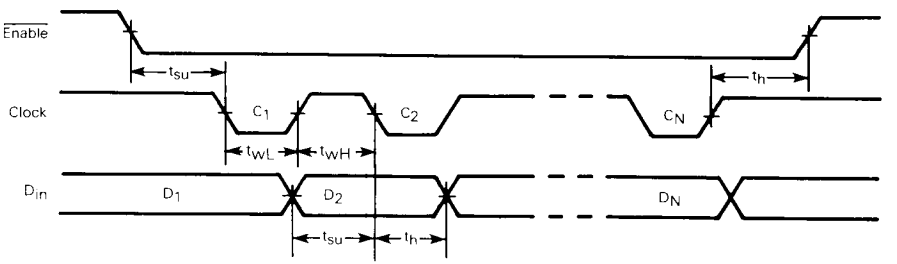


FIGURE 4 — SERIAL INPUT, NEGATIVE CLOCK



PIN DESCRIPTIONS

INPUTS

D_{in}, DATA INPUT — Six-bit words are entered serially, MSB first, into digital data input, D_{in}. Six words are loaded into the MC144110 during each D/A cycle; four words are loaded into the MC144111.

The last 6-bit word shifted in determines the output level of pins Q1 Out and R1 Out. The next-to-last 6-bit word affects pins Q2 Out and R2 Out, etc.

$\overline{\text{Enable}}$, NEGATIVE LOGIC ENABLE — The $\overline{\text{Enable}}$ pin must be low (active) during the serial load. On the low-to-high transition of $\overline{\text{Enable}}$, data contained in the shift register is loaded into the latch.

Clock, SHIFT REGISTER CLOCK — Data is shifted into the register on the high-to-low transition of Clock. Clock is fed into the D-input of a transparent latch, which is used for inhibiting the clocking of the shift register when Enable is high.

The number of Clock cycles required for the MC144110 is usually 36. The MC144111 usually uses 24 cycles. See Table 1 for additional information.

OUTPUTS

D_{out}, DATA OUTPUT — The digital data output is primarily used for cascading the DACs and may be fed into D_{in} of the next stage.

R1 Out through Rn Out, RESISTOR NETWORK OUTPUTS — These are the R-2R resistor network outputs. These outputs may be fed to high-impedance input FET op amps to bypass the on-chip bipolar transistors. The R value of the resistor network ranges from 7 to 15 kΩ.

Q1 Out through Qn Out, NPN TRANSISTOR OUTPUTS — Buffered DAC outputs utilize an emitter-follower configuration for current-gain, thereby allowing interface to low-impedance circuits.

SUPPLY PINS

V_{SS}, NEGATIVE SUPPLY VOLTAGE — This pin is usually ground.

V_{DD}, POSITIVE SUPPLY VOLTAGE — The voltage applied to this pin is used to scale the analog output swing from 4.5 to 15 volts, peak-to-peak.

TABLE 1 — NUMBER OF CHANNELS vs CLOCKS REQUIRED

Number of Channels Required	Number of Clock Cycles	Outputs Used on MC144110	Outputs Used on MC144111
1	6	Q1/R1	Q1/R1
2	12	Q1/R1, Q2/R2	Q1/R1, Q2/R2
3	18	Q1/R1, Q2/R2, Q3/R3	Q1/R1, Q2/R2, Q3/R3
4	24	Q1/R1, Q2/R2, Q3/R3, Q4/R4	Q1/R1, Q2/R2, Q3/R3, Q4/R4
5	30	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5	Not Applicable
6	36	Q1/R1, Q2/R2, Q3/R3, Q4/R4, Q5/R5, Q6/R6	Not Applicable