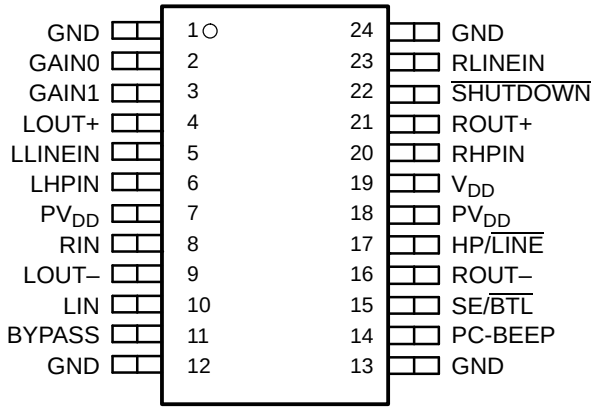
2.6-W STEREO AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS AND MUX CONTROL

FEATURES

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2.6-W/Ch Output Power Into 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA0312 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2.6 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0312 has less than 0.65% THD+N across its specified frequency range. Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of 6 dB, 10 dB, 15.6 dB, and 21.6 dB (inverting) are provided, whereas SE gain is always configured as 4.1 dB for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active, regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0312 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this reduces the gain to 4.1 dB.

The TPA0312 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to 150 µA.

The PowerPAD™ package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0312 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP(1) (PWP)
–40°C to 85°C	TPA0312PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0312PWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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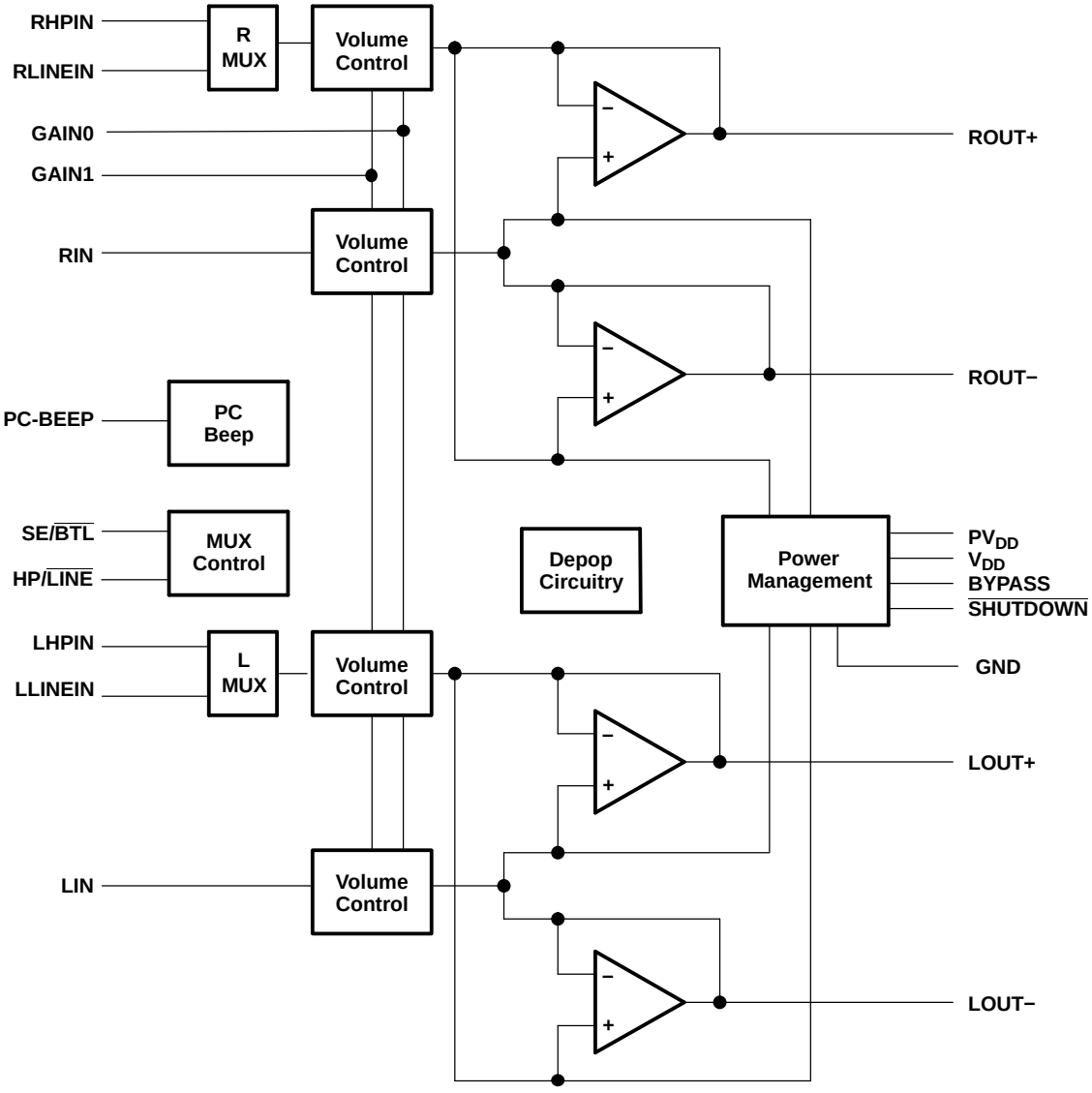
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad.
LHPIN	6	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left-channel positive output in BTL mode and positive output in SE mode
LOUT-	9	O	Left-channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input to PC-BEEP
HP/$\overline{\text{LINE}}$	17	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line inputs (LLINEIN or RLINEIN [5, 23]) are active.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right-channel positive output in BTL mode and positive output in SE mode
ROUT-	16	O	Right-channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
Thermal Pad			Connect to ground. Must be soldered down in all applications to properly secure the device on the PC board.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

V_{DD}	Supply voltage	6 V
V_I	Input voltage	–0.3 V to V_{DD} +0.3 V
	Continuous total power dissipation	Internally limited (see Dissipation Rating Table)
T_A	Operating free-air temperature range	–40°C to 85°C
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 85°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W(1)	21.8 mW/°C	1.7 W	1.4 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* of the before-mentioned document.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, GAIN0, GAIN1	0.8 x V_{DD}		V
		$\overline{\text{SHUTDOWN}}$	2		
V_{IL}	Low-level input voltage	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		0.6 x V_{DD}	V
		GAIN0, GAIN1		0.4 x V_{DD}	
		$\overline{\text{SHUTDOWN}}$		0.8	
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I = 0, A_v = 6 dB			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.5 V to 5.5 V		77		dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current	BTL mode		6	10	mA
		SE mode		3	5	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω , Gain = 6 dB, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	R_L = 3 Ω	THD + N= 10%		2.6		W
			THD + N = 1%,		2.05		
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.65%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		72		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		20		μV_{RMS}
			SE mode		18		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4-6, 9-11, 14-16, 18
		vs Frequency	2, 3, 7, 8, 12, 13, 17, 19
		vs Output voltage	20
V_n	Output noise voltage	vs Bandwidth	21
	Supply ripple rejection ratio	vs Frequency	22, 23
	Crosstalk	vs Frequency	24, 25
	Shutdown attenuation	vs Frequency	26
SNR	Signal-to-noise ratio	vs Frequency	27
	Closed-loop response		28-30
P_O	Output power	vs Load resistance	31, 32
P_D	Power dissipation	vs Output power	33, 34
		vs Ambient temperature	35

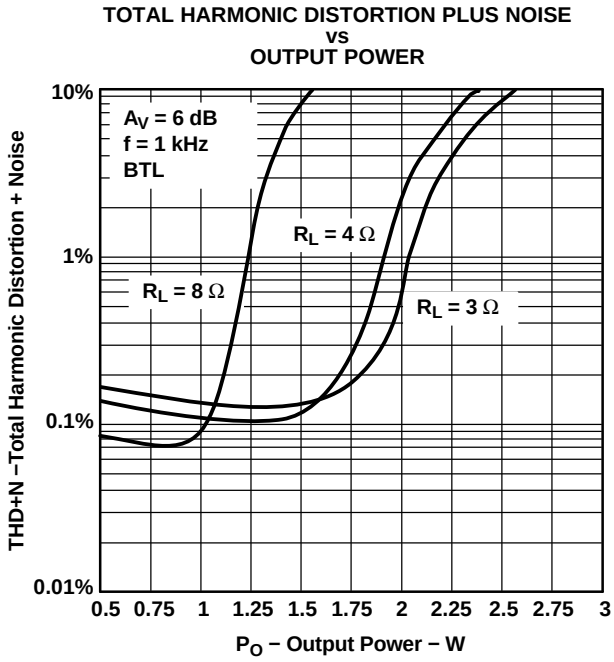
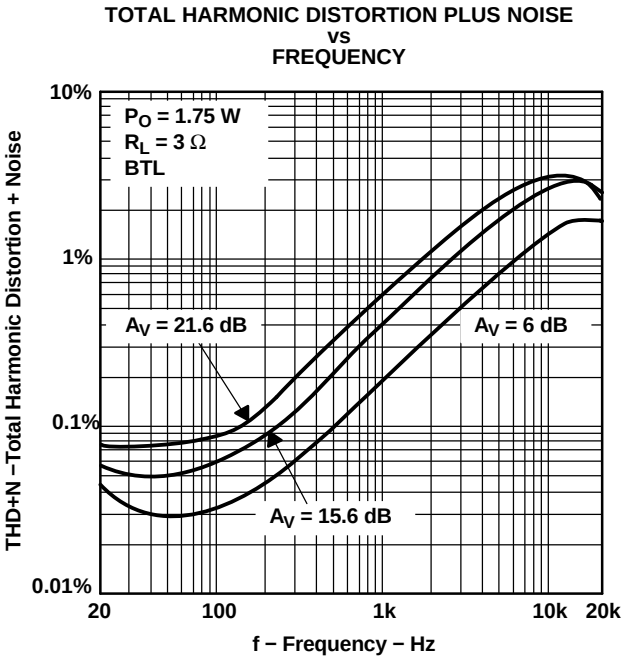


Figure 1.



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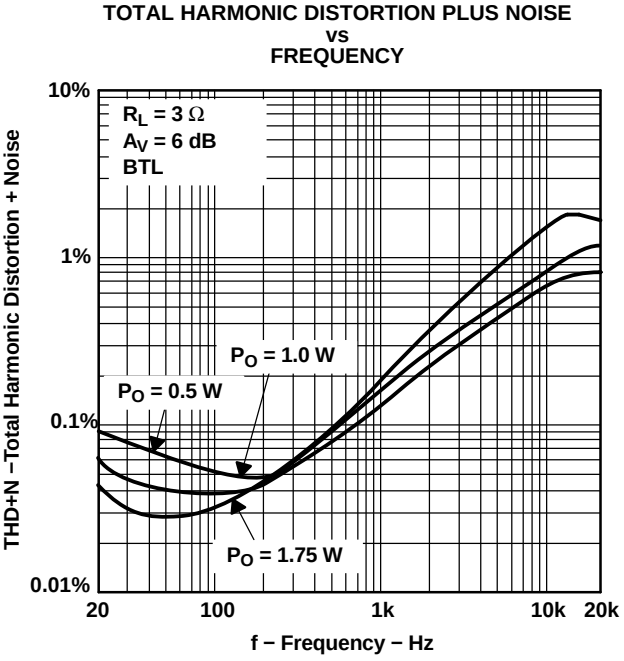

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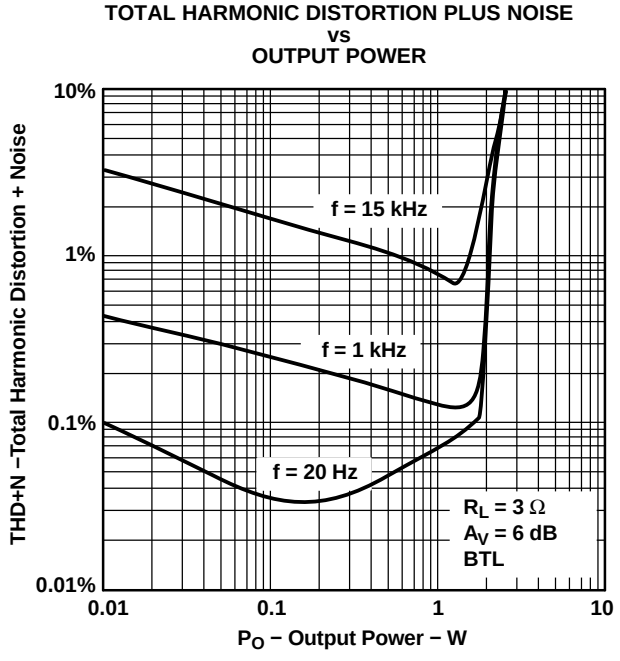

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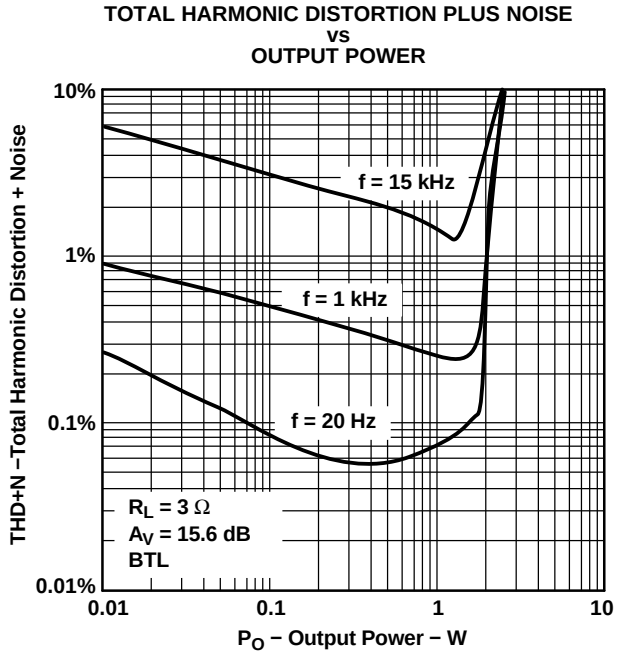

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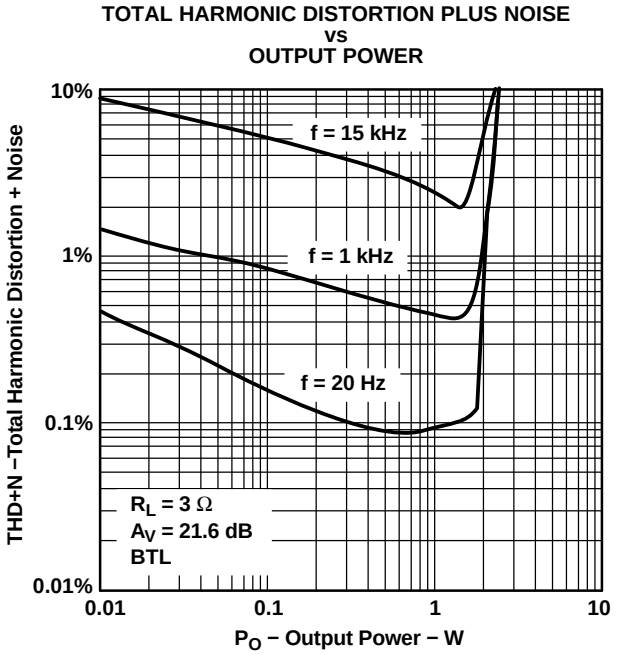

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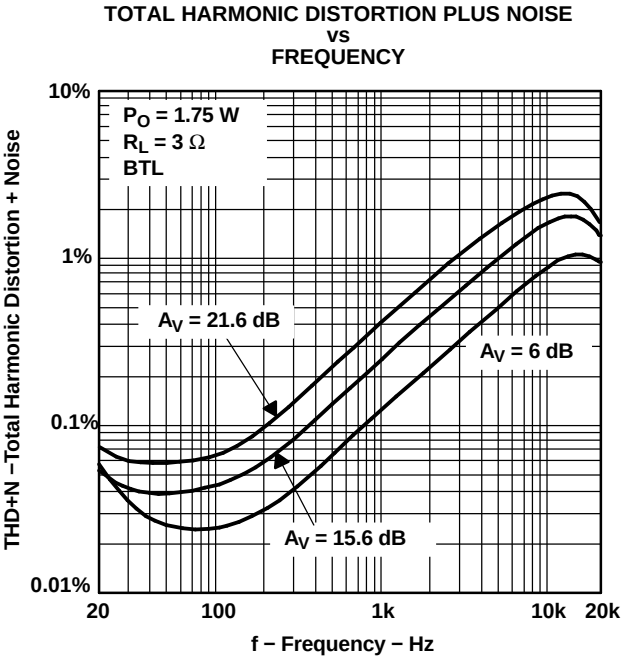

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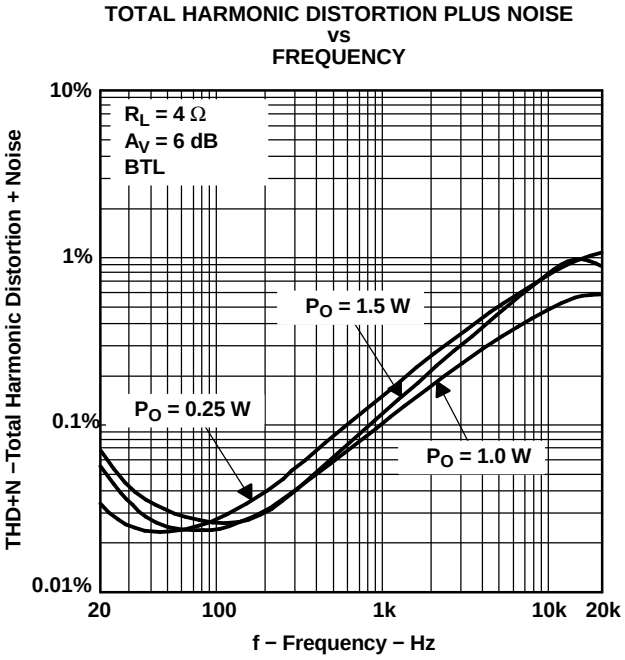

Figure 8.

TEXAS INSTRUMENTS
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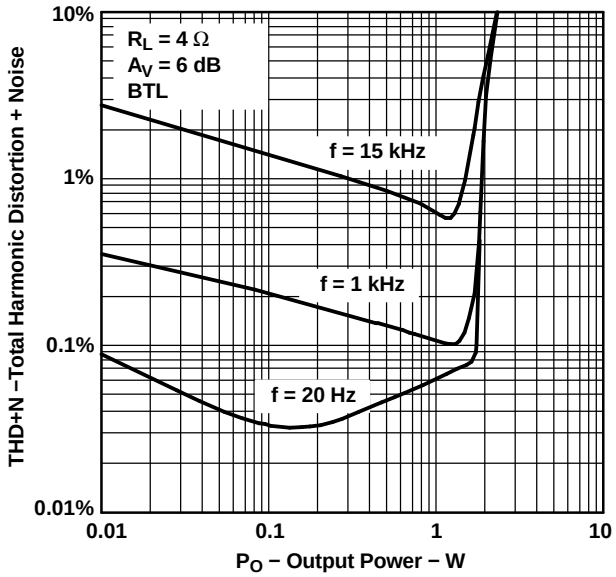
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER



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TOTAL HARMONIC DISTORTION PLUS NOISE
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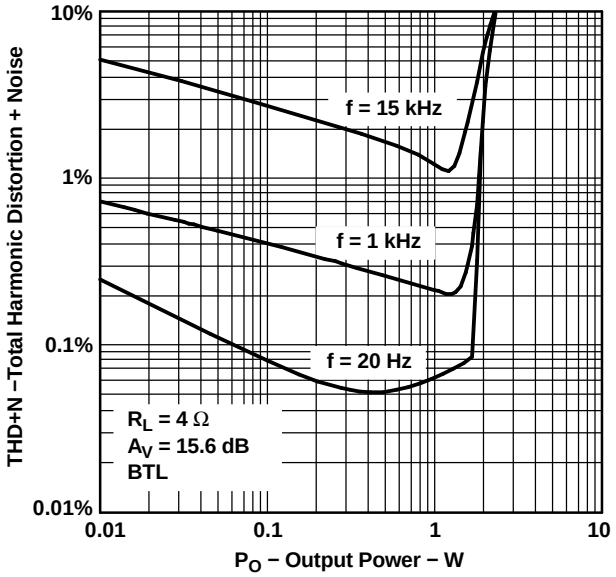

Figure 10.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

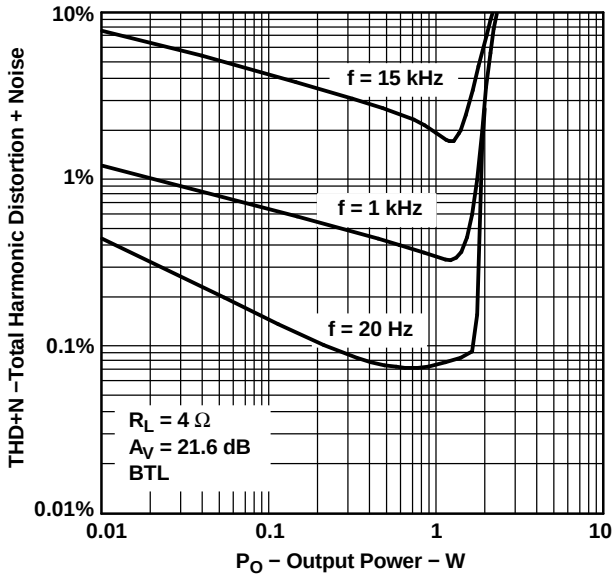

Figure 11.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

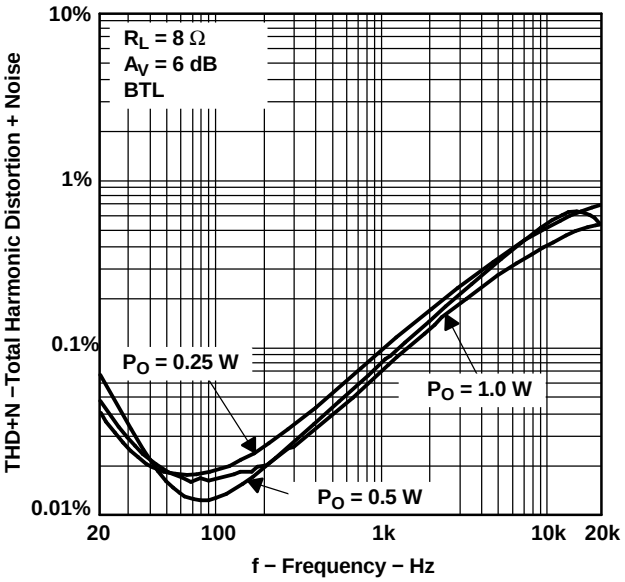

Figure 12.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

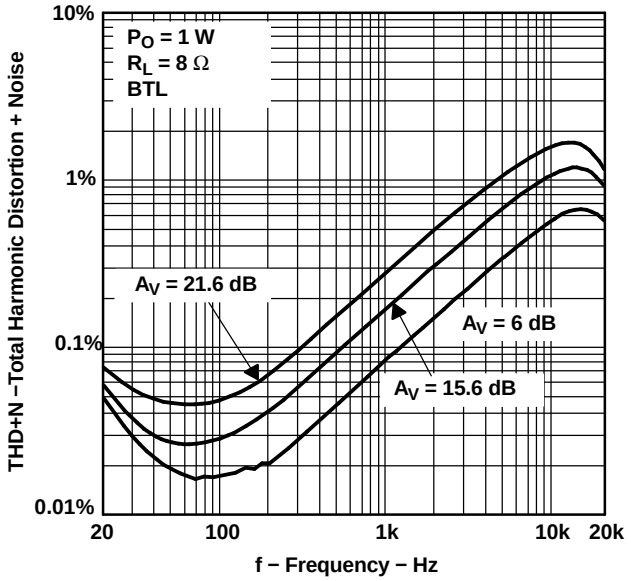

Figure 13.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

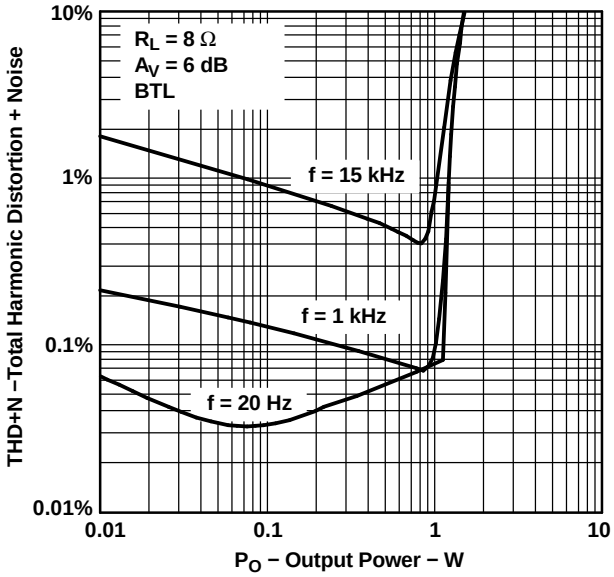

Figure 14.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

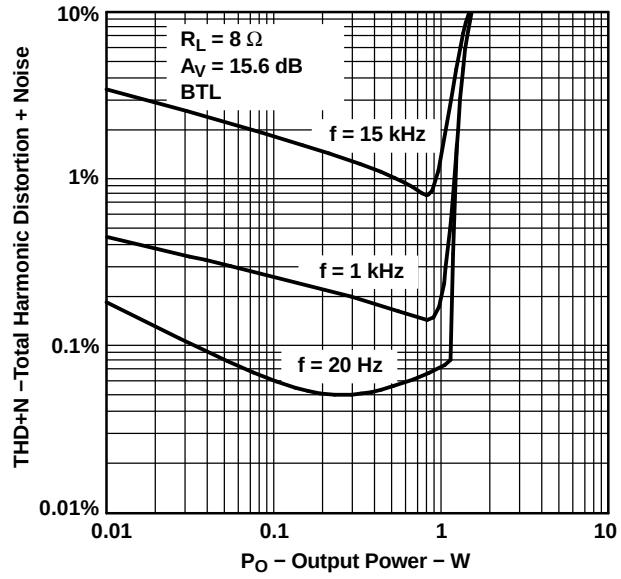

Figure 15.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

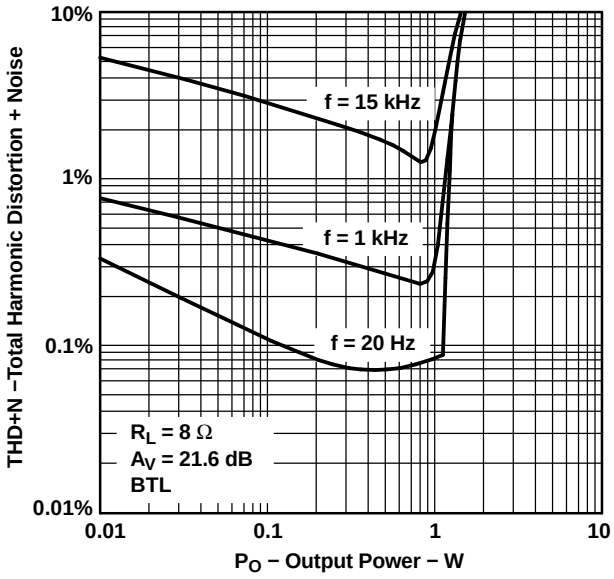

Figure 16.

TEXAS INSTRUMENTS
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TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

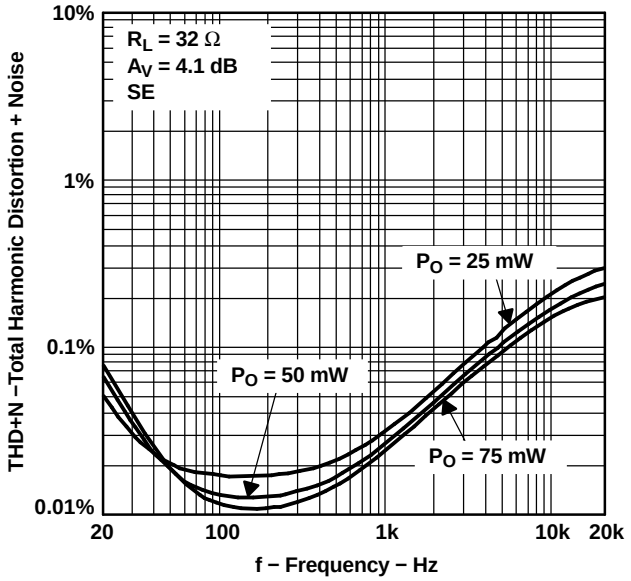


Figure 17.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

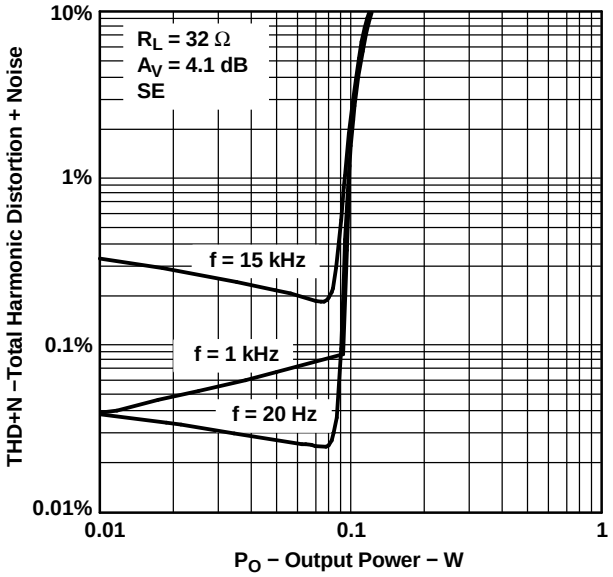


Figure 18.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

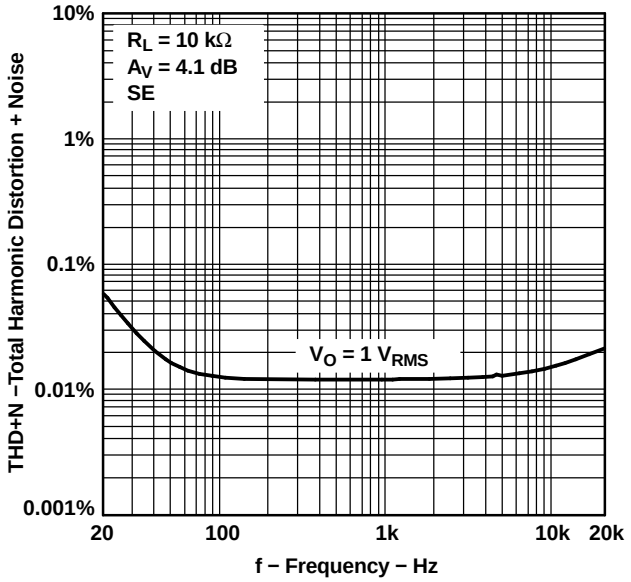
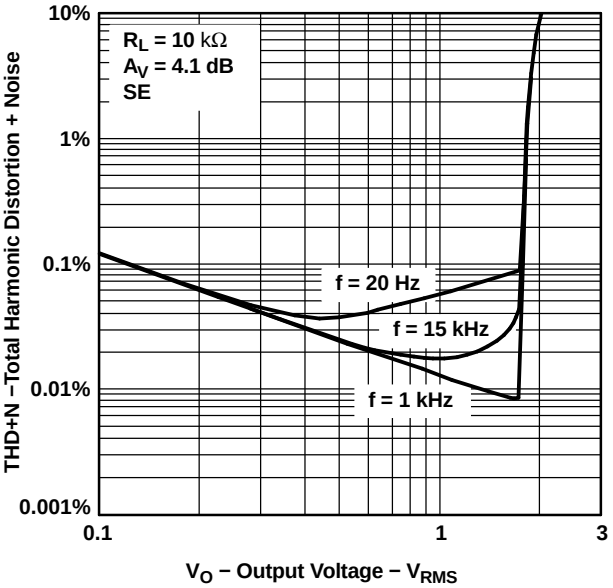


Figure 19.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT VOLTAGE



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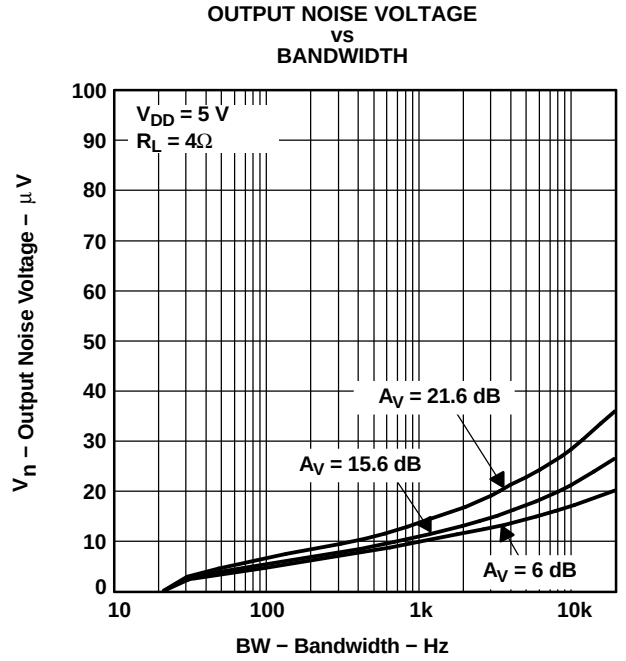

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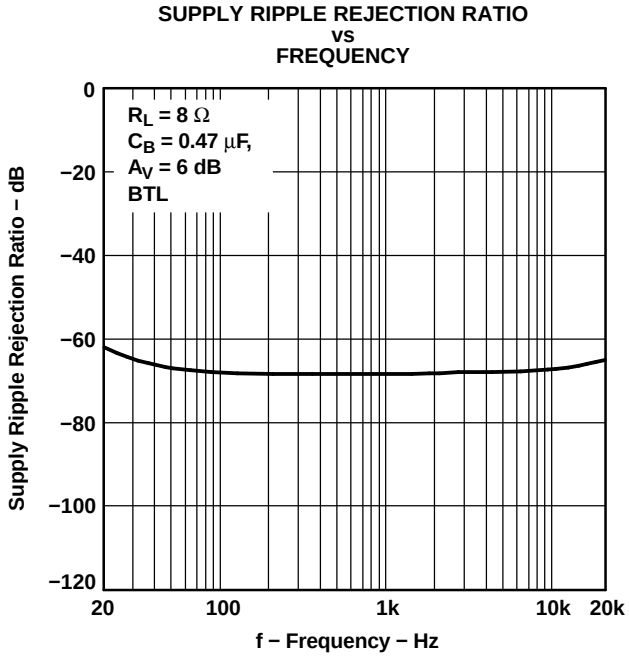

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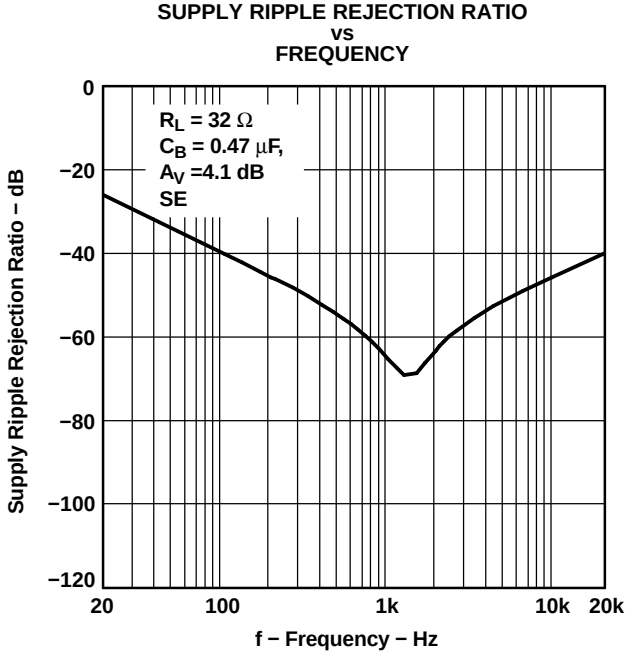

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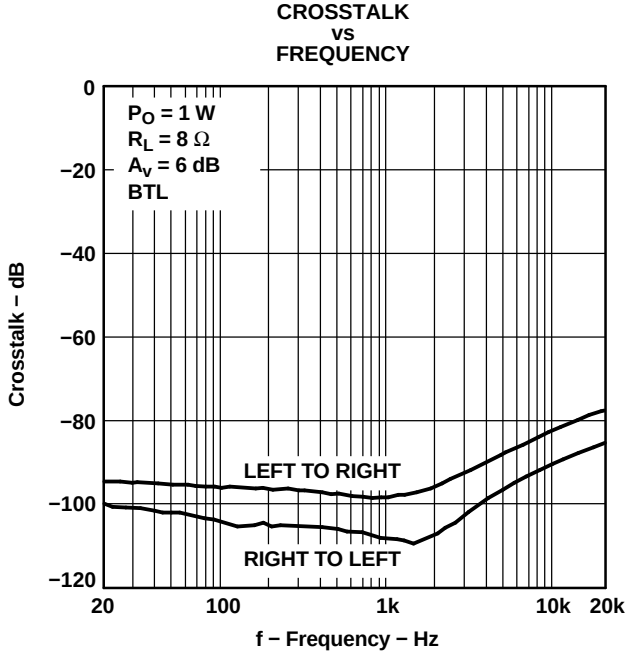

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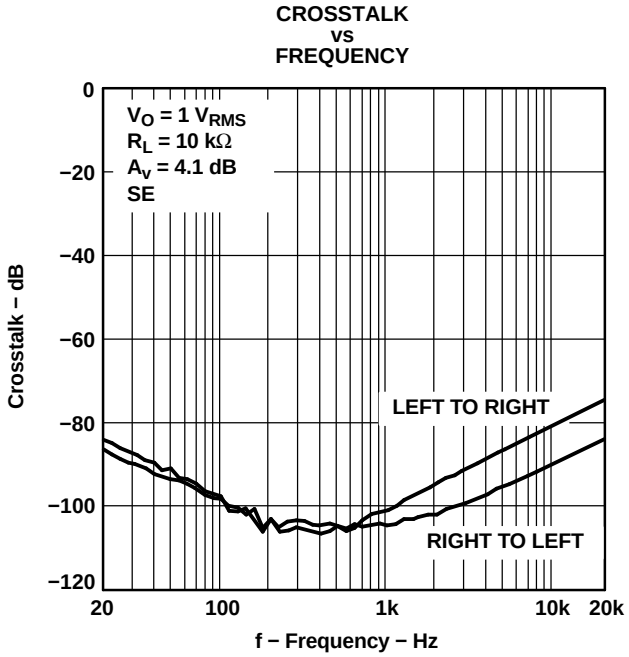

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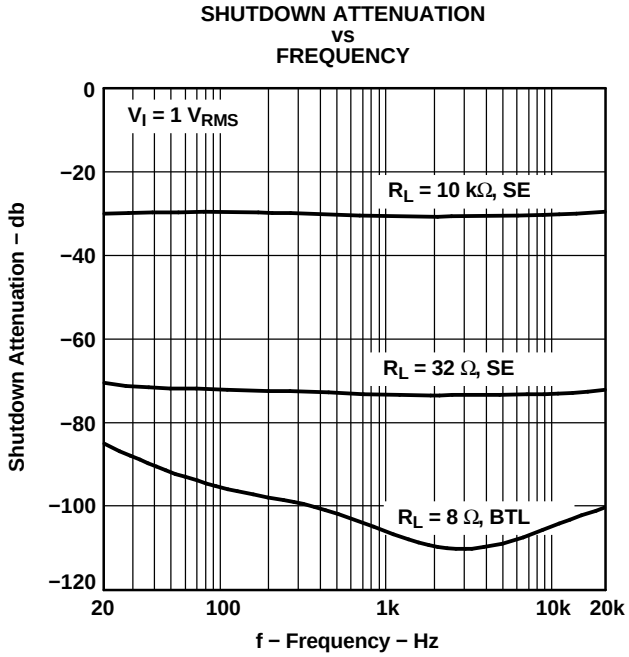

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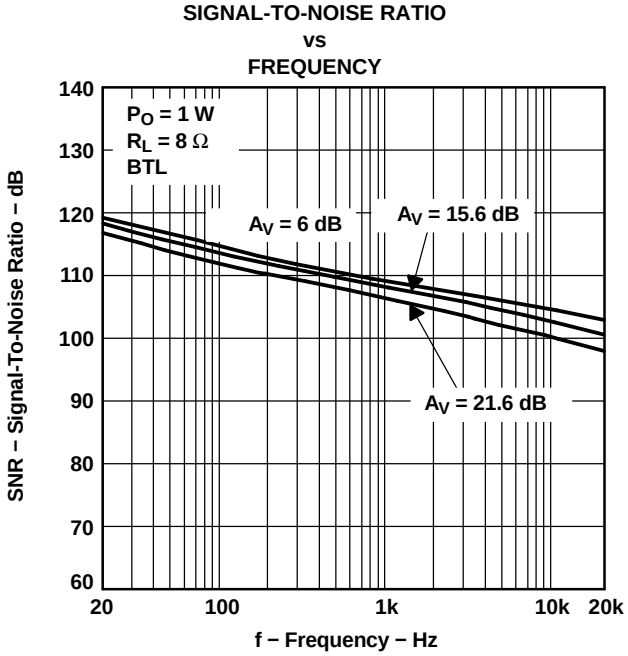

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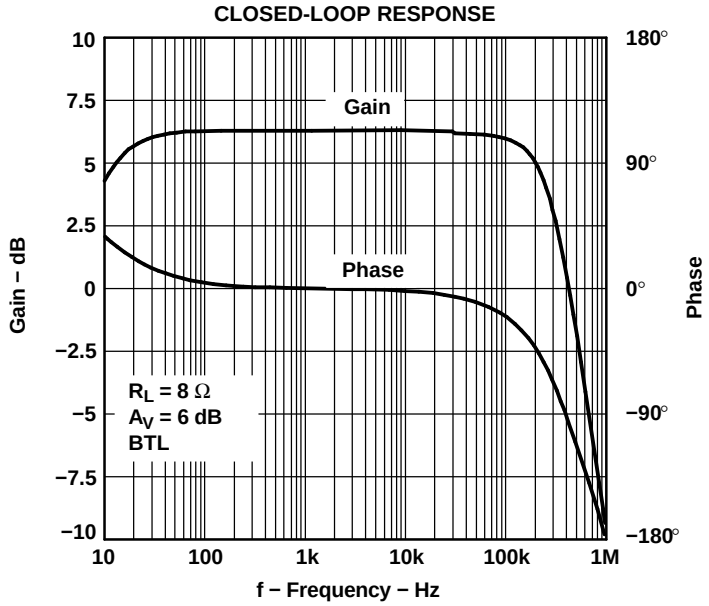

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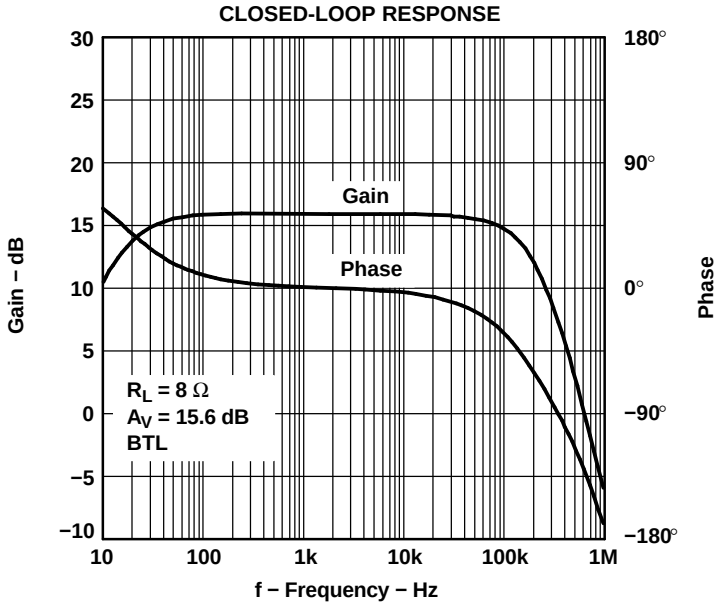

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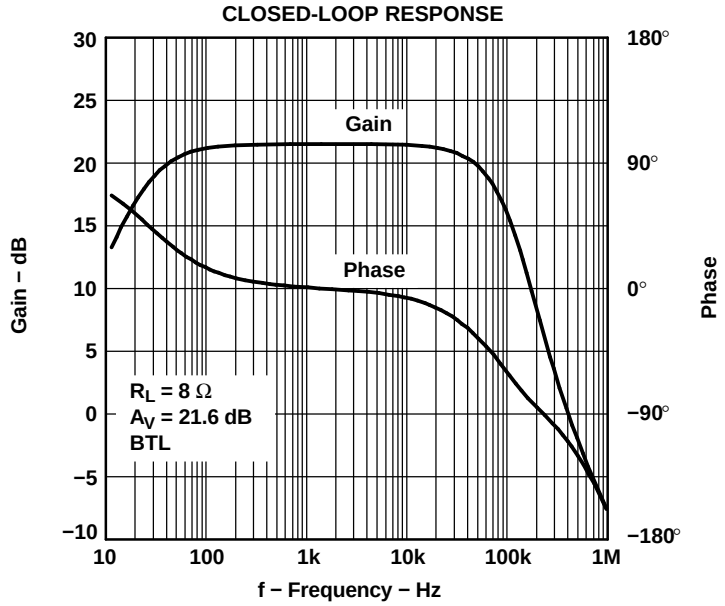

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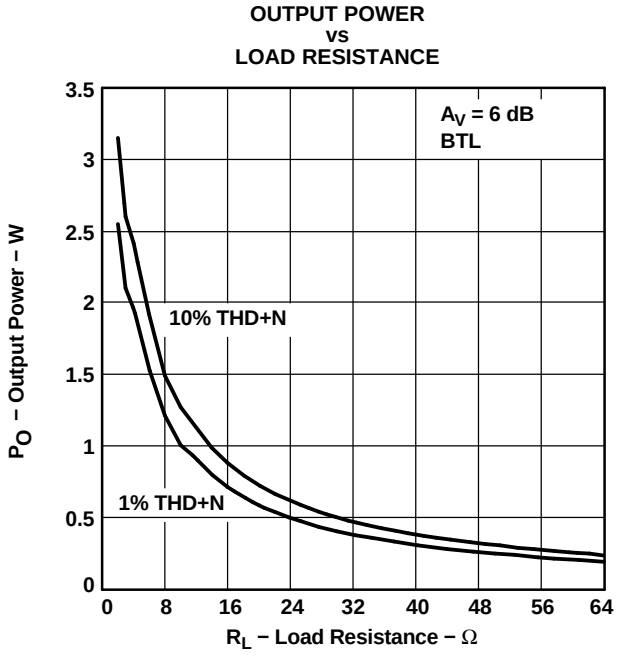

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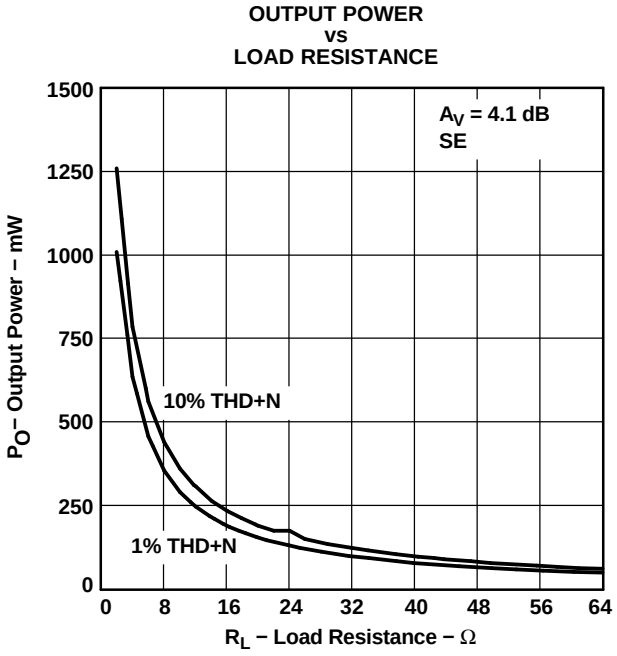

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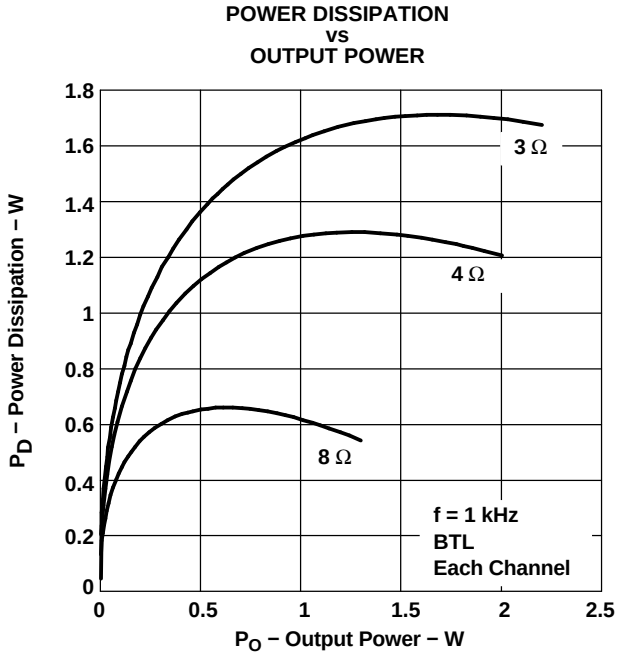

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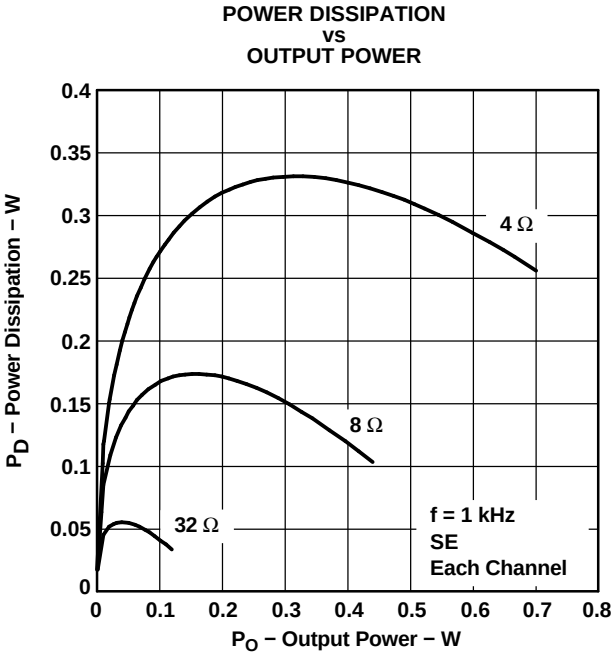

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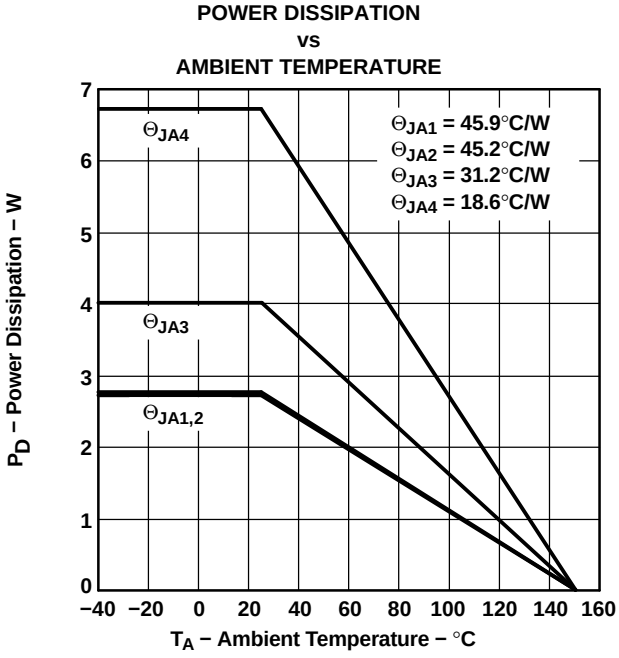


Figure 35.

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 36) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the low profile (< 2 mm) requirements of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power, surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD™ package (thermally enhanced TSSOP) combines fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD™ package is designed to optimize the heat transfer to the PWB. Because of the small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

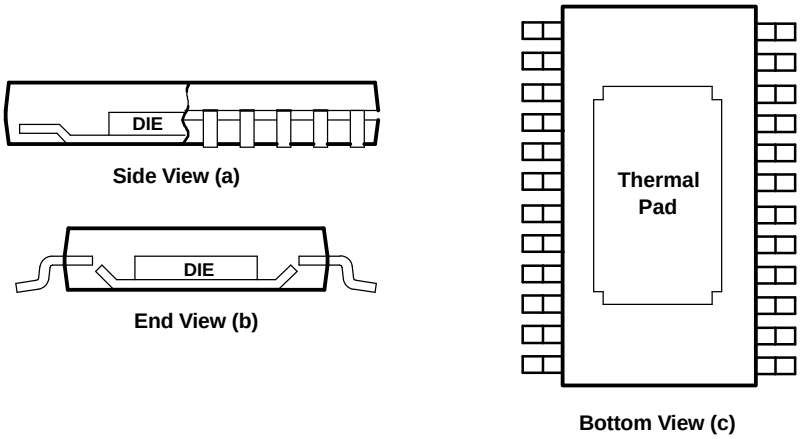
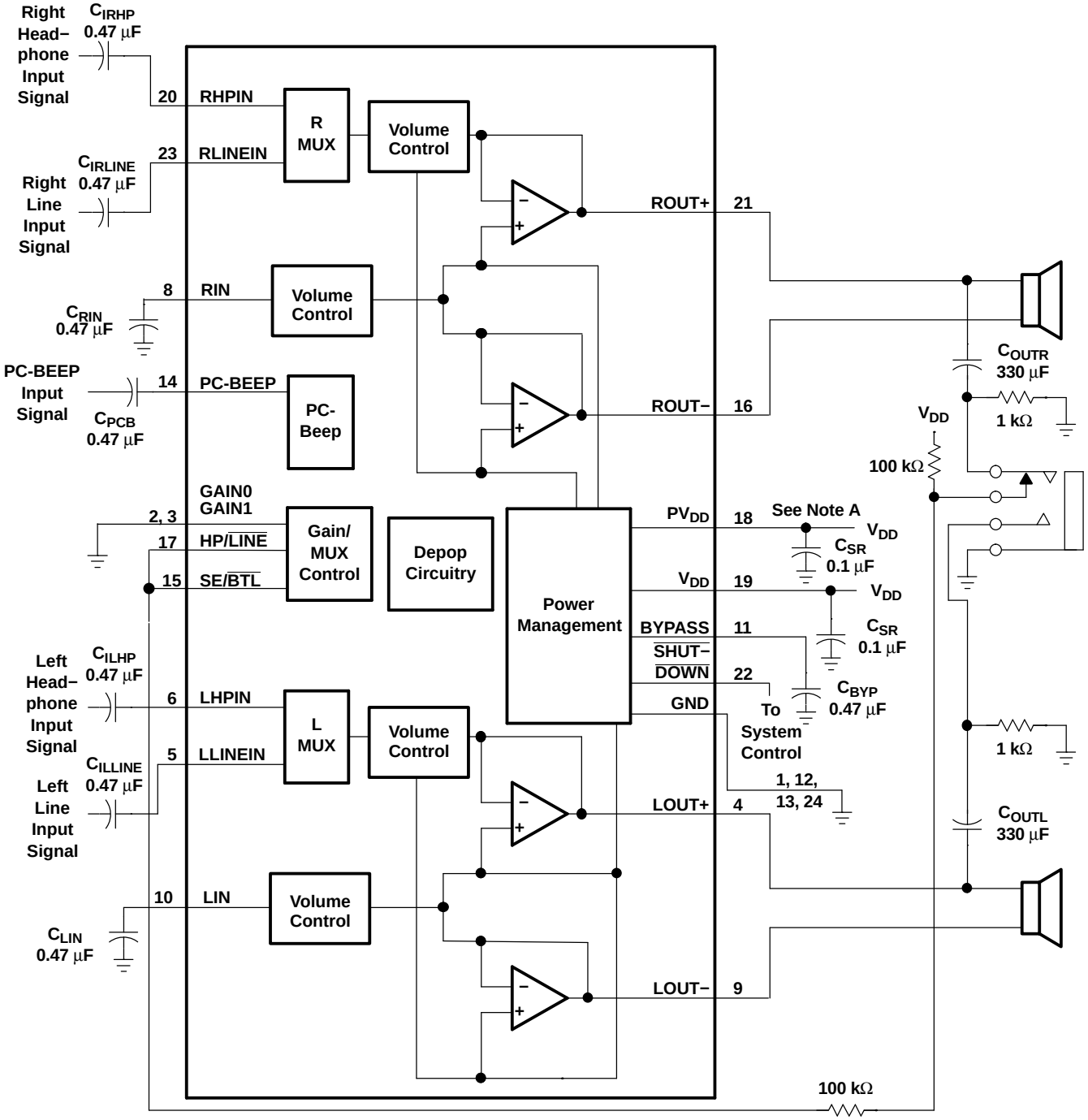


Figure 36. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

SELECTION OF COMPONENTS

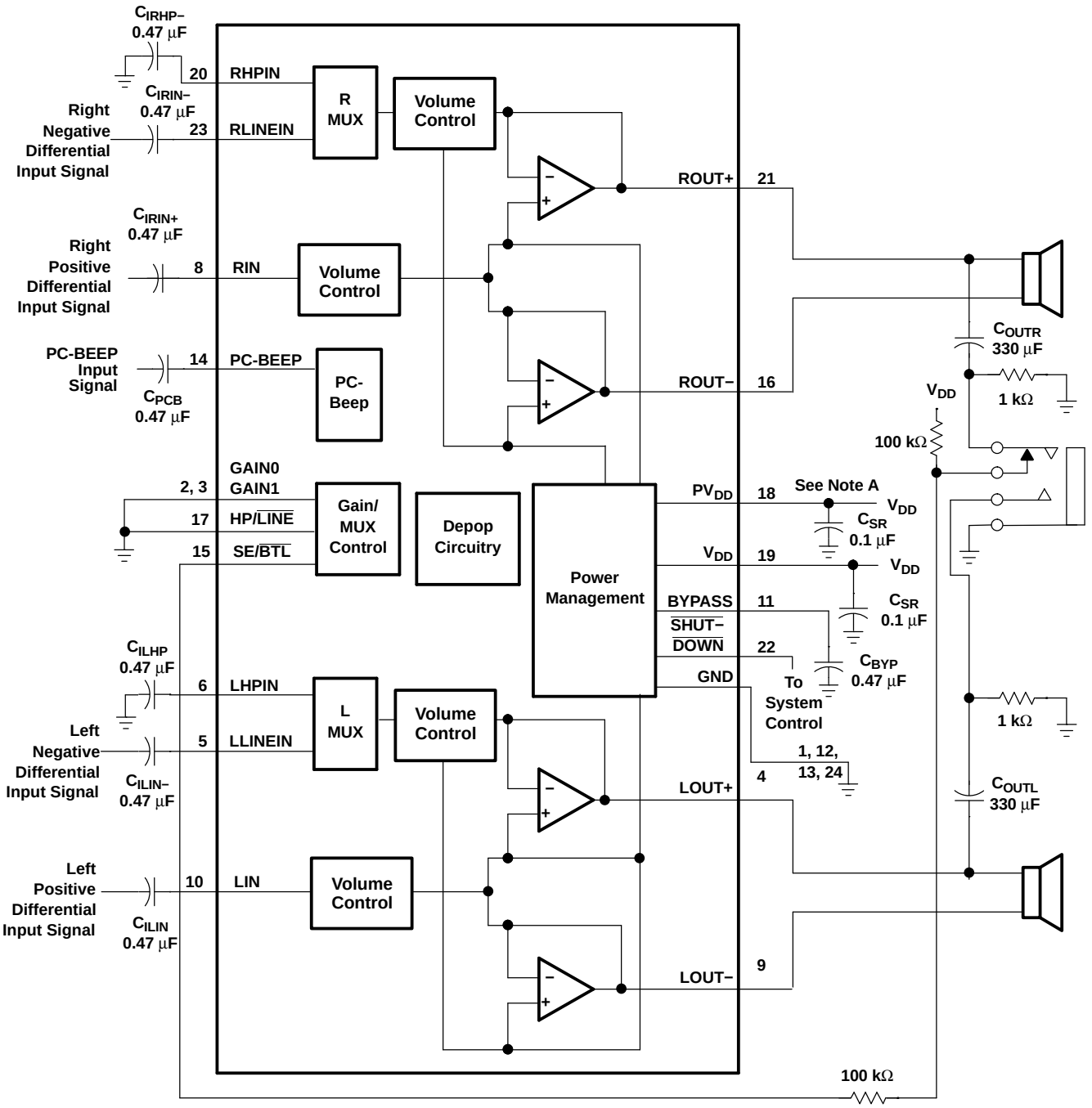
Figure 37 and Figure 38 are schematic diagrams of typical notebook computer application circuits.



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 37. Typical TPA0312 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION (continued)



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 38. Typical TPA0312 Application Circuit Using Differential Inputs

GAIN SETTING VIA GAIN0 AND GAIN1 INPUTS

The gain of the TPA0312 is set by two input terminals, GAIN0 and GAIN1.

Table 1. GAIN SETTINGS

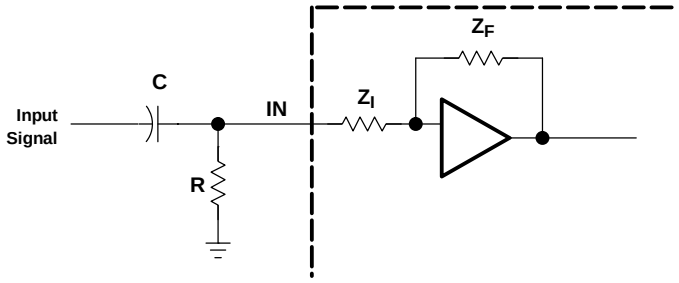
GAIN0	GAIN1	SE/$\overline{\text{BTL}}$	A_V
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependant on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA0312. At the lower gain settings, the input impedance could increase as high as 115 kΩ.

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3-dB or cutoff frequency also changes by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the following figure, the variation of the cutoff frequency is much reduced.



The typical input impedance at each gain setting is given in the table below:

A_v	Z_I
21.6 dB	25 kΩ
15.6 dB	45 kΩ
10 dB	70 kΩ
6 dB	90 kΩ

The –3-dB frequency can be calculated using Equation 1:

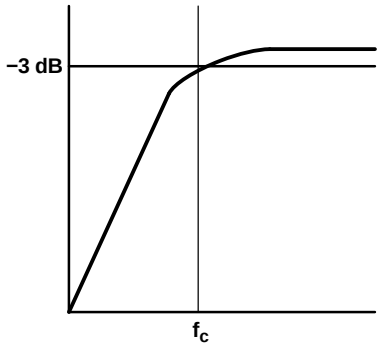
$$f_{-3\ \text{dB}} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \tag{1}$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

INPUT CAPACITOR, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in Equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I}$$



(2)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 26 kΩ and the specification calls for a flat bass response down to 65 Hz. Equation 2 is reconfigured as Equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 94 nF; so, one would likely choose a value in the range of 0.1 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, C_S

The TPA0312 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_{BYP}

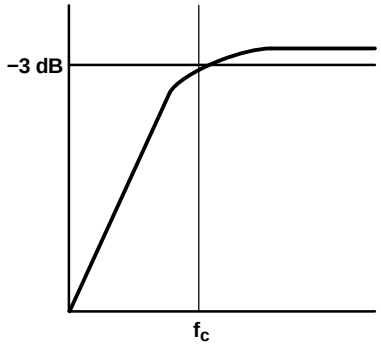
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. COMMON LOAD IMPEDANCES VS LOW FREQUENCY OUTPUT CHARACTERISTICS IN SE MODE

R_L (Ω)	C_C (µF)	LOWEST FREQUENCY(Hz)
3	330	161
4	330	120
8	330	60
32	330	15
10,000	330	0.05
47,000	330	0.01

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo, for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

BRIDGE-TIED LOAD VERSUS SINGLE-ENDED MODE

Figure 39 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0312 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground-referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \tag{5}$$

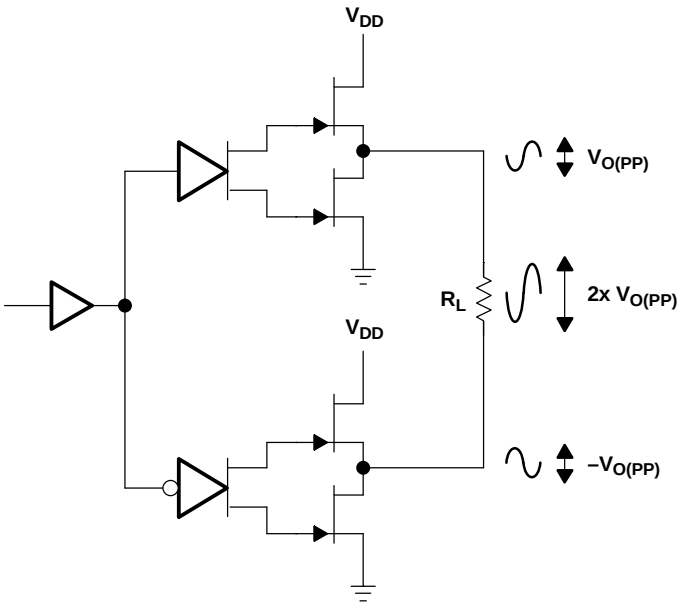


Figure 39. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 40. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF); so, they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{6}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

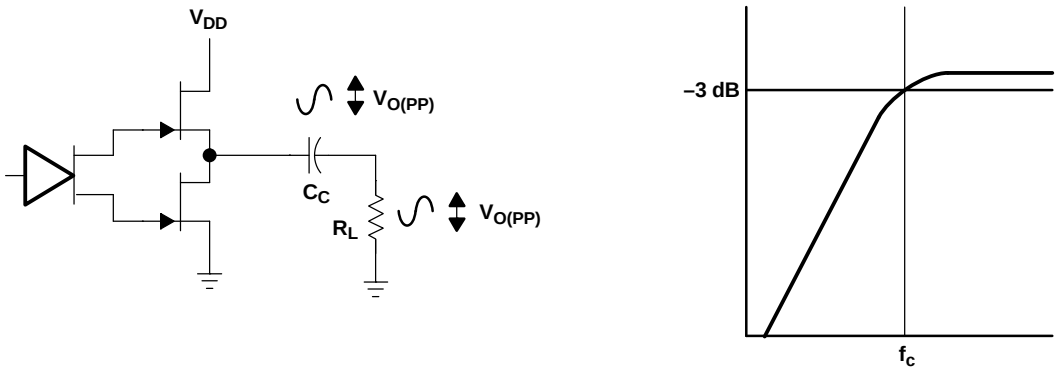


Figure 40. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *Crest Factor and Thermal Considerations* section.

SINGLE-ENDED OPERATION

In SE mode the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 4.1 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sine-wave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 41).

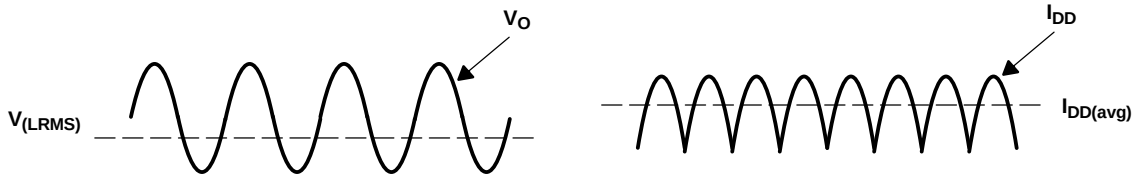


Figure 41. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into Equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

$$V_P = \sqrt{2\, P_L\, R_L} \tag{7}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\, \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

Table 3 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half-power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. EFFICIENCY VS OUTPUT POWER IN 5-V, 8-Ω, BTL SYSTEMS

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in Equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA0312 data sheet, one can see that when the TPA0312 is operating from a 5-V supply into a 3-Ω speaker, 4-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\,\text{Log}\,\frac{P_W}{P_{ref}} = 10\text{Log}\,\frac{4\ W}{1\ W} = 6\ \text{dB} \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 6 dB - 15 dB = -9 dB (15-dB crest factor)
- 6 dB - 12 dB = -6 dB (12-dB crest factor)
- 6 dB - 9 dB = -3 dB (9-dB crest factor)
- 6 dB - 6 dB = 0 dB (6-dB crest factor)
- 6 dB - 3 dB = 3 dB (3-dB crest factor)

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{PdB/10} \times P_{ref} \\ &= 63\ \text{mW (18−dB crest factor)} \\ &= 125\ \text{mW (15−dB crest factor)} \\ &= 250\ \text{mW (9−dB crest factor)} \\ &= 500\ \text{mW (6−dB crest factor)} \\ &= 1000\ \text{mW (3−dB crest factor)} \\ &= 2000\ \text{mW (15−dB crest factor)} \end{aligned} \tag{10}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0312 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0312 POWER RATING, 5-V, 3-Ω, STEREO

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE(1)
4	2 W (3 dB)	1.7	-3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	85°C

(1) Package limited to 85°C ambient

Table 5. TPA0312 POWER RATING, 5-V, 8-Ω, STEREO

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE(1)
2.5 W	1250 mW (3-dB crest factor)	0.55	85°C
2.5 W	1000 mW (4-dB crest factor)	0.62	85°C
2.5 W	500 mW (7-dB crest factor)	0.59	85°C
2.5 W	250 mW (10-dB crest factor)	0.53	85°C

(1) Package limited to 85°C ambient

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for a 3-Ω load than for an 8-Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for a 3-Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of an 8-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for an 8-Ω load, but do not exceed the maximum ambient temperature of 85°C.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0312 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\,\text{Max} &= T_J\,\text{Max} - \Theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96°C\ (15\text{–dB crest factor}) \end{aligned} \tag{13}$$

NOTE:

Internal dissipation of 0.6 W is estimated for a 2.6-W system with 15-dB crest factor per channel. Package limited to 85°C

Table 4 and Table 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0312 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 and Table 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA0312 to easily switch between BTL and SE modes is one of its most important cost-saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0312, two separate amplifiers drive OUT+ and OUT-. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT- and ROUT- (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0312 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high-output impedance state, which configures the TPA0312 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 42.

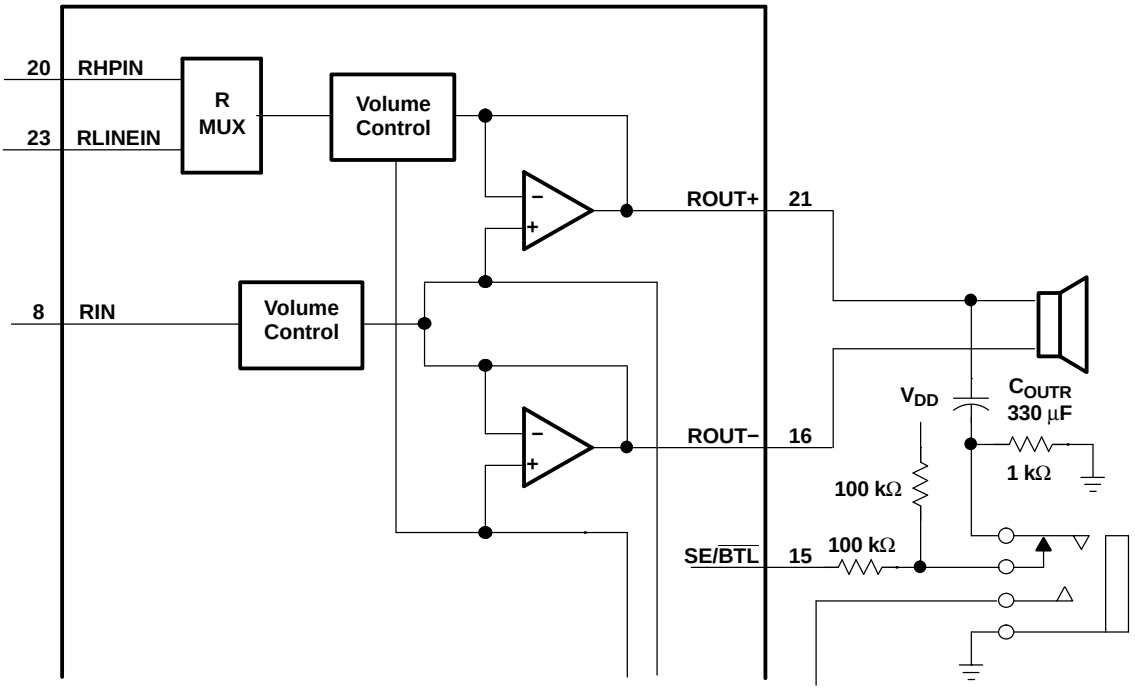


Figure 42. TPA0312 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3,5-mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

INPUT MUX OPERATION

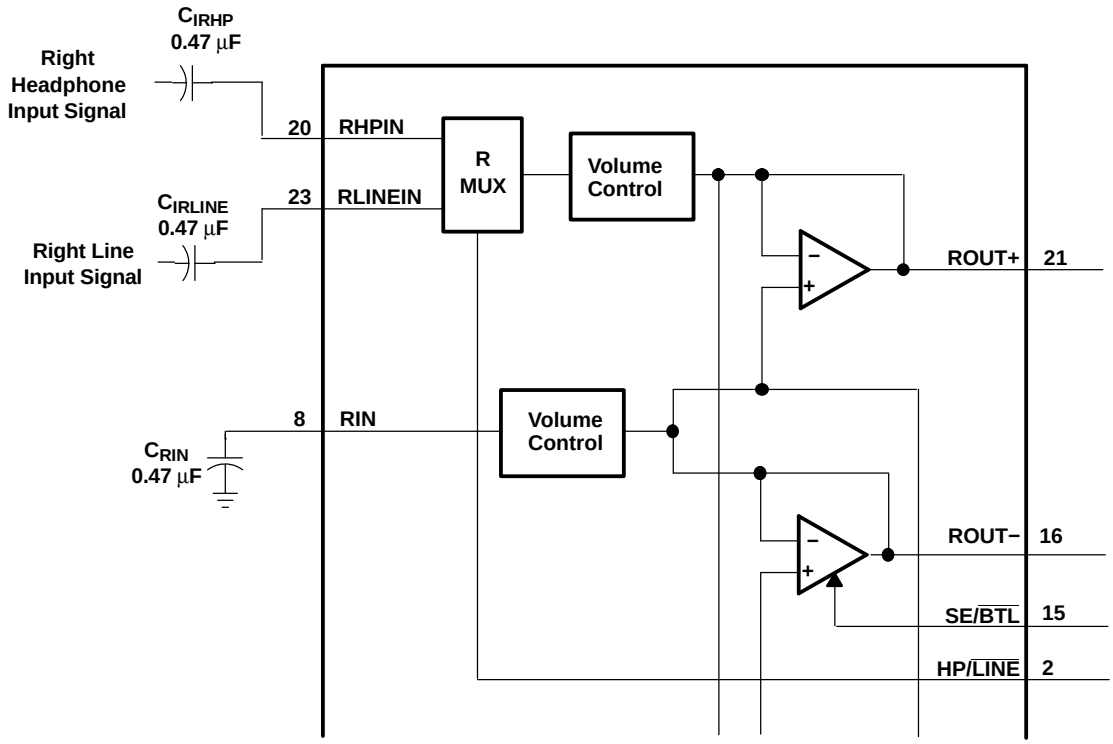


Figure 43. TPA0312 Example Input MUX Circuit

The TPA0312 offers the capability for the designer to use separate headphone inputs (RHPIN, LHPIN) and line inputs (RLINEIN, LLINEIN). The inputs can be different if the input signal is single-ended. If using a differential input signal, the inputs must be the same because the inputs share a common RIN, LIN. Although the typical application in Figure 37 shows the input mux control signal HP/LINE tied to SE/BTL, that configuration is not required. The input mux can be used to select between two inputs that are used in both SE and BTL modes.

If using the TPA0312 with a single-ended input, the RIN and LIN terminals must be tied through a capacitor to ground, as shown in Figure 43. RIN and LIN must not be tied to bypass or an offset occurs on the output causing the device to pop when turning on and off.

Input coupling capacitors can be eliminated when using differential inputs, but are used to obtain maximum output power. If the input capacitors are eliminated, the dc offset must match the voltage on BYPASS or the output power is limited.

PC-BEEP OPERATION

The PC-BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC-BEEP input is active, both LINEIN and HPIN inputs are deselected, and both the left and right channels are driven in BTL mode with the signal from PC-BEEP. The gain from the PC-BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC-BEEP input is deselected, the amplifier returns to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC-BEEP takes the device out of shutdown, outputs the PC-BEEP signal, then returns the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train. To be accurately detected, the signal must have a minimum of 1.5-V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of eight rising edges. When the signal is no longer detected, the amplifier returns to its previous operating mode and volume setting.

To ac-couple the PC-BEEP input, choose a coupling-capacitor value to satisfy Equation 14:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC-BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally rests at midrail when no signal is present.

SHUTDOWN MODES

The TPA0312 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 6. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, AND SHUTDOWN FUNCTIONS

INPUTS(1)			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X(2)	X(2)	Low	X(2)	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Inputs should never be left unconnected.
(2) X = do not care

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA0312PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0312	Samples
TPA0312PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0312	Samples
TPA0312PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0312	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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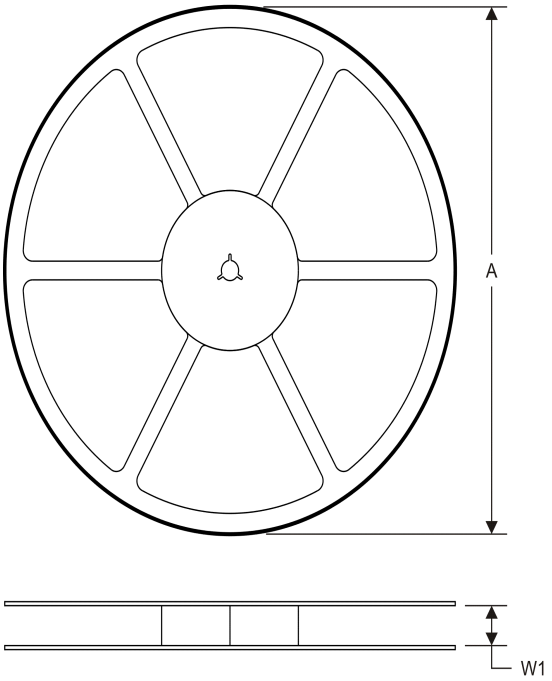
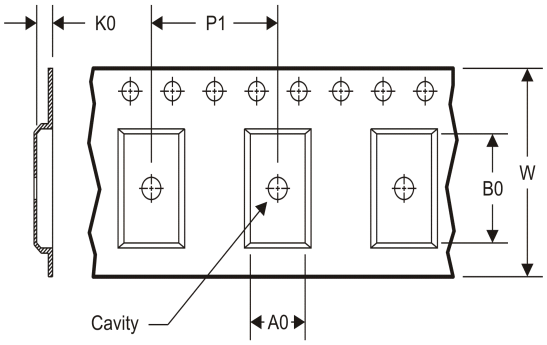
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



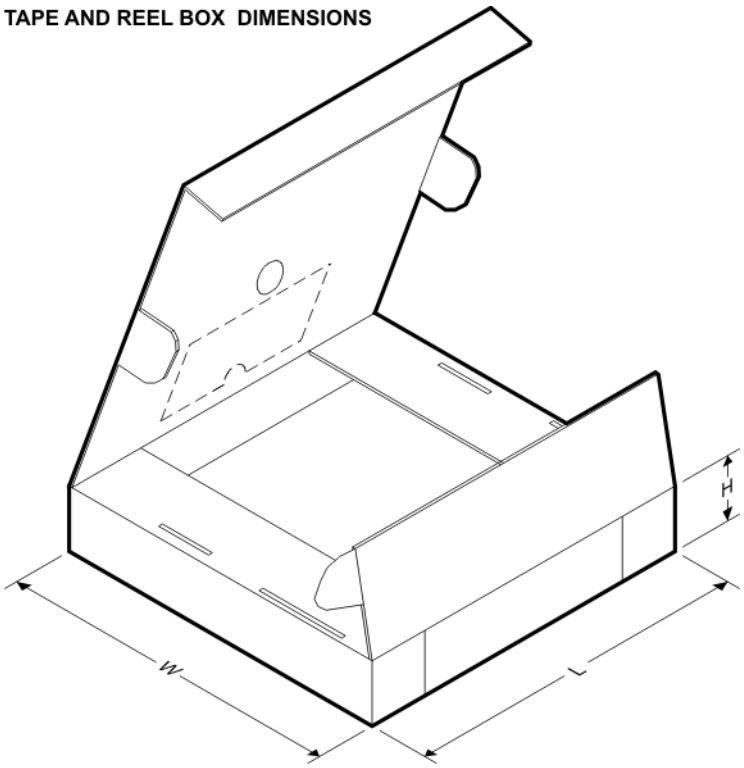
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0312PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

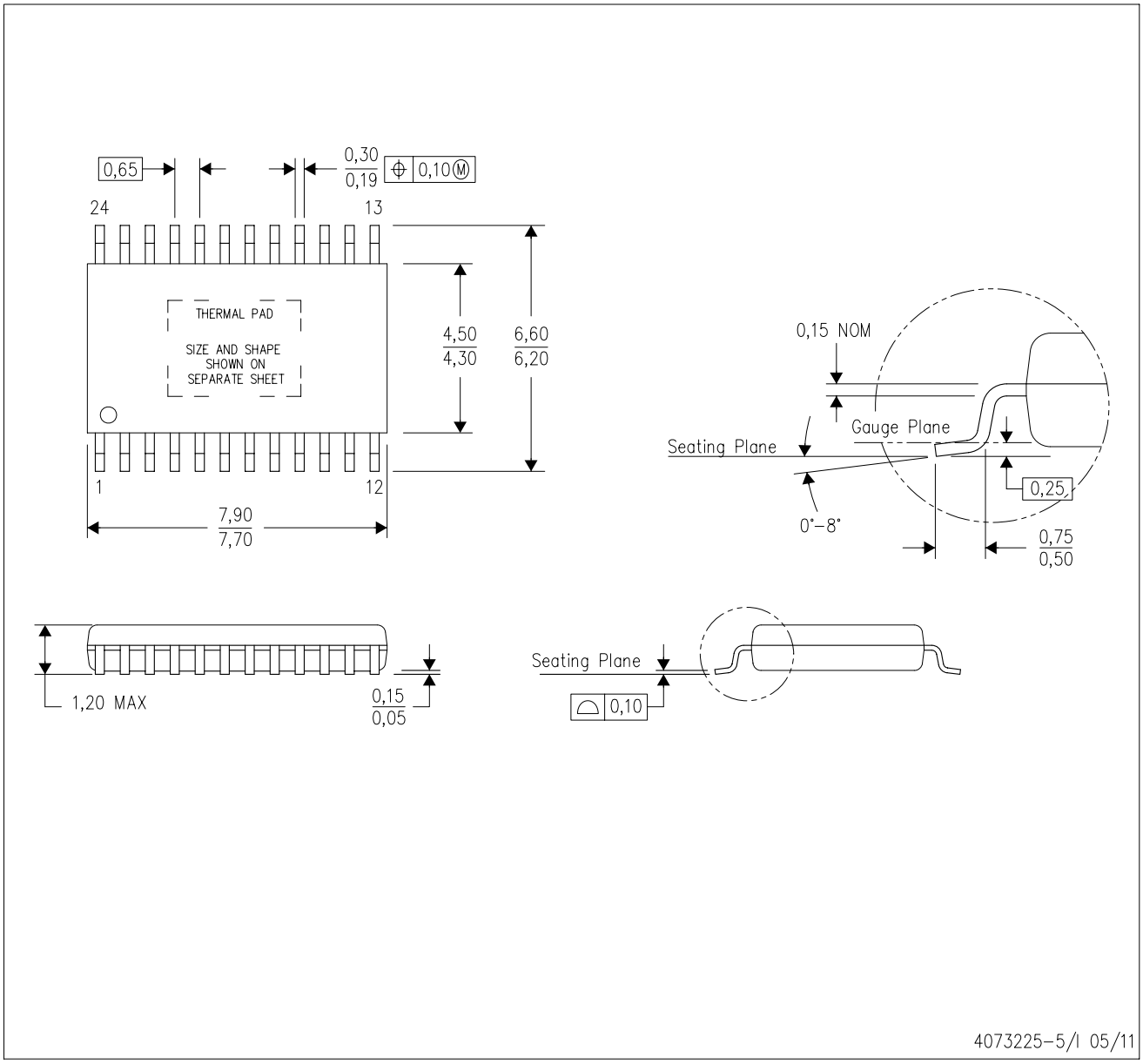
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0312PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

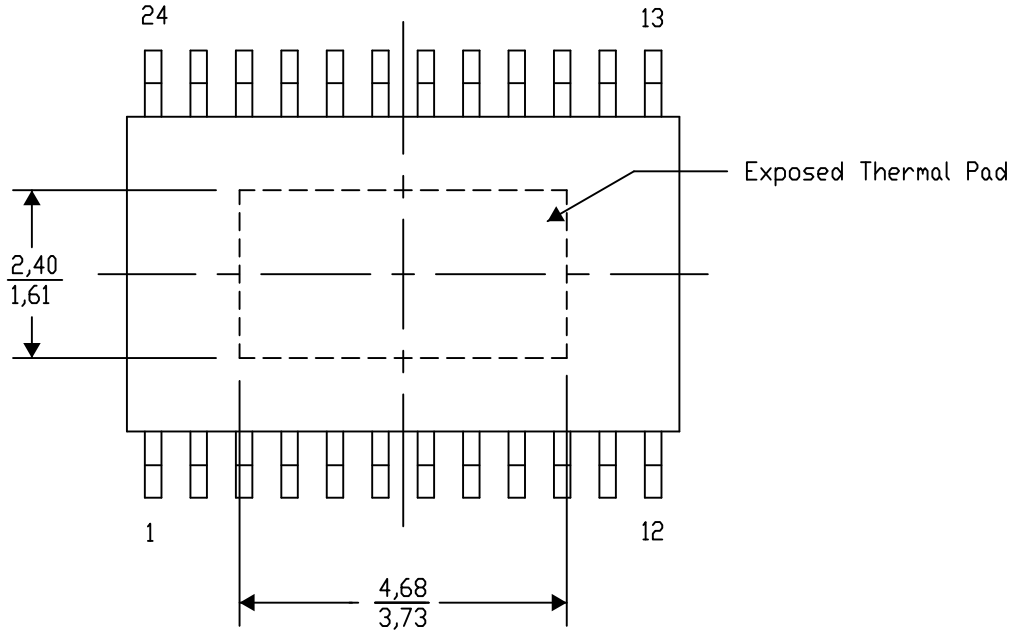
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

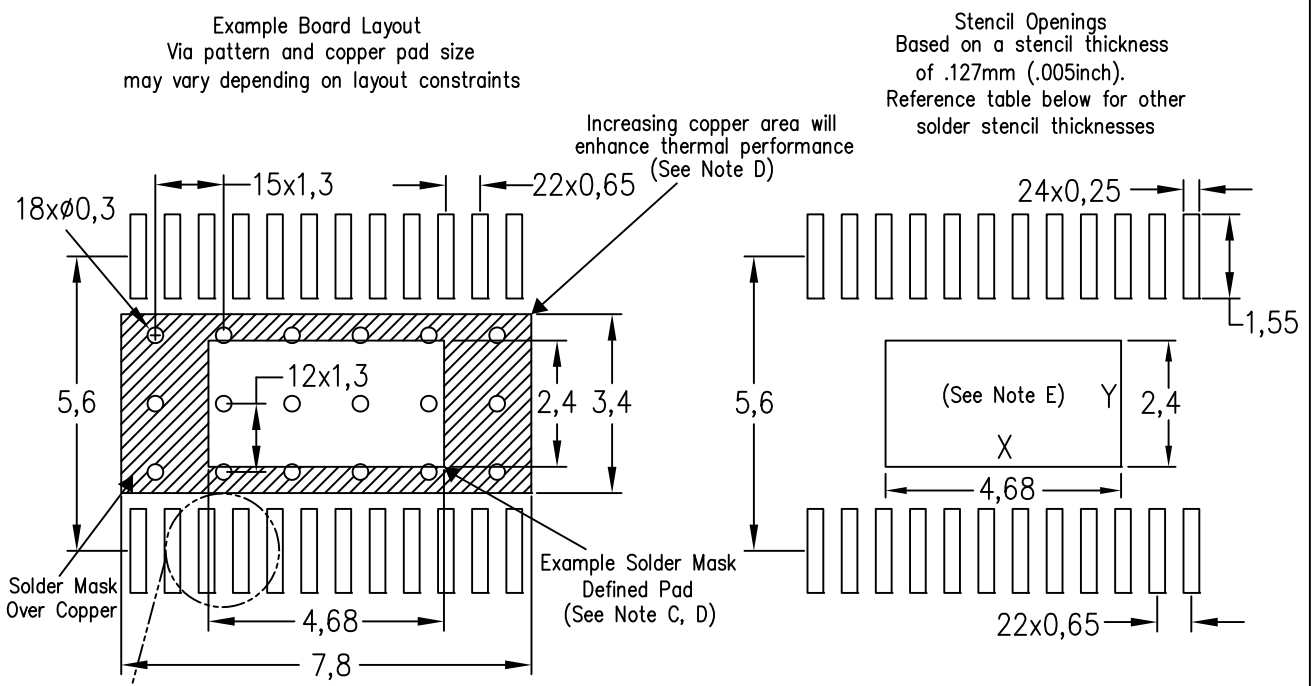
Exposed Thermal Pad Dimensions

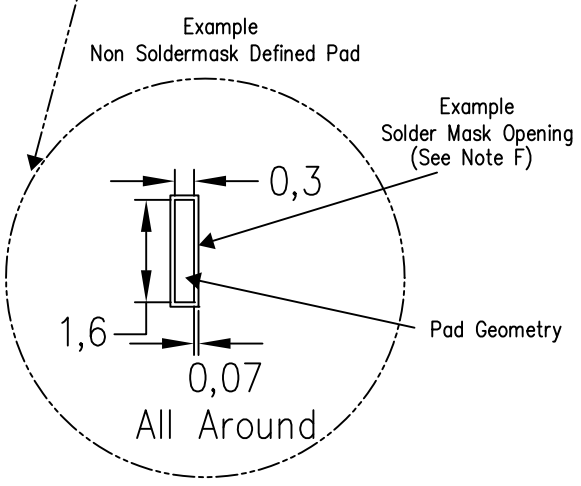
4206332–27/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.0	2.6
0.127mm	4.68	2.4
0.152mm	4.3	2.2
0.178mm	4.2	2.1

4207609–14/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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