

RoHS Compliant

SATA-Disk Module 3

Specifications for 7P/90D

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Version 1.2



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SATA-Disk Module 3

AP-SDMxxxxCAANS-XXTX

Features:

- **Standard Serial ATA 2.6 (Gen. 2)**
 - Serial ATA 2.6 (Gen. 2)
 - SATA II, 3.0 Gbps
 - ATA-compatible command set
- **Capacities**
 - 512 MB, 1, 2, 4 GB
- **Performance***
 - Burst read/write: 300 MB/sec
 - Sustained read: up to 30 MB/sec
 - Sustained write: up to 10 MB/sec
- **Intelligent endurance design**
 - Built-in hardware ECC, enabling up to 14/28 bit correction per 1K bytes
 - Static wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
 - Flash bad-block management
 - S.M.A.R.T.
 - Power Failure Management
 - ATA Secure Erase
 - Trim
- **NAND Flash Type: SLC**
- **Zero power data retention**
 - No battery required for data storage
- **Temperature ranges**
 - Operation:
 - Standard: 0°C to 70°C
 - Extended Temperature: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Supply voltage**
 - 5.0 V $\pm$ 5%
- **Low power consumption***
 - Active mode: 205 mA@5.0 V
 - Idle mode: 95 mA@5.0 V
- **Connector type**
 - 7-pin signal connector
 - 2-pin power connector
- **RoHS compliant**

*Varies from capacities, based on 512MB capacity

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1. General Description

Apacer's SATA-Disk Module 3 (SDM3) is a high-performance, embedded SSD designed to replace the conventional SATA hard disk drive. SDM SSD can be plugged into a standard Serial ATA 7-pin connector commonly found in desktops, IT-STB, industrial PC and thin client systems. Moreover, Apacer provides an innovative way for design-in customers to strengthen the vibration-resistance between SDM3 and mainboard.

Apacer's SDM3 has a built-in microcontroller with file management firmware that communicates with SATA standard interface. This means SDM3 does not require additional or proprietary host software such as Flash File System (FFS) and Memory Technology Driver (MTD). This product is well suited for embedded flash storage applications offering new and expanded functionalities as well as more cost-effective designs, better performance and increased reliability.

SDM3 Series is designed to work at 5 Volts and uses a standard SATA driver that complies with major operating systems such as Microsoft's Windows series.

Featuring technologies as Apacer-specific Wear-leveling algorithms, S.M.A.R.T, Enhanced Data Integrity, Intelligent Power Failure Recovery, ATA Secure Erase, and TRIM, Apacer assures users of a versatile device on data storage.

1.1 Performance-Optimized Controller

The heart of SDM3 is the Flash controller, which translates standard SATA signals into the data and controls of the flash media. The SATA and Flash Management controller are specifically designed to attain high data throughput from the host to the flash.

1.1.1 Power Management Unit (PMU)

The power management unit (PMU) controls the power consumption of SDM3. It can dramatically extend product battery life by leaving the idle part of the circuitry into sleep mode. The PMU has zero wake-up latency.

1.1.2 SRAM Buffer

The Flash Controller performs as a SRAM buffer to optimize the host's data transfer to and from the flash media.

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2. Functional Block

SDM3 includes the SATA and Flash Management controllers, and flash media, as well as the SATA standard interface. Figure 2-1 shows the functional block diagram.

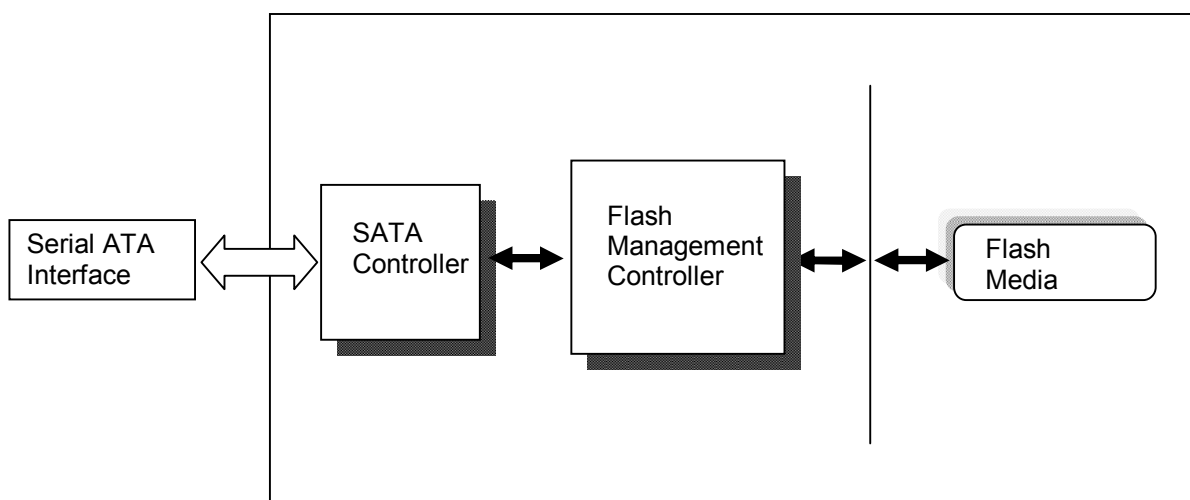


Figure 2-1: Functional block diagram

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3. Pin Assignments

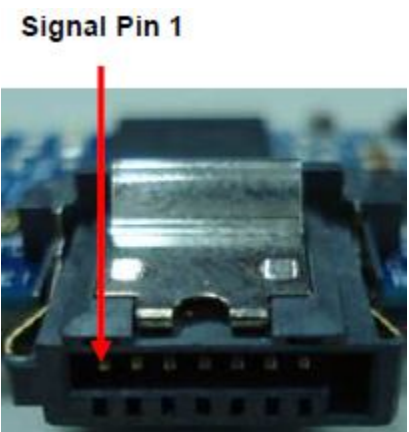


Table 3-1: Signal segment

Name	Type	Description
S1	GND	
S2	RxP	+ Differential Receive Signal
S3	RxN	- Differential Receive Signal
S4	GND	
S5	TxN	- Differential Transmit Signal
S6	TxP	+ Differential Transmit Signal
S7	GND	

Table 3-2: Power segment

Pin	Signal/Description
P1	VCC (5V)
P2	GND

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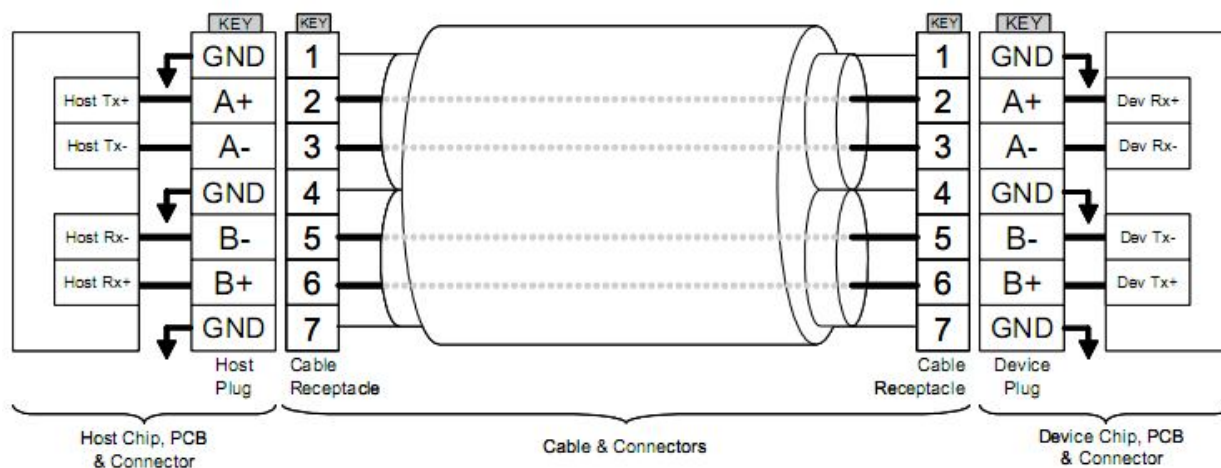


Figure 3-1: SATA Cable/Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

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4. Capacity Specification

Capacity specification of SDM3 product family is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
512 MB	494,936,064	959	16	63	966,672
1 GB	988,839,936	1916	16	63	1,931,328
2 GB	1,982,324,736	3841	16	63	3,871,728
4 GB	3,952,263,168	7658	16	63	7,719,264

*Display of total bytes varies from file systems.

4.1 Performance Specification

4.1.1 ATA Mode Support

SDM3 supports the following ATA operating modes:

- Supports up to PIO Mode-4
- Supports up to Multi-word DMA Mode-2
- Supports up to Ultra DMA Mode-5

4.1.2 Performance

Performances of SDM3 are listed below in table 4-2.

Table 4-2: Performance

Capacity	512 MB	1 GB	2 GB	4 GB
Performance				
Sustained read (MB/s)	25	30	30	30
Sustained write (MB/s)	5	10	10	10

Note: Results may differ from various flash configurations.

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4.2 Environmental Specifications

Environmental specification of SDM3 product family which follows the MIL-STD-810F standards is available as shown in Table 4-3.

Table 4-3 SDM3 environmental specifications

Item	Specification
operating temp.	0~70(°C) ^{*1} ; -40~85(°C) ^{*2}
non-operating temp.	-40~100(°C)
humidity	10~95% R.H, 30(°C) max. wet bulb temp., operating
operating vibration	10~2000(Hz), 15(G), sine wave
non-operating vibration	20~2000(Hz), 7.7(Grms), random wave
operating shock	50(G), 11(ms), half-sine wave
non-operating shock	1500(G), 0.5(ms), half-sine wave

*1 : commercial grade

*2 : industrial grade

4.3 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SDM3. Although many component MTBFs are given in databases and often these values are not really accurate, the prediction result for SDM3 is more than 2,000,000 hours.

4.4 Certification and Compliance

SDM3 complies with the following standards:

- CE – EN55022/55024
- FCC 47CFR Part15 Class B
- RoHS
- MIL-STD-810F
- SATA II (SATA Rev. 2.6)
- Up to ATA/ATAPI-7 (including S.M.A.R.T.)

5. Flash Management

5.1 Error Correction/Detection

SDM3 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 14 bits or 28 bits error in 1K bytes.

5.2 Bad Block Management

Although bad blocks on the flash media are already identified by the flash manufacturer, they can also be accumulated over time during operation. SDM3's controller maintains a table that lists those normal blocks with disk data, the free blocks for wear leveling, and bad blocks with errors. When a normal block is detected broken, it is replaced with a free block and listed as a bad block. When a free block is detected broken, it is then removed from the free block list and marked as a bad block.

During device operation, this ensures that newly accumulated bad blocks are transparent to the host. The device will stop file write service once there are only two free blocks left such that the read function is still available for copying the files from the disk into another.

5.3 Wear Leveling

The NAND flash devices are limited by a certain number of write cycles. When using a FAT-based file system, frequent FAT table updates are required. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole SSD, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. This scheme is called wear leveling.

Apacer's wear-leveling scheme is achieved both via buffer management and Apacer-specific static wear leveling. They both ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

5.4 Power Failure Management

The Low Power Detection on the controller initiates crucial data saving before the power supplied to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected power-off.

5.5 ATA Secure Erase

Accomplished by the Secure Erase (SE) command, which added to the open ANSI standards that control disk drives, "ATA Secure Erase" is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is a positive easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. Once executed, neither data nor the erase counter on the device would be recoverable, which blurs the accuracy of device lifespan. The process to erase will not be stopped until finished while encountering power failure, and will be continued when power is back on.

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5.6 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer SDM3 uses the standard SMART command B0h to read data from the drive for SMART feature as the SATA Rev.2.6 ATA/ATAPI-7 specifications. Based on the SFF-8035i Rev. 2.0 specifications, Apacer SMART defines vendor-specified SMART Attribute IDs (A0h, A1h, A2h, A3h, A4h-A5h) in SDM3. They represent initial back block count, bad block count, spare block count, maximum erase count, and average erase counts respectively. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before SDM3 is in critical condition.

5.7 Trim

Made of millions of NAND flash cells, SSD can be written into groups called pages in 4K size generally, but can only be erased in larger groups called blocks of 128 pages or 512KB. These stipulations are partially the source of many performance issues. Until an address gets used again, the SSD has to keep track of every last bit of data that's written on it. The ATA-TRIM instruction tilts the balance in favor of the SSD. TRIM addresses a major part of the performance degradation issue over time that plagues all SSDs. A TRIM enabled drive running an OS with TRIM support will stay closer to its peak performance over time.

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6. Software Interface

6.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SDM3. Commands are issued to SDM3 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 6-1: Command set

Code	Command	Code	Command
E5h	Check Power Mode	F3h	Security Erase Prepare
06h	Data Set Management	F4h	Security Erase Unit
90h	Execute Device Diagnostic	F5h	Security Freeze Lock
E7h	Flush Cache	F1h	Security Set Password
EAh	Flush Cache EXT	F2h	Security Unlock
Ech	Identify Device	70h	Seek
E3h	Idle	Efh	Set Features
E1h	Idle Immediate	C6h	Set Multiple Mode
91h	Initialize Device Parameters	E6h	Sleep
C8h	Read DMA	B0h	SMART
25h	Read DMA EXT	E2h	Standby
C4h	Read Multiple	E0h	Standby Immediate
29h	Read Multiple EXT	Cah	Write DMA
20h	Read Sector	35h	Write DMA EXT
24h	Read Sector EXT	C5h	Write Multiple
40h	Read Verify Sectors	39h	Write Multiple EXT
42h	Read Verify Sectors EXT	30h	Write Sector
10h	Recalibrate	34h	Write Sector EXT
F6h	Security Disable Password		

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7. Electrical Specification

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Range	Ambient Temperature	5V
Standard	0°C to +70°C	4.5-5.5V
Extended Temperature	-40°C to 85°C	

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V _{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V _{DD} with respect to GND	V	-0.5V min. to V _{DD} + 0.5V max.

Table 7-3: Recommended system power-up timing

Symbol	Parameter	Typical	Maximum	Units
T _{PU-READY} ¹	Power-up to Ready Operation	200	1000	ms
T _{PU-WRITE} ¹	Power-up to Write Operation	200	1000	ms

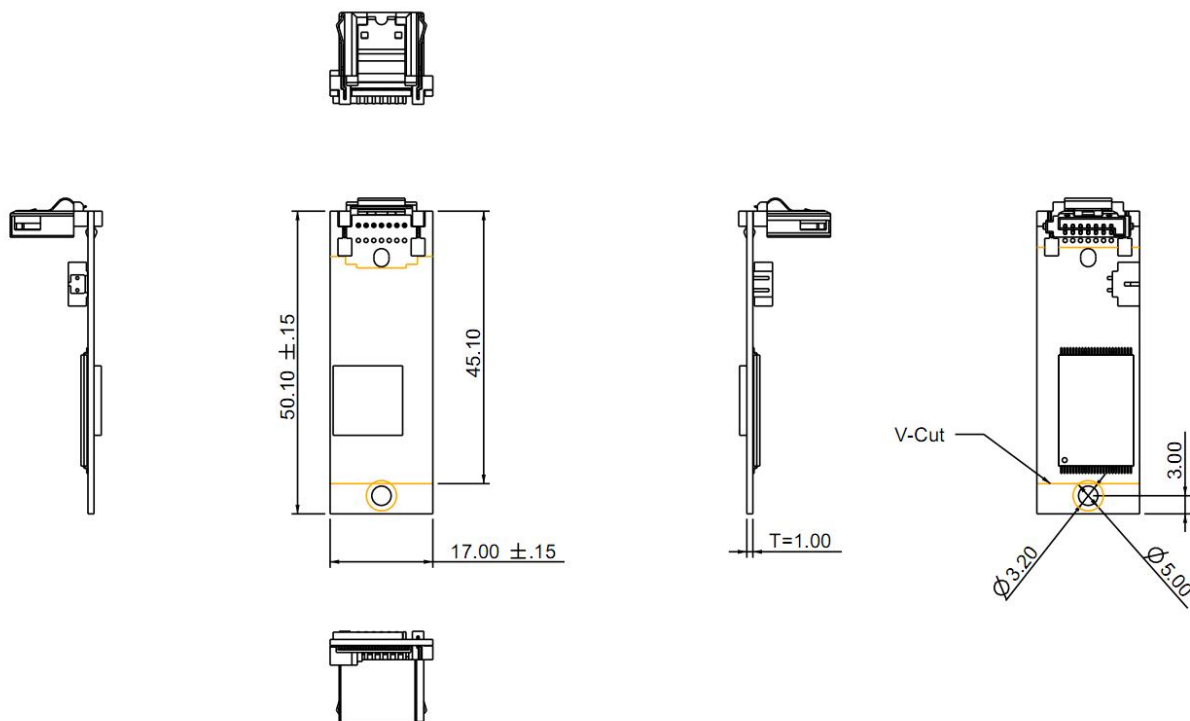
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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8. Physical Characteristics

8.1 Dimension

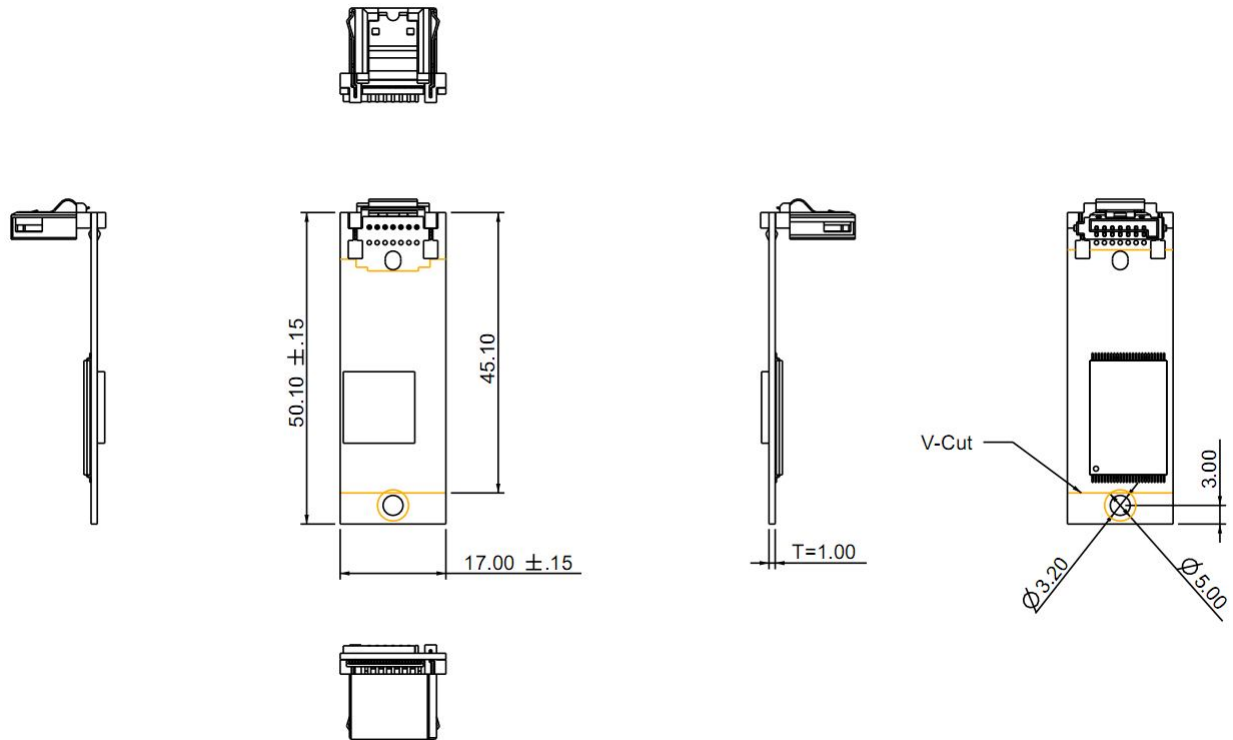
8.1.1 Power Cable Type



Unit: mm
Tolerance: ± 0.25

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8.1.2 Power Cable-Less Type



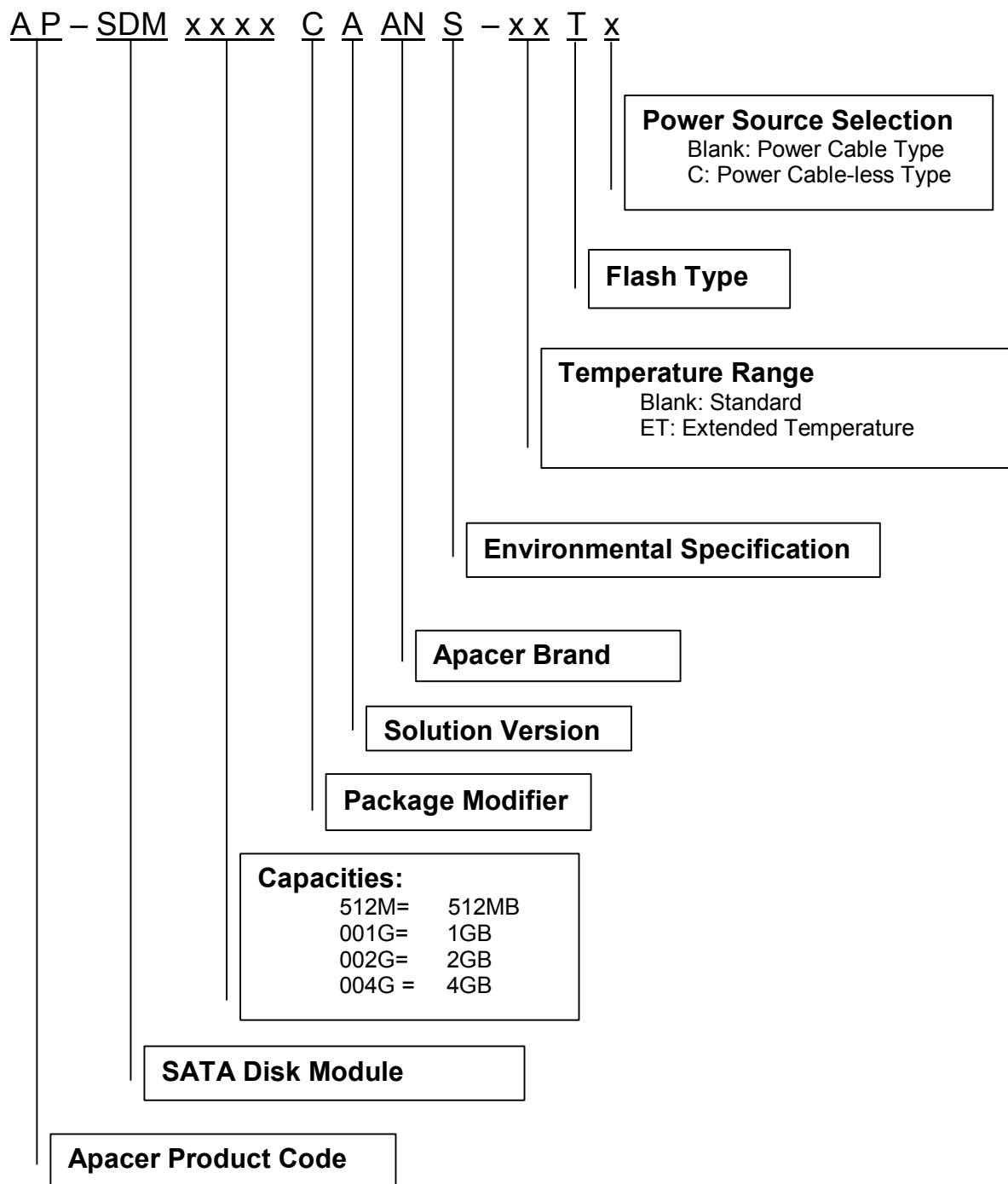
Unit: mm
Tolerance: $\pm$ 0.25

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9. Product Ordering Information

9.1 Product Code Designations



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9.2 Valid Combinations

7P/90D: Power Cable Type

Capacity	Standard	Extended Temperature
512MB	AP-SDM512MCAANS-T	AP-SDM512MCAANS-ETT
1GB	AP-SDM001GCAANS-T	AP-SDM001GCAANS-ETT
2GB	AP-SDM002GCAANS-T	AP-SDM002GCAANS-ETT
4GB	AP-SDM004GCAANS-T	AP-SDM004GCAANS-ETT

7P/90D: Power Cable-less Type

Capacity	Standard	Extended Temperature
512MB	AP-SDM512MCAANS-TC	AP-SDM512MCAANS-ETTC
1GB	AP-SDM001GCAANS-TC	AP-SDM001GCAANS-ETTC
2GB	AP-SDM002GCAANS-TC	AP-SDM002GCAANS-ETTC
4GB	AP-SDM004GCAANS-TC	AP-SDM004GCAANS-ETTC

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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Revision History

Revision	Date	Description	Remark
1.0	06/22/2011	Formal release	
1.1	07/18/2011	Updated Power Consumption - Active mode : 209 mA -> 205mA - Idle mode : 200 mA -> 95mA (Based on 512MB capacity)	
1.2	02/22/2012	Revised Pin assignment drawing Updated address of our European branch	

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Global Presence

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