CY7C343
CY7C343B

64-Macrocell MAX® EPLD

Features

- **64 MAX macrocells in 4 LABs**
- **8 dedicated inputs, 24 bidirectional I/O pins**
- **Programmable interconnect array**
- **0.8-micron double-metal CMOS EPROM technology (CY7C343)**
- **Advanced 0.65-micron CMOS technology to increase performance (CY7C343B)**
- **Available in 44-pin HLCC, PLCC**
- **Lowest power MAX device**

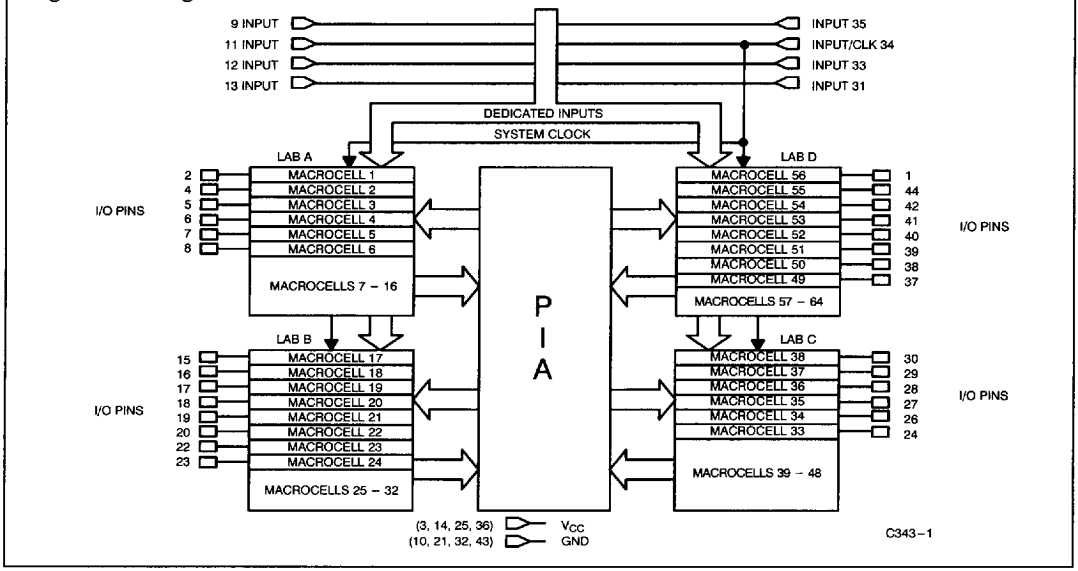
Functional Description

The CY7C343/CY7C343B is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343/CY7C343B contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Interconnect Array (PIA). There are 8 input pins, one that doubles as a clock pin when needed. The CY7C343/CY7C343B also has 28 I/O pins, each connected to a macrocell (6 for LABs A and C, and 8 for LABs B and D). The remaining 36 macrocells are used for embedded logic.

The CY7C343/CY7C343B is excellent for a wide range of both synchronous and asynchronous applications.

Logic Block Diagram



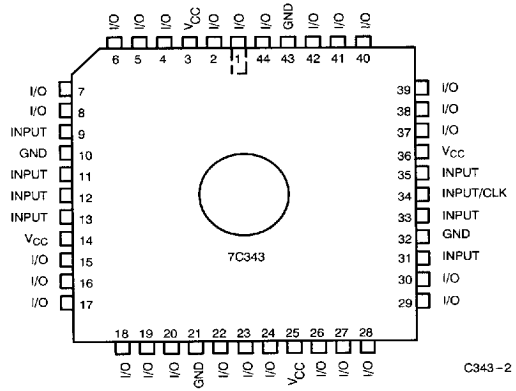
Selection Guide

		7C343B–12	7C343B–15	7C343–20 7C343B–20	7C343–25 7C343B–25	7C343–30 7C343B–30	7C343–35 7C343B–35
Maximum Access Time (ns)		12	15	20	25	30	35
Maximum Operating Current (mA)	Commercial	135	135	135	135	135	135
	Military		225	225	225	225	225
	Industrial	225	225	225	225	225	225
Maximum Standby Current (mA)	Commercial	125	125	125	125	125	125
	Military		200	200	200	200	200
	Industrial	200	200	200	200	200	200

Shaded area contains advanced information.

Pin Configuration

HLCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Maximum Junction Temperature (Under Bias) ..... 150°C

Supply Voltage to Ground Potential ..... −2.0V to +7.0V

Maximum Power Dissipation ..... 2500 mW

DC V_{CC} or GND Current ..... 500 mA

DC Output Current, per Pin ..... −25 mA to +25 mA

DC Input Voltage[1] ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... >1100V (per MIL-STD-883, method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		− 40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 4]		− 30	− 90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		125	mA
			Military/Industrial		200	mA
I_{CC2}	Power Supply Current[5]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4, 5]	Commercial		135	mA
			Military/Industrial		225	mA
t_R	Recommended Input Rise Time				100	ns
t_F	Recommended Input Fall Time				100	ns

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Guaranteed but not 100% tested.
5. Measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.

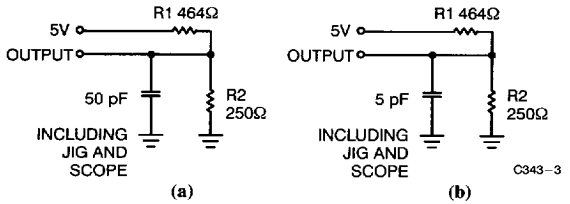
Capacitance[6]

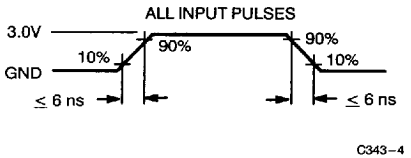
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	10	pF

Notes:

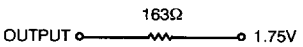
6. Part (a) in AC Test Load and Waveforms is used for all parameters except t_{ER} and t_{XZ}, which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by ensuring that internal signal skews or races are avoided. The result is simpler design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C343/CY7C343B may be easily determined using *Warp2™*, *Warp3™*, or MAX+PLUS® software or by the model shown in *Figure 1*. The CY7C343/CY7C343B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* or MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.The CY7C343/CY7C343B contains circuitry to protect device pins from high static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set-up time. If ($t_{AS2} + t_{AH}$)

is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AH})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C343/CY7C343B.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous), then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}), causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

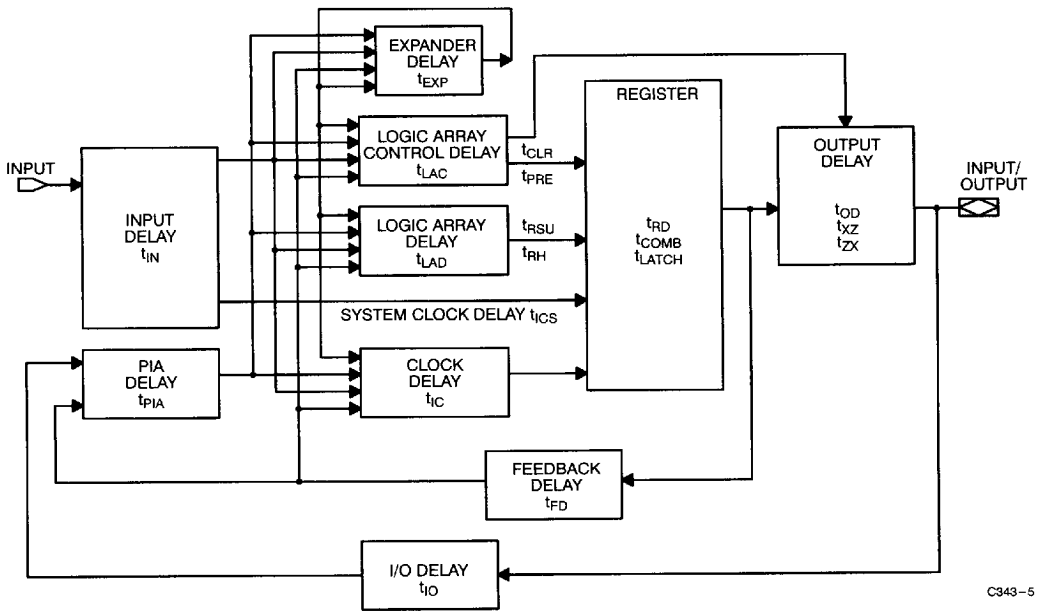


Figure 1. CY7C343/CY7C343B Internal Timing Model

External Synchronous Switching Characteristics[6] Over Operating Range

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l/Ind		20		25		32	ns
		Mil				25		32	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l/Ind		18		23		30	ns
		Mil				23		30	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l/Ind		26		33		42	ns
		Mil				33		42	
t_{EA}	Input to Output Enable Delay[4, 7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		6		7		12	ns
		Mil				7		12	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l/Ind		14		17		25	ns
		Mil				17		25	
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7]	Com'l/Ind	8		10		12		ns
		Mil			10		12		
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7, 12]	Com'l/Ind	16		20		24		ns
		Mil			20		24		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0		0		ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	4.5		5		6		ns
		Mil			5		6		
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	4.5		5		6		ns
		Mil			5		6		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		3		3	ns
		Mil				3		3	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	9		10		12		ns
		Mil			10		12		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l/Ind	71.4		58.8		41.6		MHz
		Mil			58.8		41.6		

Shaded areas contain advanced information.

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	Com'l/Ind	90.9		76.9		66.6		MHz
		Mil			76.9		66.6		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	111.1		100		83.3		MHz
		Mil			100		83.3		
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	Com'l/Ind	111.1		100		83.3		MHz
		Mil			100		83.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3		3		ns
		Mil			3		3		
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l/Ind	12		15		20		ns
		Mil			15		20		

Shaded areas contain advanced information.

Notes:

7. This specification is a measure of the delay from input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input.
   If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9. This specification is a measure of the delay from an input signal applied to a dedicated input (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
10. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
12. If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
14. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
15. This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local, originating within the same LAB.
16. This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343–25 7C343B–25		7C343–30 7C343B–30		7C343–35 7C343B–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[8]	Com'l/Ind		39		44		53	ns
		Mil		39		44		53	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[9]	Com'l/Ind		37		44		55	ns
		Mil		37		44		55	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[4, 10]	Com'l/Ind		51		58		73	ns
		Mil		51		58		73	
t_{EA}	Input to Output Enable Delay[4, 7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{ER}	Input to Output Disable Delay[4, 7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l/Ind		14		16		20	ns
		Mil		14		16		20	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[4, 11]	Com'l/Ind		30		35		42	ns
		Mil		30		35		42	
t_{S1}	Dedicated Input or Feedback Set-Up Time to Synchronous Clock Input[7]	Com'l/Ind	15		20		25		ns
		Mil	15		20		25		
t_{S2}	I/O Input Set-Up Time to Synchronous Clock Input[7, 12]	Com'l/Ind	30		35		42		ns
		Mil	30		35		42		
t_H	Input Hold Time from Synchronous Clock Input[7]	Com'l/Ind	0		0		0		ns
		Mil	0		0		0		
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{RW}	Asynchronous Clear Width[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{RR}	Asynchronous Clear Recovery Time[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{RO}	Asynchronous Clear to Registered Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{PR}	Asynchronous Preset Recovery Time[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		
t_{PO}	Asynchronous Preset to Registered Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{CF}	Synchronous Clock to Local Feedback Input[4, 13]	Com'l/Ind		3		3		5	ns
		Mil		3		3		5	
t_P	External Synchronous Clock Period ($1/f_{MAX3}$)[4]	Com'l/Ind	16		20		25		ns
		Mil	16		20		25		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO1} + t_{S1})$)[4, 14]	Com'l/Ind	34		27		22.2		MHz
		Mil	34		27		22.2		

External Synchronous Switching Characteristics[6] Over Operating Range (continued)

Parameter	Description		7C343–25 7C343B–25 Min.	7C343–25 7C343B–25 Max.	7C343–30 7C343B–30 Min.	7C343–30 7C343B–30 Max.	7C343–35 7C343B–35 Min.	7C343–35 7C343B–35 Max.	Unit
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $(1/(t_{S1} + t_{CF}))$ or $(1/t_{CO1})$[4, 15]	Com'l/Ind	55		43		33		MHz
		Mil	55		43		33		
f_{MAX3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$, or $(1/t_{CO1})$[4, 16]	Com'l/Ind	62.5		50		40		MHz
		Mil	62.5		50		40		
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH}))$[4, 17]	Com'l/Ind	62.5		50		40		MHz
		Mil	62.5		50		40		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[4, 18]	Com'l/Ind	3		3		3		ns
		Mil	3		3		3		
t_{PW}	Asynchronous Preset Width[4, 7]	Com'l/Ind	25		30		35		ns
		Mil	25		30		35		

External Asynchronous Switching Characteristics Over Operating Range[6]

Parameter	Description		7C343B–12 Min.	7C343B–12 Max.	7C343B–15 Min.	7C343B–15 Max.	7C343–20 7C343B–20 Min.	7C343–20 7C343B–20 Max.	Unit
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l/Ind		12		15		20	ns
		Mil				15		20	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		20		25		32	ns
		Mil				25		32	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	3		3.5		4		ns
		Mil			3.5		4		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	12		13.5		15		ns
		Mil			13.5		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l/Ind	4		4.5		5		ns
		Mil			4.5		5		
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l/Ind	8		8.5		9		ns
		Mil			8.5		9		
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	Com'l/Ind	6		6.5		7		ns
		Mil			6.5		7		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		9		11		13	ns
		Mil				11		13	
t_{AP}	External Asynchronous Clock Period $(1/f_{MAXA4})$[4]	Com'l/Ind	14		15		16		ns
		Mil			15		16		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[4, 22]	Com'l/Ind	66.6		54.0		41.6		MHz
		Mil			54.0		41.6		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	Com'l/Ind	71.4		66.6		58.8		MHz
		Mil			66.6		58.8		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	71.4		66.6		50		MHz
		Mil			66.6		50		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	71.4		66.6		62.5		MHz
		Mil			66.6		62.5		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	12		12		15		ns
		Mil			12		15		

Shaded areas contain advanced information.

External Asynchronous Switching Characteristics Over Operating Range[6] (continued)

Parameter	Description		7C343–25 7C343B–25		7C343–30 7C343B–30		7C343–35 7C343B–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[7]	Com'l/Ind		25		30		35	ns
		Mil		25		30		35	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[19]	Com'l/Ind		40		46		55	ns
		Mil		40		46		55	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	5		6		8		ns
		Mil	5		6		8		
t_{AS2}	I/O Input Set-Up Time to Asynchronous Clock Input[7]	Com'l/Ind	20		25		30		ns
		Mil	20		25		30		
t_{AH}	Input Hold Time from Asynchronous Clock Input[7]	Com'l/Ind	6		8		10		ns
		Mil	6		8		10		
t_{AWH}	Asynchronous Clock Input HIGH Time[7]	Com'l/Ind	11		14		16		ns
		Mil	11		14		16		
t_{AWL}	Asynchronous Clock Input LOW Time[7, 20]	Com'l/Ind	9		11		14		ns
		Mil	9		11		14		
t_{ACF}	Asynchronous Clock to Local Feedback Input[4, 21]	Com'l/Ind		15		18		22	ns
		Mil		15		18		22	
t_{AP}	External Asynchronous Clock Period ($1/f_{MAXA4}$)[3]	Com'l/Ind	20		25		30		ns
		Mil	20		25		30		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$[4, 22]	Com'l/Ind	33		27		23		MHz
		Mil	33		27		23		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[4, 23]	Com'l/Ind	50		40		33		MHz
		Mil	50		40		33		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[4, 24]	Com'l/Ind	40		33		28		MHz
		Mil	40		33		28		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[4, 25]	Com'l/Ind	50		40		33		MHz
		Mil	50		40		33		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[4, 26]	Com'l/Ind	15		15		15		ns
		Mil	15		15		15		

Notes:

19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
20. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.

Internal Switching Characteristics Over Operating Range[6]

Parameter	Description		7C343B–12		7C343B–15		7C343–20 7C343B–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		2.5		3		4	ns
		Mil				3		4	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		2.5		3		4	ns
		Mil				3		4	
t_{EXP}	Expander Array Delay	Com'l/Ind		6		8		10	ns
		Mil				8		10	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		6		8		10	ns
		Mil				8		10	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		5		6		8	ns
		Mil				6		8	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	2		3		4		ns
		Mil			3		4		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	3		3.5		4		ns
		Mil			3.5		4		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		1		1		2	ns
		Mil				1		2	
t_{RD}	Register Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		1		1		2	ns
		Mil				1		2	
t_{CH}	Clock HIGH Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{CL}	Clock LOW Time	Com'l/Ind	3		4		6		ns
		Mil			4		6		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		5		7		12	ns
		Mil				7		12	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		0.5		0.5		2	ns
		Mil				0.5		2	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		1	ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		3		3		4	ns
		Mil				3		4	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l /Ind	2		3		4		ns
		Mil			3		4		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	2		3		4		ns
		Mil			3		4		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		8		10		12	ns
		Mil				10		12	

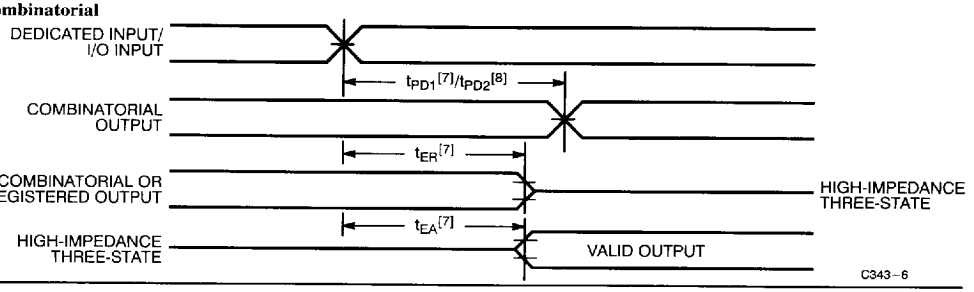
Shaded areas contain advanced information.

Internal Switching Characteristics Over Operating Range[6] (continued)

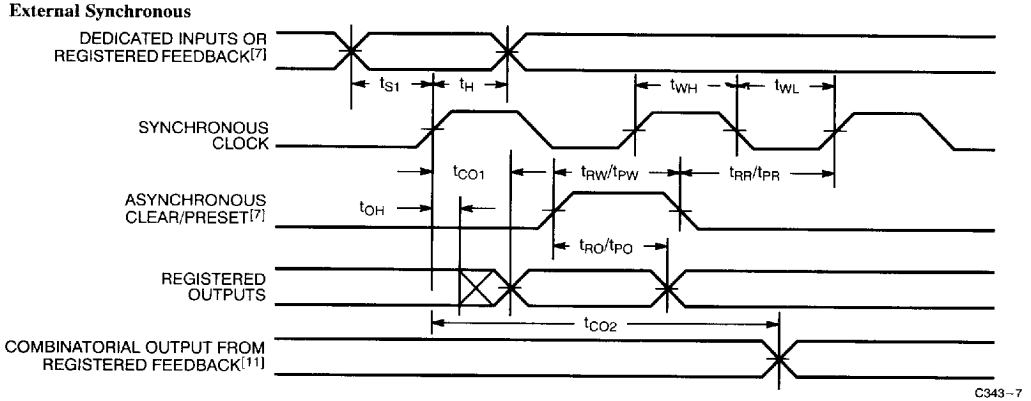
Parameter	Description		7C343–25 7C343B–25		7C343–30 7C343B–30		7C343–35 7C343B–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		5		7		9	ns
		Mil		5		7		9	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		5		5		7	ns
		Mil		5		5		7	
t_{EXP}	Expander Array Delay	Com'l/Ind		12		14		20	ns
		Mil		12		14		20	
t_{LAD}	Logic Array Data Delay	Com'l/Ind		12		14		16	ns
		Mil		12		14		16	
t_{LAC}	Logic Array Control Delay	Com'l/Ind		10		12		13	ns
		Mil		10		12		13	
t_{OD}	Output Buffer and Pad Delay	Com'l/Ind		5		5		6	ns
		Mil		5		5		6	
t_{ZX}	Output Buffer Enable Delay[27]	Com'l/Ind		10		11		13	ns
		Mil		10		11		13	
t_{XZ}	Output Buffer Disable Delay	Com'l/Ind		10		11		13	ns
		Mil		10		11		13	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	6		8		10		ns
		Mil	6		8		10		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	6		8		12		ns
		Mil	6		8		12		
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		3		4		4	ns
		Mil		3		4		4	
t_{RD}	Register Delay	Com'l/Ind		1		2		2	ns
		Mil		1		2		2	
t_{COMB}	Transparent Mode Delay[28]	Com'l/Ind		3		4		4	ns
		Mil		3		4		4	
t_{CH}	Clock HIGH Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{CL}	Clock LOW Time	Com'l/Ind	8		10		12.5		ns
		Mil	8		10		12.5		
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		14		16		18	ns
		Mil		14		16		18	
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		2		3	ns
		Mil		2		2		3	
t_{FD}	Feedback Delay	Com'l/Ind		1		1		2	ns
		Mil		1		1		2	
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		5		6		7	ns
		Mil		5		6		7	
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		5		6		7	ns
		Mil		5		6		7	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l/Ind	5		6		7		ns
		Mil	5		6		7		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l/Ind	5		6		7		ns
		Mil	5		6		7		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l/Ind		14		16		20	ns
		Mil		14		16		20	

Switching Waveforms

External Combinatorial



External Synchronous

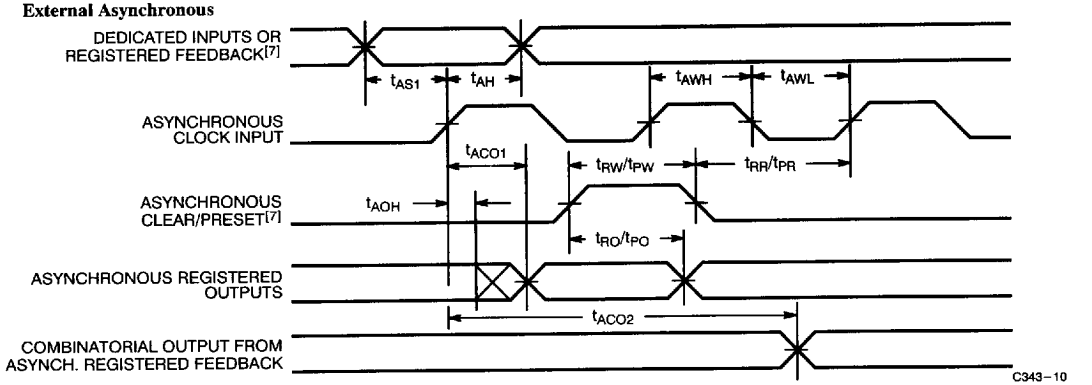


Notes:

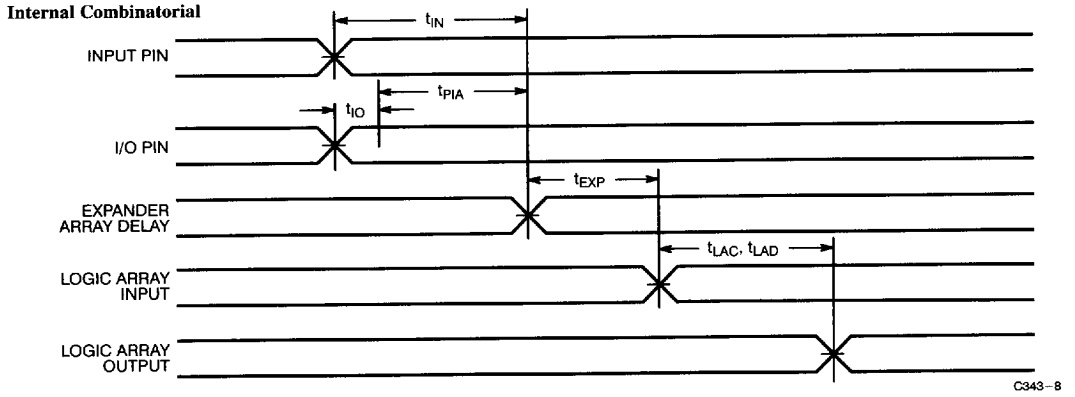
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/t_{ACF} + t_{AS1})$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Switching Waveforms (continued)

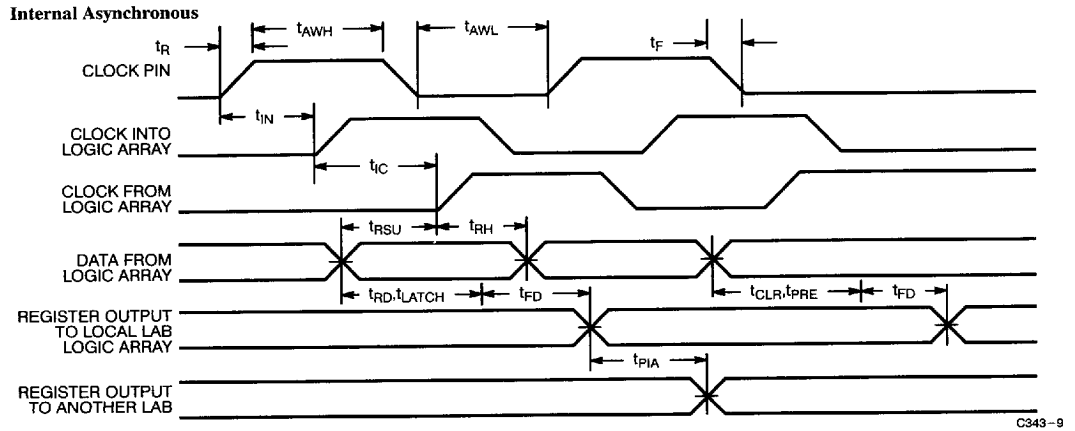
External Asynchronous



Internal Combinatorial

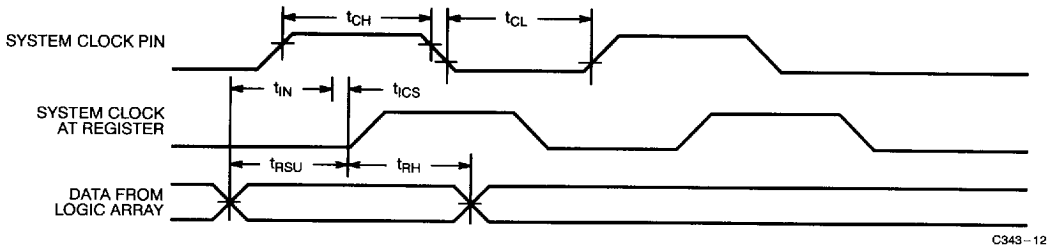


Internal Asynchronous

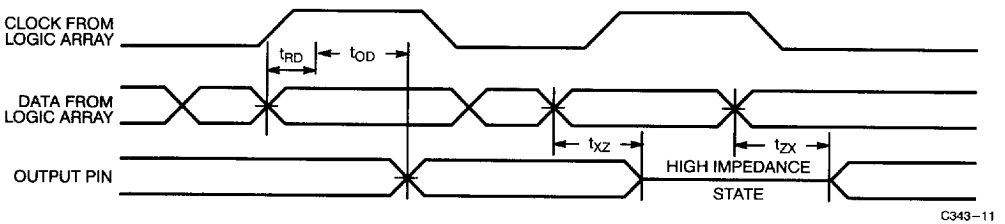


Switching Waveforms (continued)

Internal Synchronous



Output Mode



3

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C343B–12HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B–12JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
15	CY7C343B–15HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343B–15JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–15HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
20	CY7C343–20HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–20JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–20HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–20JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–20HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
25	CY7C343–25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–25HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–25JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–25HMB	H67	44-Pin Windowed Leaded Chip Carrier	
30	CY7C343–30HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–30HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–30JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–30HMB	H67	44-Pin Windowed Leaded Chip Carrier	
35	CY7C343–35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C343–35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343B–35HC/HI	H67	44-Pin Windowed Leaded Chip Carrier	
	CY7C343B–35JC/JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C343–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C343B–35HMB	H67	44-Pin Windowed Leaded Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD1}	7, 8, 9, 10, 11
t_{PD2}	7, 8, 9, 10, 11
t_{PD3}	7, 8, 9, 10, 11
t_{CO1}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{ACO1}	7, 8, 9, 10, 11
t_{ACO2}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11

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