

TLV2352 Dual Low-Voltage Differential Comparators

1 Features

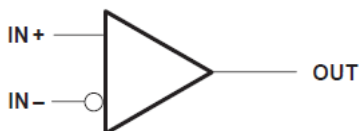
- Wide range of supply voltages: 2V to 8V
- Wide range of supply voltages: 2.7V to 8V (TLV2352IDR and TLV2352IPWR only)
- Fully characterized at 3V and 5V
- Very-low supply-current drain: 120 μ A typical at 3V
- Output compatible with TTL, MOS, and CMOS
- Fast response time: 200ns typical for TTL-level input step
- High input impedance: 10¹² Ω typical
- Extremely low input bias current: 5pA typical
- Common-mode input voltage range includes ground
- Built-in ESD protection

2 Description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and operates with power-supply rails as low as 2V (2.7V TLV2352IDR and TLV2352IPWR only). When powered from a 3V supply, the typical supply current is only 120 μ A.

The TLV2352 is designed using the Texas Instruments CMOS technology and therefore features an extremely high input impedance (typically greater than 10¹² Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and can be connected to achieve positive-logic wired-AND relationships. The TLV2352I is fully characterized at 3V and 5V for operation from –40°C to 85°C. The TLV2352M is fully characterized at 3V and 5V for operation from –55°C to 125°C.

The TLV2352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 1000V ESD rating using Human Body Model testing. However, care must be exercised in handling this device as exposure to ESD can result in degradation of the device parametric performance.



Symbol (Each Comparator)



Table of Contents

1 Features	1	5.8 Electrical Characteristics TLV2352M.....	6
2 Description	1	5.9 Switching Characteristics TLV2352M 3V.....	6
3 Device Comparison Table	3	5.10 Switching Characteristics TLV2352M 5V.....	7
4 Pin Configuration and Functions	3	6 Typical Characteristics (TLV2352IDR and TLV2352IPWR only)	8
5 Specifications	4	7 Device and Documentation Support	9
5.1 Absolute Maximum Ratings.....	4	7.1 Receiving Notification of Documentation Updates.....	9
5.2 Recommended Operating Conditions.....	4	7.2 Support Resources.....	9
5.3 Electrical Characteristics TLV2352I.....	5	7.3 Trademarks.....	9
5.4 Switching Characteristics TLV2352I 3V.....	5	7.4 Electrostatic Discharge Caution.....	9
5.5 Switching Characteristics TLV2352I 3V (TLV2352IDR and TLV2352IPWR only).....	5	7.5 Glossary.....	9
5.6 Switching Characteristics TLV2352I 5V.....	5	8 Revision History	9
5.7 Switching Characteristics TLV2352I 5V (TLV2352IDR and TLV2352IPWR only).....	6	9 Mechanical, Packaging, and Orderable Information	9

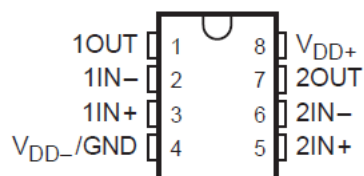
3 Device Comparison Table

Device Information							
T _A	V _{IO} max at 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D) ⁽¹⁾	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW) ⁽²⁾	PLASTIC DIP (U)
–40°C to 85°C	5mV	TLV2352ID	—	—	TLV2352IP	TLV2352IPWLE	—
–55°C to 125°C	5mV	—	TLV2352MFK	TLV2352MJG	—	—	TLV2352MU

(1) The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).

(2) The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE).

4 Pin Configuration and Functions



**Figure 4-1. TLV2352I D or P Package
TLV2352M JG Package (Top View)**

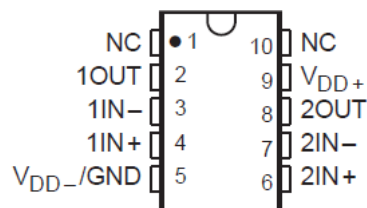
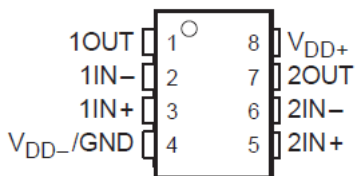


Figure 4-2. TLV2254M U Package (Top View)



NC - No internal connection

Figure 4-3. TLV2352I PW Package (Top View)

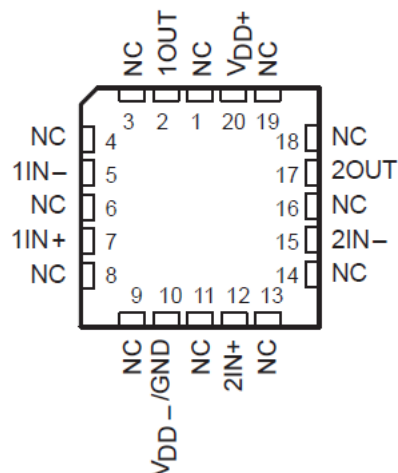


Figure 4-4. TLV2352M FK Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{DD}	Supply voltage ⁽²⁾			8	V
V _{ID}	Differential input voltage ⁽³⁾			±V _{DD}	V
V _I	Input voltage range		–0.3	V _{DD}	V
V _O	Output voltage			8	V
I _I	Input current			±5	mA
I _O	Output current			20	mA
	Duration of output short-circuit current to GND ⁽⁴⁾			Unlimited	
T _A	Operating free-air temperature range	TLV2352I	–40	85	°C
		TLV2352M	–55	125	
T _{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D package		260	°C
		P package			
		PW package			
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	FK package		300	°C
		JG package			
		U package			

- (1) Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{DD}	Supply voltage		2	8	V
V _{DD}	Supply voltage (TLV2352IDR and TLV2352IPWR only)		2.7	8	V
V _{IC}	Common-mode input voltage	V _{DD} = 3V	0	1.75	V
		V _{DD} = 5V	0	3.75	
T _A	Operating free-air temperature	TLV2352I	–40	85	°C
		TLV2352M	–55	125	

5.3 Electrical Characteristics TLV2352I

at specified free-air temperature⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A ⁽²⁾	TLV2352I						UNIT
					V _{DD} = 3V			V _{DD} = 5V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = V _{ICR} min		25°C	1		5	1		5	mV
				Full range	7		7				
I _{IO}	Input offset current			25°C	1			1			pA
				85°C	1		1			nA	
I _{IB}	Input bias current			25°C	5			5			pA
				85°C	2		2			nA	
V _{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75		0 to 3.75				
I _{OH}	High-level output current	V _{ID} = 1V		25°C	0.1			0.1			nA
				Full range	1		1			μA	
V _{OL}	Low-level output voltage	V _{ID} = −1V	I _{OL} = 2mA	25°C	115	300	150		400	mV	
				Full range	600		700				
I _{OL}	Low-level output current	V _{ID} = −1V	V _{OL} = 1.5V	25°C	6	16	6		16	mA	
I _{DD}	Supply current	V _{ID} = 1V	No load	25°C	120	250	140		300	μA	
				Full range	350		400				

(1) All characteristics are measured with zero common-mode input voltages unless otherwise noted.

(2) Full range is -40°C to 85°C.

5.4 Switching Characteristics TLV2352I 3V

V_{dd} = 3V, T_a = 25°C

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1kΩ, C _L = 15pF ^{(1) (2)}	100mV input step with 5mV overdrive		640		ns

5.5 Switching Characteristics TLV2352I 3V (TLV2352IDR and TLV2352IPWR only)

V_{dd} = 3V, T_a = 25°C

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1kΩ, C _L = 15pF ^{(1) (2)}	100mV input step with 10mV overdrive		200		ns

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1V with V_{DD} = 3V or V_O = 1.4V with V_{DD} = 5V.

5.6 Switching Characteristics TLV2352I 5V

V_{DD} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	R _L = 5.1kΩ, C _L = 15pF ^{(1) (2)}	100mV input step with 5mV overdrive		650		ns
		TTL-level input step		200		

5.7 Switching Characteristics TLV2352I 5V (TLV2352IDR and TLV2352IPWR only)

 $V_{DD} = 5V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	$R_L = 5.1k\Omega$, $C_L = 15pF^{(1)(2)}$	100mV input step with 10mV overdrive		200		ns
		100mV overdrive		100		

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses $V_O = 1V$ with $V_{DD} = 3V$ or $V_O = 1.4V$ with $V_{DD} = 5V$.

5.8 Electrical Characteristics TLV2352M

 at specified free-air temperature⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A ⁽²⁾	TLV2352M						UNIT
					V _{DD} = 3V			V _{DD} = 5V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = V _{ICRmin}		25°C	1		5	1		5	mV
				Full range			10			10	
I _{IO}	Input offset current			25°C	1			1			pA
				125°C			10			10	nA
I _{IB}	Input bias current			25°C	5			5			pA
				125°C			20			20	nA
V _{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75			0 to 3.75			
I _{OH}	High-level output current	V _{ID} = 1V		25°C	0.1			0.1			nA
				Full range	1			1			μA
V _{OL}	Low-level output voltage	V _{ID} = −1V	I _{OL} = 2mA	25°C	115		300	150		400	mV
				Full range			600			700	
I _{OL}	Low-level output current	V _{ID} = −1V	V _{OL} = 1.5V	25°C	6	16		6	16		mA
I _{DD}	Supply current	V _{ID} = 1V	No load	25°C	120		250	140		300	μA
				Full range			350			400	

(1) All characteristics are measured with zero common-mode input voltages unless otherwise noted.

(2) Full range is $-55^\circ C$ to $125^\circ C$.

5.9 Switching Characteristics TLV2352M 3V

 $V_{DD} = 3V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS		TLV2352M			UNIT
			MIN	TYP	MAX	
Response time	$R_L = 5.1k\Omega$, $C_L = 100pF^{(1)(2)}$	100mV input step with 5mV overdrive			1400	ns

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses $V_O = 1V$ with $V_{DD} = 3V$ or $V_O = 1.4V$ with $V_{DD} = 5V$.

5.10 Switching Characteristics TLV2352M 5V

$V_{DD} = 5V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS		TLV2352M			UNIT
			MIN	TYP	MAX	
Response time	$R_L = 5.1k\Omega$, $C_L = 100pF^{(1) (2)}$	100mV input step with 5mV overdrive			1300	ns
		TTL-level input step			900	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses $V_O = 1V$ with $V_{DD} = 3V$ or $V_O = 1.4V$ with $V_{DD} = 5V$.

6 Typical Characteristics (TLV2352IDR and TLV2352IPWR only)

At $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{V}$, $V_{CM} = V_S/2$, $C_L = 15\text{pF}$, Input Overdrive = Input Underdrive = 100mV , $R_{PU} = 10\text{k}\Omega$, unless otherwise noted.

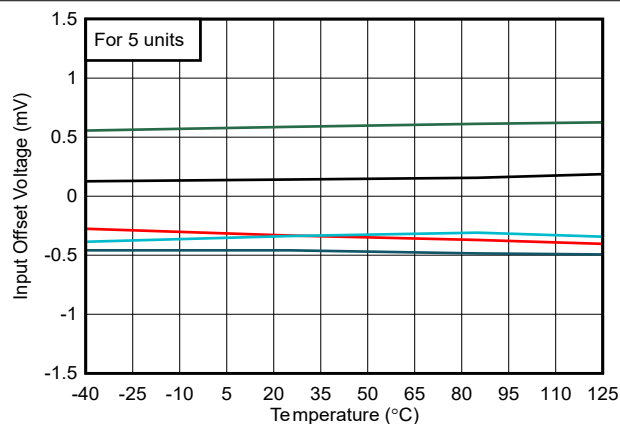


Figure 6-1. Offset vs. Temperature

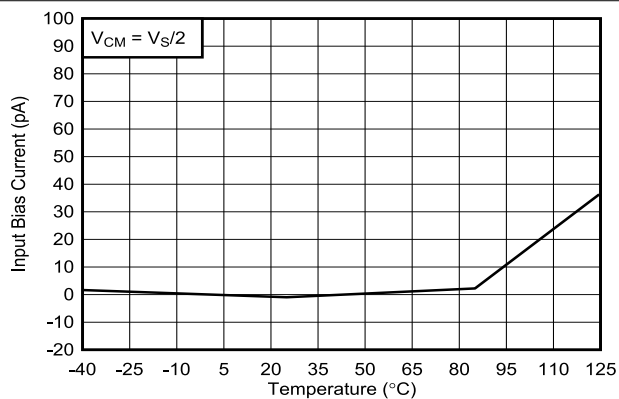


Figure 6-2. Bias Current vs. Temperature

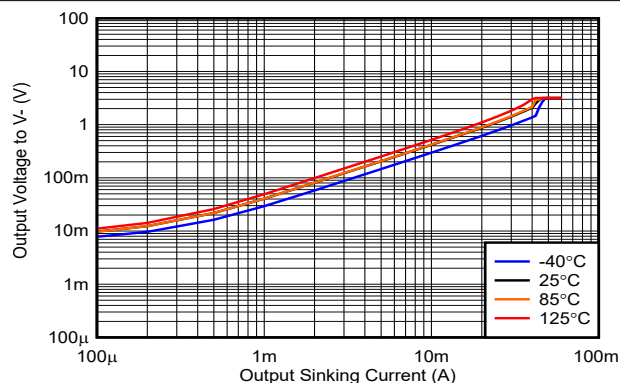


Figure 6-3. Output Voltage vs. Sinking Current

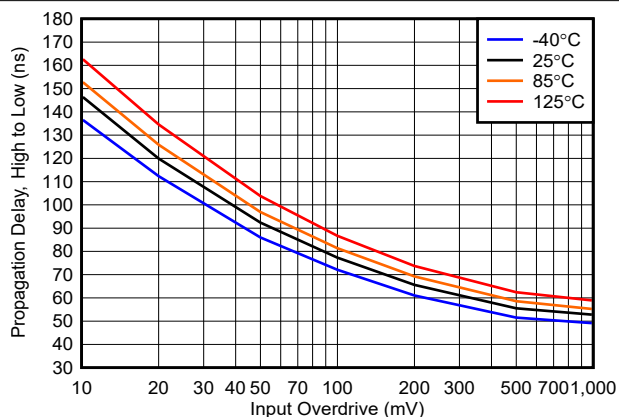


Figure 6-4. Propagation Delay, (High to Low) vs. Input Overdrive

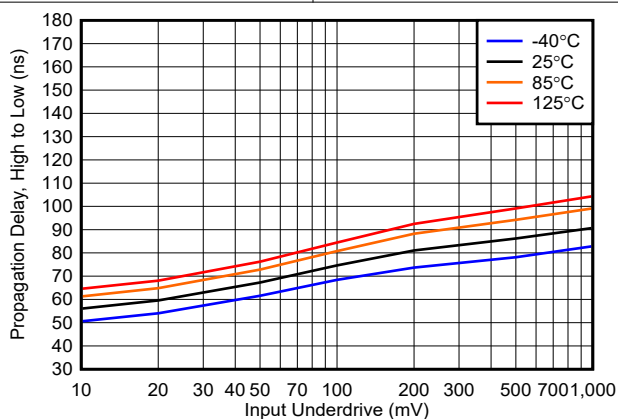


Figure 6-5. Propagation Delay, (High to Low) vs. Input Underdrive

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2025) to Revision D (July 2025)	Page
• Removed TLV2352Y throughout data sheet.....	1
• Specified electrical characteristic differences for orderables TLV2352IDR and TLV2352IPWR.....	1

Changes from Revision B (March 1999) to Revision C (June 2025)	Page
• Updates throughout data sheet to reflect performance of new die.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9688101QPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M
TLV2352ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2352I
TLV2352IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I
TLV2352IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I
TLV2352IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2352IP
TLV2352IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2352IP
TLV2352IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 85	TY2352
TLV2352IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352
TLV2352IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352
TLV2352MJG	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLV2352MJG
TLV2352MJG.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLV2352MJG
TLV2352MJGB	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M
TLV2352MJGB.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2352, TLV2352M :

- Catalog : [TLV2352](#)

- Military : [TLV2352M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2352IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2352IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2352IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2352IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2352IP.A	P	PDIP	8	50	506	13.97	11230	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025