❑ MN102H55G

Type		MN102H55G
ROM (×8-bit)		128 K
RAM (×8-bit)		4 K
Package		LQFP100-P-1414 *Pb free
Minimum Instruction Execution Time	With Main Clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)
Interrupts	• $\overline{\text{RST}}$ pin • Watchdog • NMI pin • Timer counter 0 to 7 underflow • Timer counter 8 to 12 underflow • Timer counter 8 to 12 compare capture A • Timer counter 8 to 12 compare capture B • ATC ch 0 to 3 transfer finish • ETC ch 0 to 1 transfer finish • External 0 to 4 • Serial ch 0 to 4 transmission • Serial ch 0 to 4 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish	
Timer Counter	Timer counter 0 : 8-bit × 1 (prescaler, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; 1/4 of system clock (XI) frequency; system clock (BOSC); TM0IO pin Interrupt source ····· underflow of timer counter 0 Timer counter 1 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 1 Timer counter 2 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 2 Timer counter 3 : 8-bit × 1 (A/D conversion start, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 3 Timer counter 4 : 8-bit × 1 (serial clock generator, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM4IO pin Interrupt source ····· underflow of timer counter 4 Timer counter 5 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; system clock (BOSC) Interrupt source ····· underflow of timer counter 5 Timer counter 6 : 8-bit × 1 (timer interrupts) Clock source ····· 1/4 of system clock (XI) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 6 Timer counter 7 : 8-bit × 1 (timer output, event count, timer interrupts) Clock source ····· 1/4 of system clock (XI) frequency; underflow of timer counter 0; TM7IO pin Interrupt source ····· underflow of timer counter 7 (Connectable) timer counter 0 to 7 Timer counter 8 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM8IB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM8IA pin/TM8IB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 8; timer counter 8 compare capture A; timer counter 8 compare capture B	

Timer Counter (Continue)		Timer counter 9 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM9IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM9IA pin/TM9IB pin (1 ×, 4 ×); TM9IC pin Interrupt source ····· underflow of timer counter 9; timer counter 9 compare capture A; timer counter 9 compare capture B Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM10IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM10IA pin/TM10IB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM11IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM11IA pin/TM11IB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM12IB pin; 1/2 of system clock (BOSC); 2-phase encode of TM12IA pin/TM12IB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B Timer counter 13, 14 : 8-bit × 4 (simple PWM output) Clock source ····· 1/2 of system clock (BOSC); underflow of timer counter 0 Timer counter 15 : 16-bit × 1 (pulse width measurement) Clock source ····· system clock (BOSC); 1/2 of system clock (BOSC); underflow of timer counter 0; TM15IB pin
Serial Interface		Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 1 underflow; 1/8, 1/2 of timer counter 2 underflow; external pin Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 4 underflow; 1/8, 1/2 of timer counter 5 underflow; external pin Serial 4 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 1 underflow; 1/8, 1/2 of timer counter 5 underflow; external pin UART × 2 (common use with serial 3, 4) I^2C × 2 (common use with serial 3,4; single master)
I/O Pins	**I/O**	82 • Common use : 46 (address data separate 8-bit mode) • Common use : 53 (address data multiplex 8-bit mode)
A/D Inputs		10-bit × 8-ch. (with S/H)
D/A Inputs		8-bit × 2-ch.
PWM		16-bit × 5-ch. (timer counter 8 to 12)
ICR		16-bit × 5-ch. (timer counter 8 to 12)
OCR		16-bit × 5-ch. (timer counter 8 to 12)
Notes		Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

A/D characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Non-linear error		10-bit			±4	LSB
A/D conversion time		at 34 MHz	3.29			µs
Analog input voltage	VIA		VSS		VDD	V

(Ta = 25°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

D/A characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Non-linear error		8-bit			±3	LSB
Setting time		CL = 70 pF			6	µs
Analog output resistance			3	12	20	kΩ

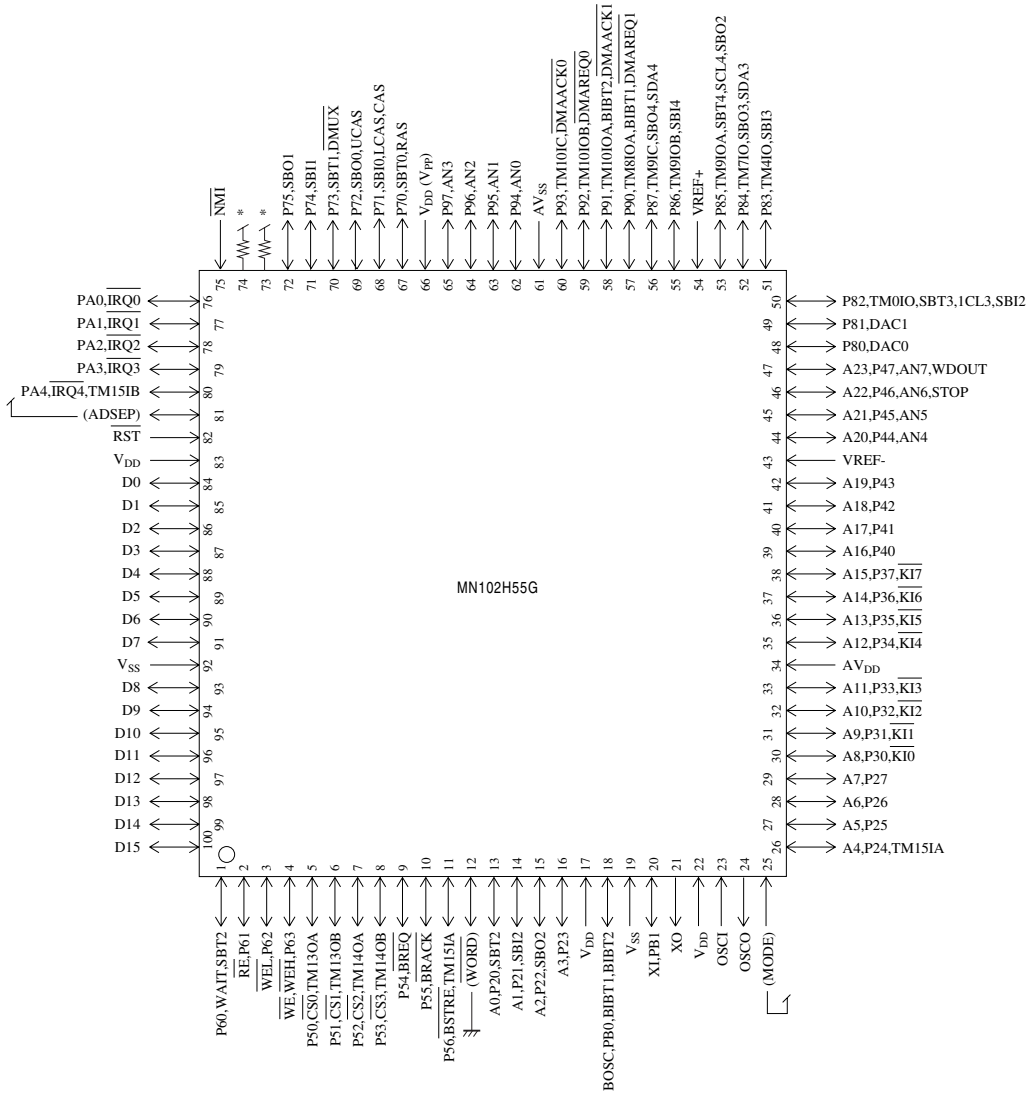
(Ta = 25°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz , VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open			70	µA
Supply current at HALT	IDDH				23	mA

(Ta = –40°C to +85°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Pb free

* Use 33 kΩ to 50 kΩ

* Pin position in 16-bit bus width address data split memory extension mode.

Support Tool

In-circuit Emulator	PX-ICE102H55-LQFP100-P-1414	
Flash Memory Built-in Type	Type	MN102HF55G
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	66.6 ns (at 3.0 V to 3.6 V, 30 MHz)
	Package	LQFP100-P-1414 *Pb free

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