LM2724A High Speed 3A Synchronous MOSFET Driver

Check for Samples: LM2724A

FEATURES

- **Shoot-Through Protection**
- **Input Under-Voltage-Lock-Out**
- **3A Peak Driving Current**
- **195µA Quiescent Current**
- **28V Input Voltage in Buck Configuration**
- **SOIC-8 and WSON Packages**

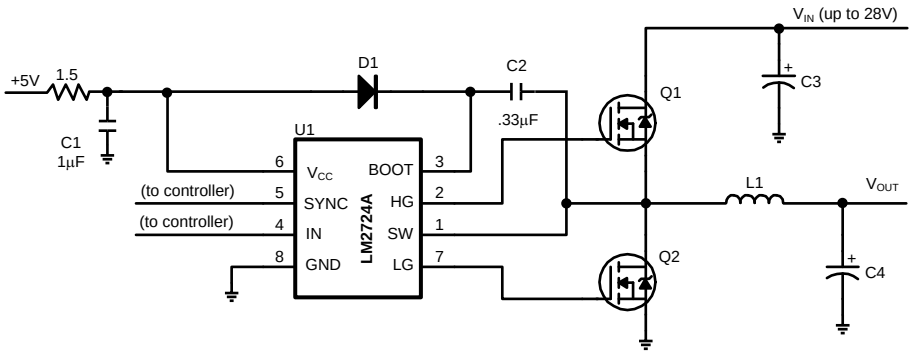
APPLICATIONS

- **High Current DC/DC Power Supplies**
- **High Input Voltage Switching Regulators**
- **Fast Transient Microprocessors**
- **Notebook Computers**

DESCRIPTION

The LM2724A is a dual N-channel MOSFET driver which can drive both the top and bottom MOSFETs in a push-pull structure simultaneously. The LM2724A takes a logic input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom MOSFETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2724A is about 3A. Input UVLO (Under-Voltage-Lock-Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both driver outputs and will not turn on a driver until the other driver output is low. The top gate voltage needed by the top MOSFET is obtained through an external boot-strap structure. When not switching, the LM2724A only draws up to 195µA from the 5V rail. The synchronization operation of the bottom MOSFET can be disabled by pulling the SYNC pin to ground.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

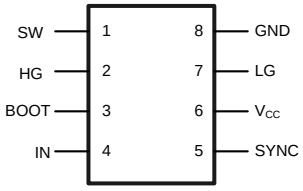


Figure 1. 8-Lead SOIC
See Package Number D

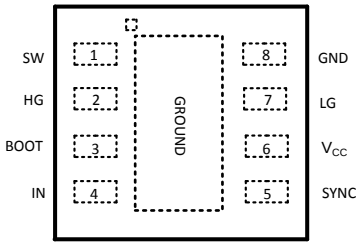
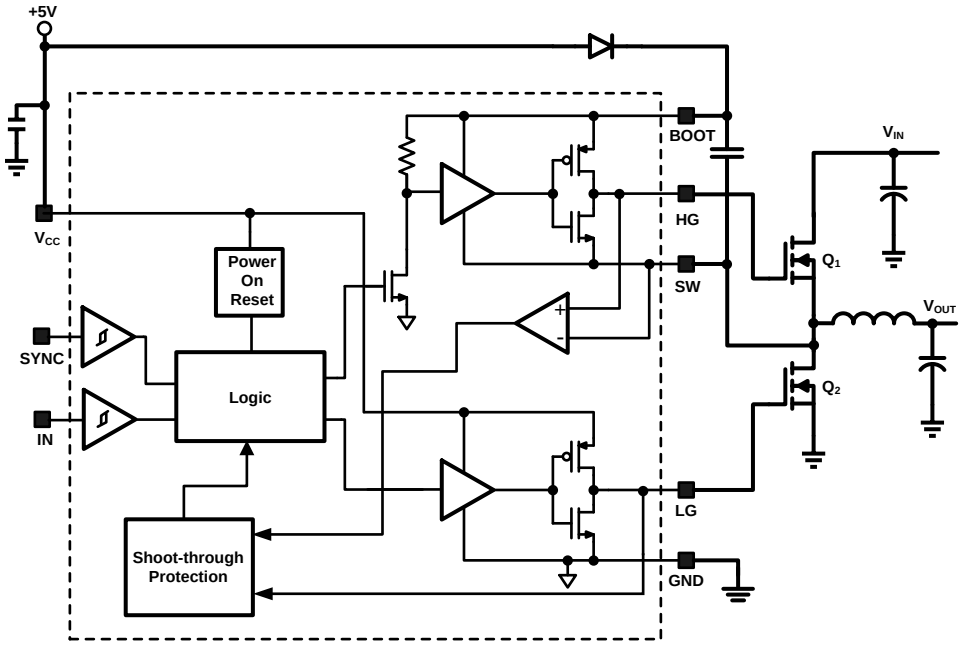


Figure 2. 8-Lead WSON
See Package Number NGN

PIN DESCRIPTIONS

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output. Should be connected to the top FET gate.
3	BOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	IN	Accepts a logic control signal
5	SYNC	Bottom gate enable
6	V_{CC}	Connect to +5V supply
7	LG	Bottom gate drive output. Should be connected to the bottom FET gate.
8	GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE / UNITS
V_{CC}		7V
BOOT to SW		7V
BOOT to GND(3)		35V
SW to GND(4)		-2V to 30V
Junction Temperature		+150°C
Power Dissipation(5)		720mW (SOIC-8) 3.2W (WSON-8)
Storage Temperature		−65°C to 150°C
ESD Susceptibility	Human Body Model(6)	2.0 kV
Soldering Time, Temperature		10sec., 300°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The ensured specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) If BOOT voltage exceeds this value, the ESD structure will degrade.
(4) The SW pin can have -2V to -0.5V applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30V.
(5) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for LM2724A is 172°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 0.7W. The θ_{JA}, for LM2724A WSON package is 39°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 3.2W.
(6) ESD machine model susceptibility is 200V.

RECOMMENDED OPERATING CONDITIONS(1)

	VALUE / UNITS
V_{CC}	4.3V to 6.8V
Junction Temperature Range	-40°C to 125°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The ensured specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.

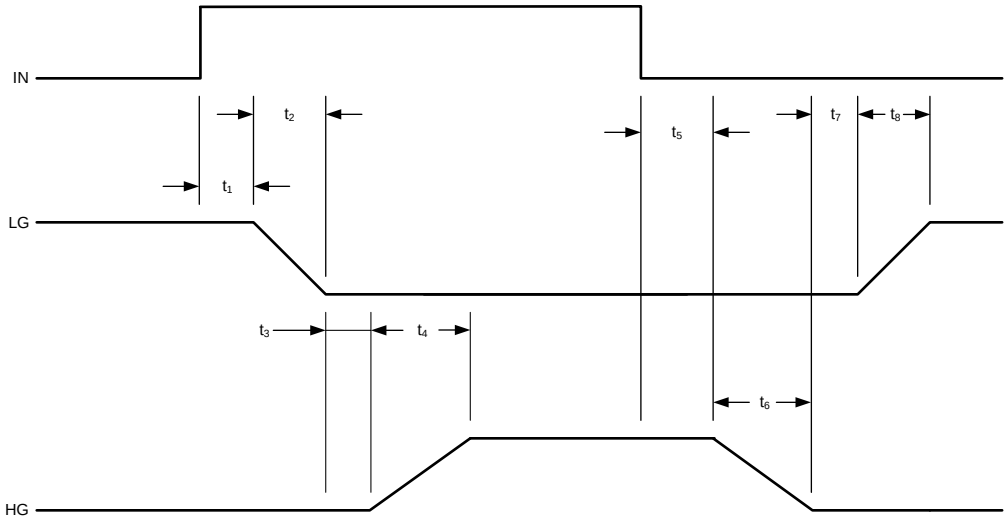
Electrical Characteristics — LM2724A

V_{CC} = BOOT = SYNC = 5V, SW = GND = 0V, unless otherwise specified. Tyicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	IN = 0V		145	**195**	µA
TOP DRIVER						
	Peak Pull-Up Current			3.0		A
	Pull-Up Rds_on	$I_{BOOT} = I_{HG}$ = 0.3A		1.2		Ω
	Peak Pull-down Current			−3.2		A
	Pull-down Rds_on	$I_{SW} = I_{HG}$ = 0.3A		0.5		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			12		ns
t_3	Pull-Up Dead Time	Timing Diagram		19		ns
t_5	Pull-Down Delay	Timing Diagram, from IN Falling Edge		27		ns
BOTTOM DRIVER						
	Peak Pull-Up Current			3.2		A
	Pull-up Rds_on	$I_{VCC} = I_{LG}$ = 0.3A		1.1		Ω
	Peak Pull-down Current			3.2		A
	Pull-down Rds_on	$I_{GND} = I_{LG}$ = 0.3A		0.6		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time			14		ns
t_7	Pull-up Dead Time	Timing Diagram		22		ns
t_1	Pull-down Delay	Timing Diagram		13		ns
LOGIC						
V_{uvlo_up}	V_{CC} Under-Voltage-Lock-Out Upper Threshold	V_{CC} rises from 0V toward 5V			**4**	V
V_{uvlo_dn}	V_{CC} Under-Voltage-Lock-Out Lower Threshold	VCC falls from 5V toward 0V	**2.5**			V
V_{uvlo_hys}	V_{CC} Under-Voltage-Lock-Out Hysteresis	V_{CC} falls from 5V toward 0V		0.8		V
V_{IH_SYNC}	SYNC Pin High Input		**55%**			V_{CC}
V_{IL_SYNC}	SYNC Pin Low Input				**25%**	V_{CC}
I_{leak_SYNC}	SYNC Pin Leakage Current	SYNC = 5V, Sink Current			**2**	µA
		SYNC = 0V, Source Current			**10**	µA
I_{leak_IN}	IN Pin Leakage Current	IN = 0V, Source Current			**2**	µA
		IN = 5V, Sink Current			**10**	µA
t_{on_min1}	Minimum Positive Pulse Width at IN Pin (1)			160		ns
t_{on_min2}	Minimum Positive Pulse Width at IN Pin for HG to Respond (2)			45		ns
t_{on_min3}	Minimum Positive Pulse Width at IN Pin for LG to Respond (3)			10		ns
t_{off_min1}	Minimum Negative Pulse Width at IN Pin for LG to Respond (4)			40		ns
t_{off_min2}	Minimum Negative Pulse Width at IN Pin for HG to Respond (5)			5		ns
V_{IH_IN}	IN High Level Input Voltage	When IN pin goes high from 0V	**55%**			V_{CC}
V_{IL_IN}	IN Low Level Input Voltage	When IN pin goes low from 5V			**25%**	V_{CC}

(1) If the positive pulse width at IN pin is below this value but above t_{on_min2}, the pulse is internally stretched to t_{on_min1}, so the HG width will be a constant value.
(2) If the positive pulse width at IN pin is below this value but above t_{on_min3}, then HG stops responding while LG still responds to the pulse.
(3) If the positive pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.
(4) If the negative pulse width at IN pin is below this value but above t_{off_min2}, then LG stops responding while HG still responds.
(5) If the negative pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.

TIMING DIAGRAM



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2724AMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2724 AM
LM2724AMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2724 AM
LM2724AMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2724 AM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

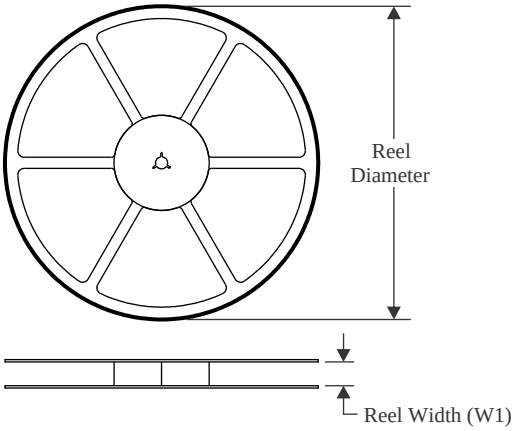
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

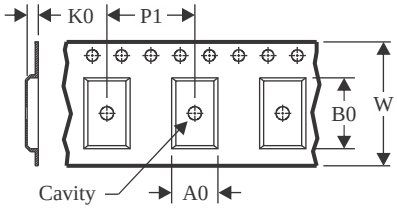
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

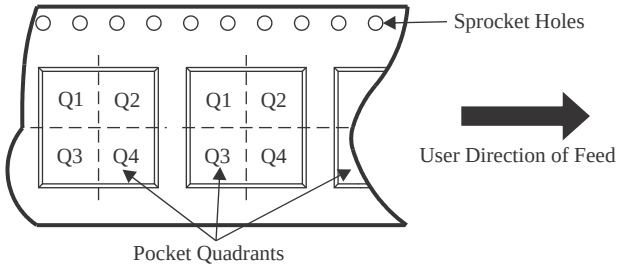


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

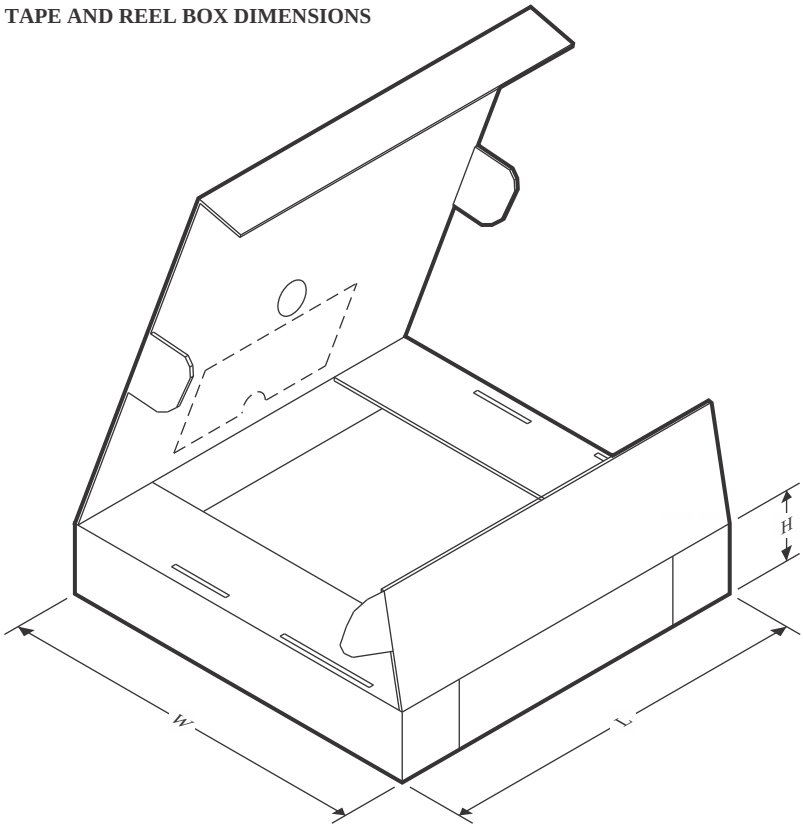
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

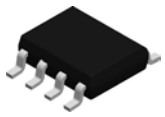
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2724AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2724AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

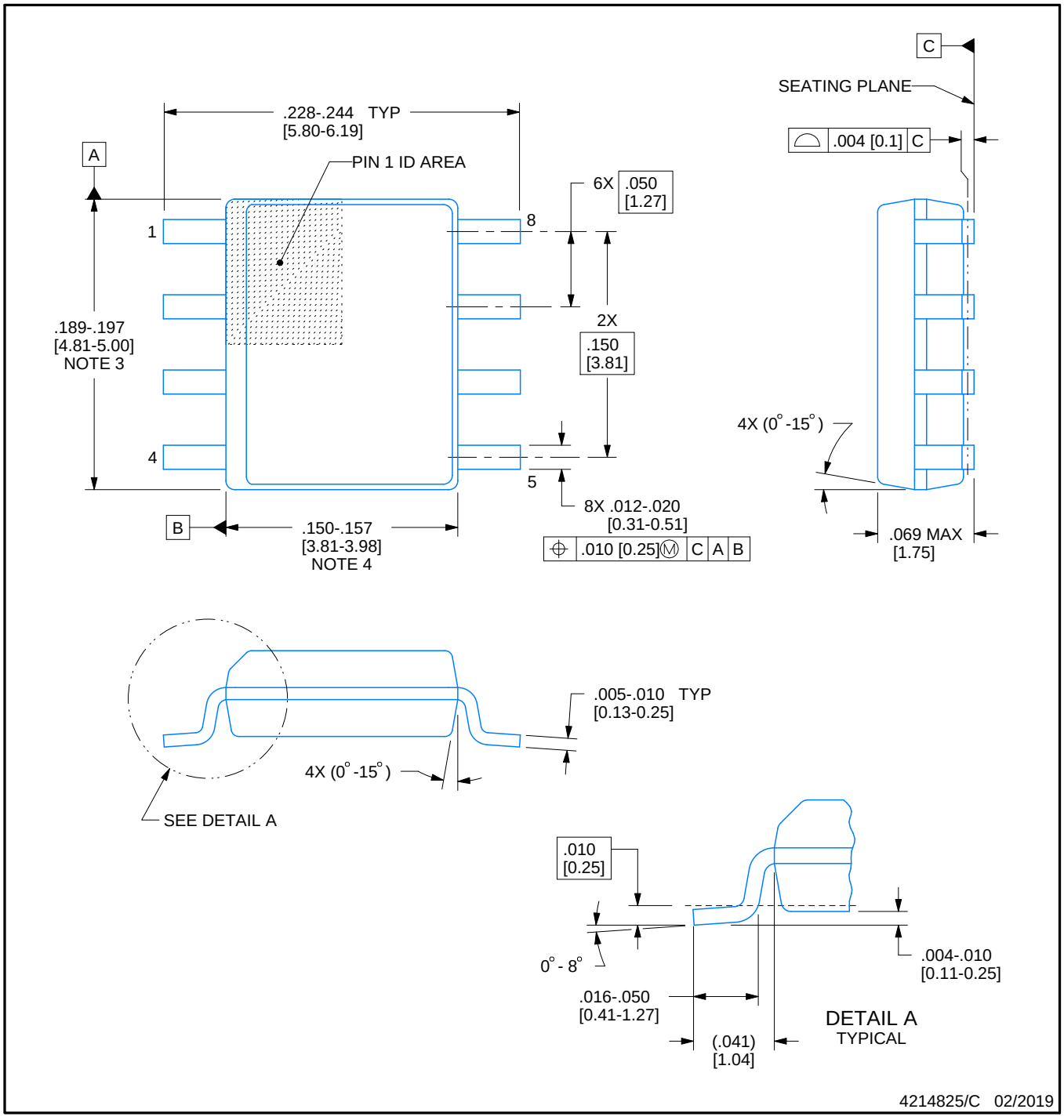


PACKAGE OUTLINE

D0008A

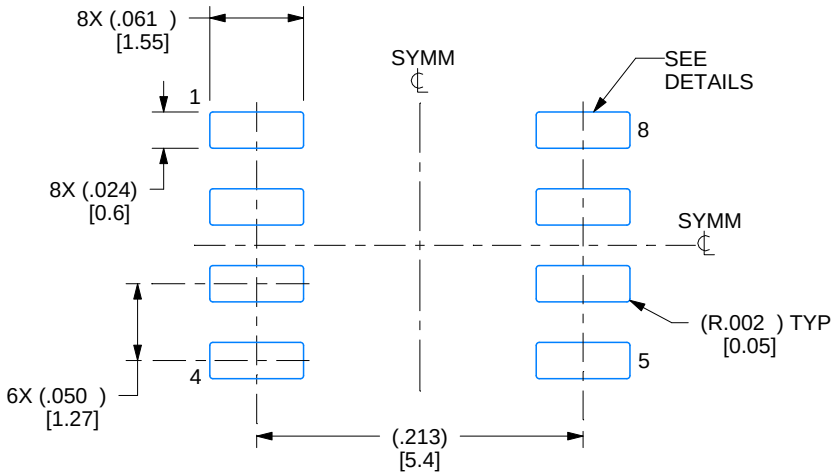
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

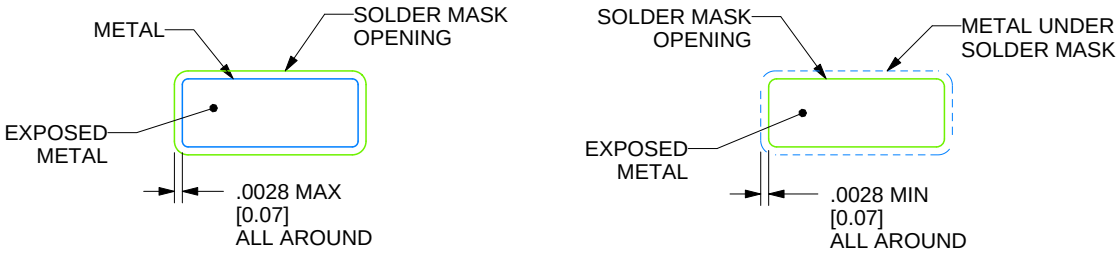


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

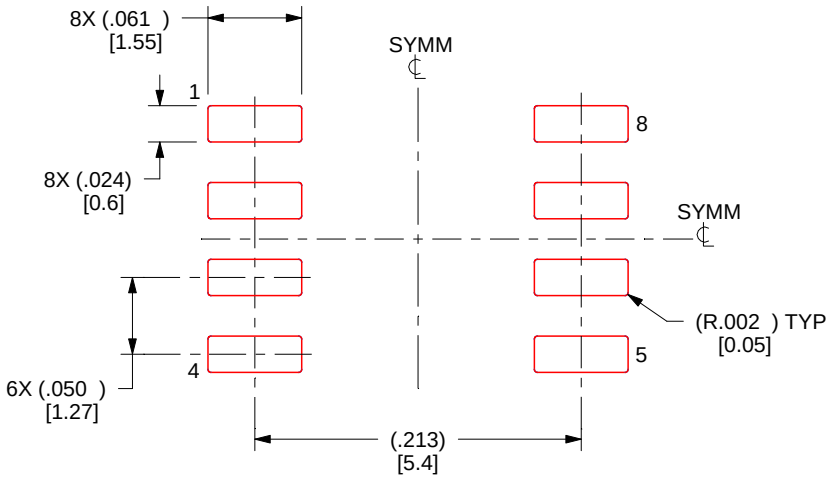
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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