

Features

- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40°C to +85°C
 - Automotive-A: -40°C to +85°C
 - Automotive-E: -40°C to +125°C
- Wide voltage range: 2.20V to 3.60V
- Pin compatible with CY62136V, CY62136CV30/CV33, and CY62136EV30
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 5 μ A (Industrial)
- Ultra low active power
 - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

The CY62136FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an

automatic power down feature that significantly reduces power consumption by 90 percent when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

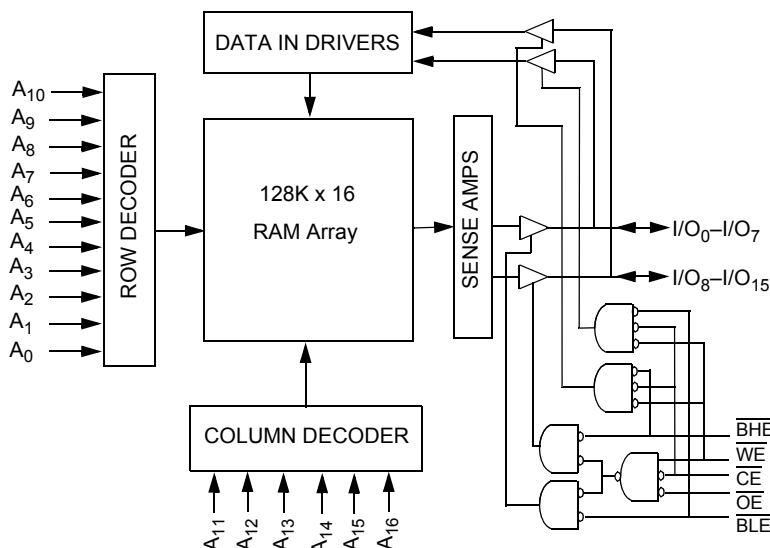
- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064](#), [SRAM System Guidelines](#).

Logic Block Diagram



Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1 MHz		f = f _{max}							
		Min	Typ ^[1]	Max		Typ ^[1]	Max	Typ ^[1]	Max	Typ ^[1]	Max
CY62136FV30LL	Industrial/Auto-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5
	Auto-E	2.2	3.0	3.6	55	2	3	15	25	1	20

Pin Configuration

Figure 1. 48-Ball VFBGA Pinout ^[2, 3]

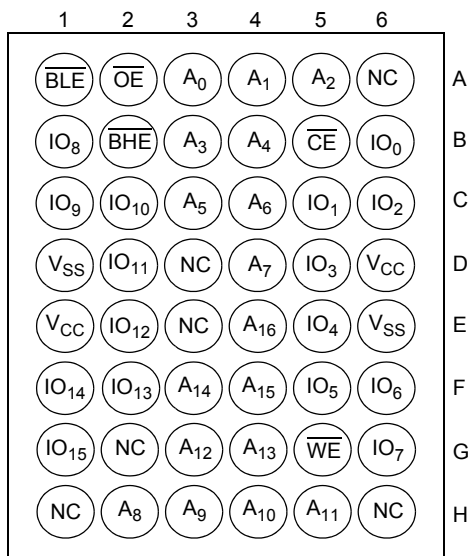
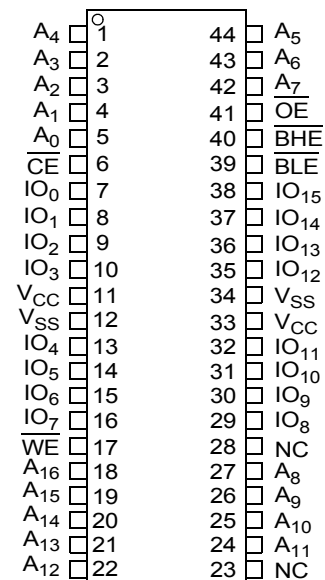


Figure 2. 44-Pin TSOP II ^[2]



Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, and H6 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to + 150°C

Ambient Temperature with

Power Applied -55°C to + 125°C

Supply Voltage to Ground

Potential -0.3V to 3.9V ($V_{CC(max)}$ + 0.3V)

DC Voltage Applied to Outputs

in High Z State ^[4, 5] -0.3V to 3.9V ($V_{CC(max)}$ + 0.3V)

DC Input Voltage ^[4, 5] -0.3V to 3.9V ($V_{CC(max)}$ + 0.3V)

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(MIL-STD-883, Method 3015)

Latch up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[6]
CY62136FV30LL	Ind'I/Auto-A	-40°C to +85°C	2.2V to 3.6V
	Auto-E	-40°C to +125°C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-45 (Industrial/Auto-A)			-55 (Auto-E)			Unit
			Min	Typ ^[1]	Max	Min	Typ ^[1]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	2.0			2.0			V
		$2.7 \leq V_{CC} \leq 3.6$							
V_{OL}	Output LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$			0.4			0.4	V
		$2.7 \leq V_{CC} \leq 3.6$							
V_{IH}	Input HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$							
V_{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$	-0.3		0.6	-0.3		0.6	V
		$2.7 \leq V_{CC} \leq 3.6$							
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	-4		+4	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$		13	18		15	25	mA
		$f = 1 \text{ MHz}$		1.6	2.5		2	3	
I_{SB1}	Automatic CE Power Down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE), $V_{CC} = 3.60V$		1	5		1	20	μA
I_{SB2} ^[7]	Automatic CE Power Down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.60V$		1	5		1	20	μA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$,	10	pF
C_{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

Notes

4. $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.

5. $V_{IH(max)}$ = $V_{CC} + 0.75V$ for pulse durations less than 20 ns.

6. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to $V_{CC(min)}$ and 200 μs wait time after V_{CC} stabilization.

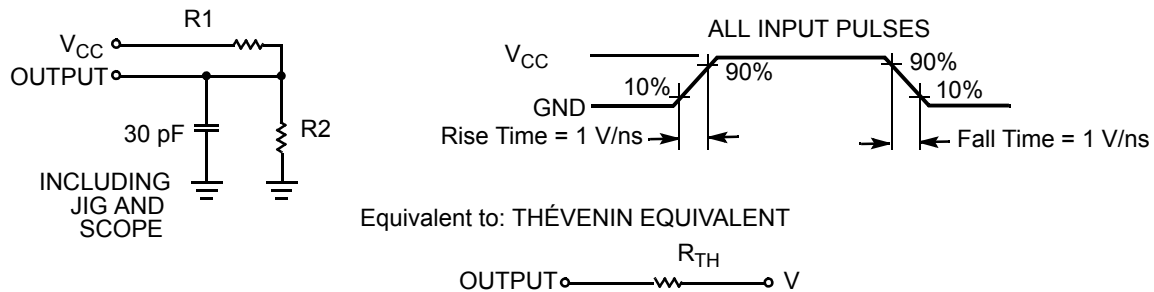
7. Only chip enable (CE) and byte enables (BHE and BLE) are tied to CMOS levels to meet the I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		10	13	°C/W

Figure 3. AC Test Loads and Waveforms



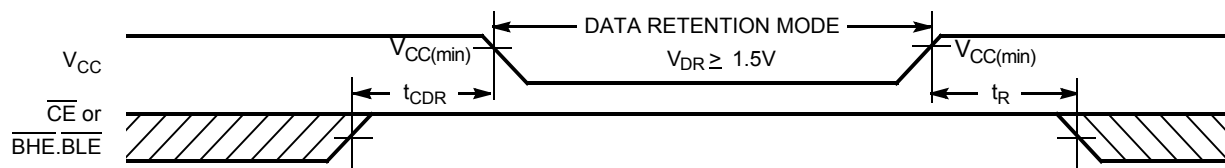
Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[1]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
$I_{CCDR}^{[7]}$	Data Retention Current	$V_{CC} = 1.5V, \overline{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			4	μA
		Industrial/Auto-A				
		Auto-E			12	
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		t_{RC}			ns

Figure 4. Data Retention Waveform^[10]



Notes

8. Tested initially and after any design or process changes that may affect these parameters.

9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100 \mu s$ or stable at $V_{CC(min)}$ $\geq 100 \mu s$.

10. $\overline{BHE.BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range ^[11, 12]

Parameter	Description	-45 (Industrial/Auto-A)		-55 (Auto-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read Cycle Time	45		55		ns
t _{AA}	Address to Data Valid		45		55	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		45		55	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		22		25	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[13]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[13, 14]		18		20	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[13]	10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[13, 14]		18		20	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power Down		45		55	ns
t _{DBE}	$\overline{\text{BLE/BHE}}$ LOW to Data Valid		22		25	ns
t _{LZBE}	$\overline{\text{BLE/BHE}}$ LOW to Low Z ^[13]	5		5		ns
t _{HZBE}	$\overline{\text{BLE/BHE}}$ HIGH to High Z ^[13, 14]		18		20	ns
Write Cycle ^[15]						
t _{WC}	Write Cycle Time	45		55		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	35		40		ns
t _{AW}	Address Setup to Write End	35		40		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Setup to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	35		40		ns
t _{BW}	$\overline{\text{BLE/BHE}}$ LOW to Write End	35		40		ns
t _{SD}	Data Setup to Write End	25		25		ns
t _{HD}	Data Hold From Write End	0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[13, 14]		18		20	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[13]	10		10		ns

Notes

11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4.
12. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. Please see application note AN13842 for further clarification.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE and/or BLE = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5. Read Cycle No.1: Address Transition Controlled. [16, 17]

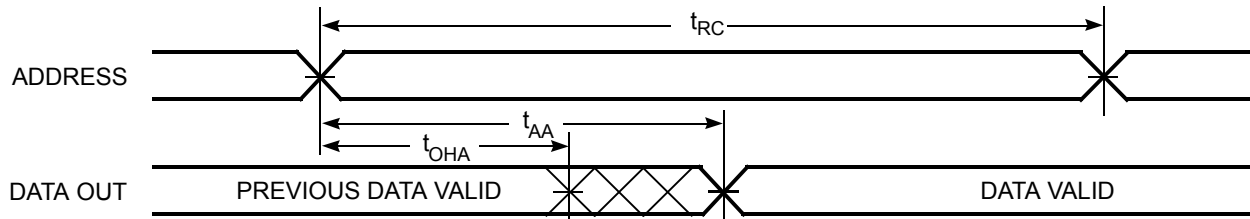
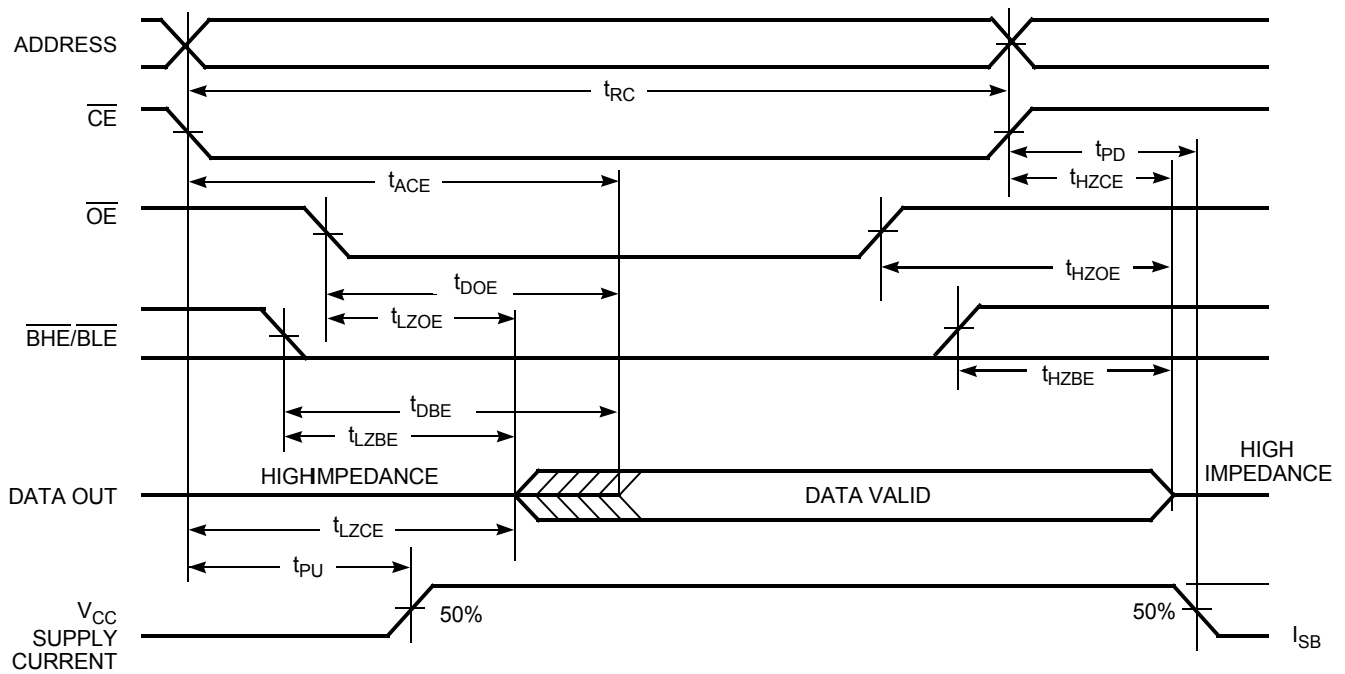


Figure 6. Read Cycle No. 2: $\overline{OE}$ Controlled [17, 18]



Notes

16. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} , $\overline{BHE}$ and $\overline{BLE}$ = V_{IL} .
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No 1: $\overline{\text{WE}}$ Controlled [15, 19, 20]

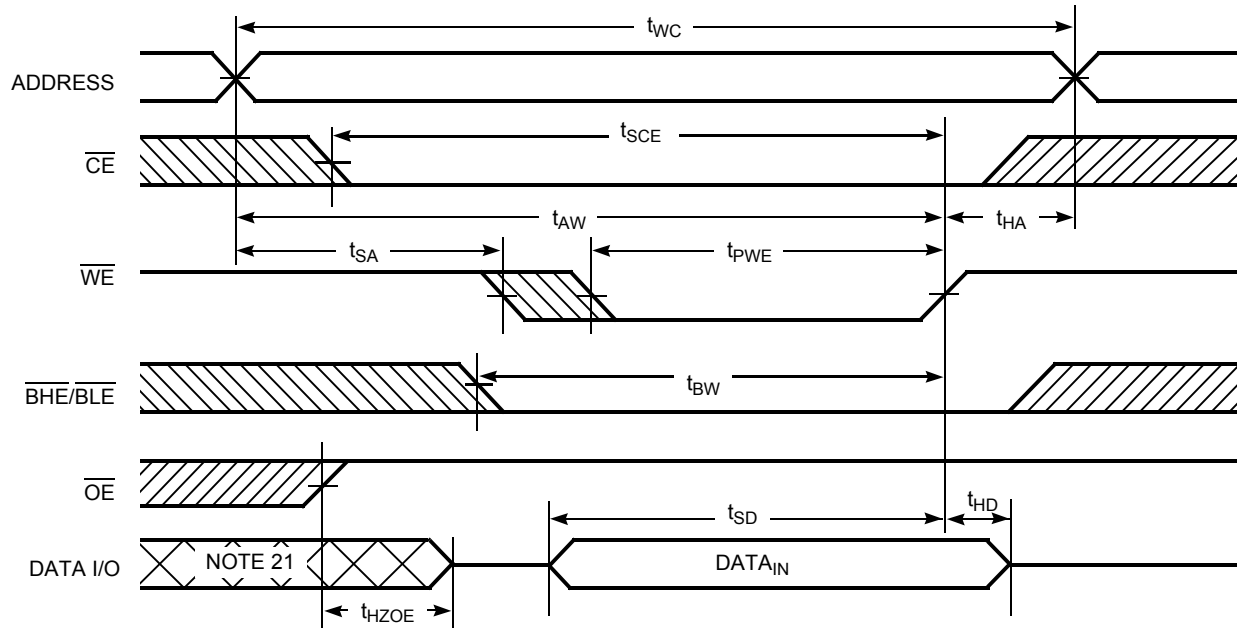
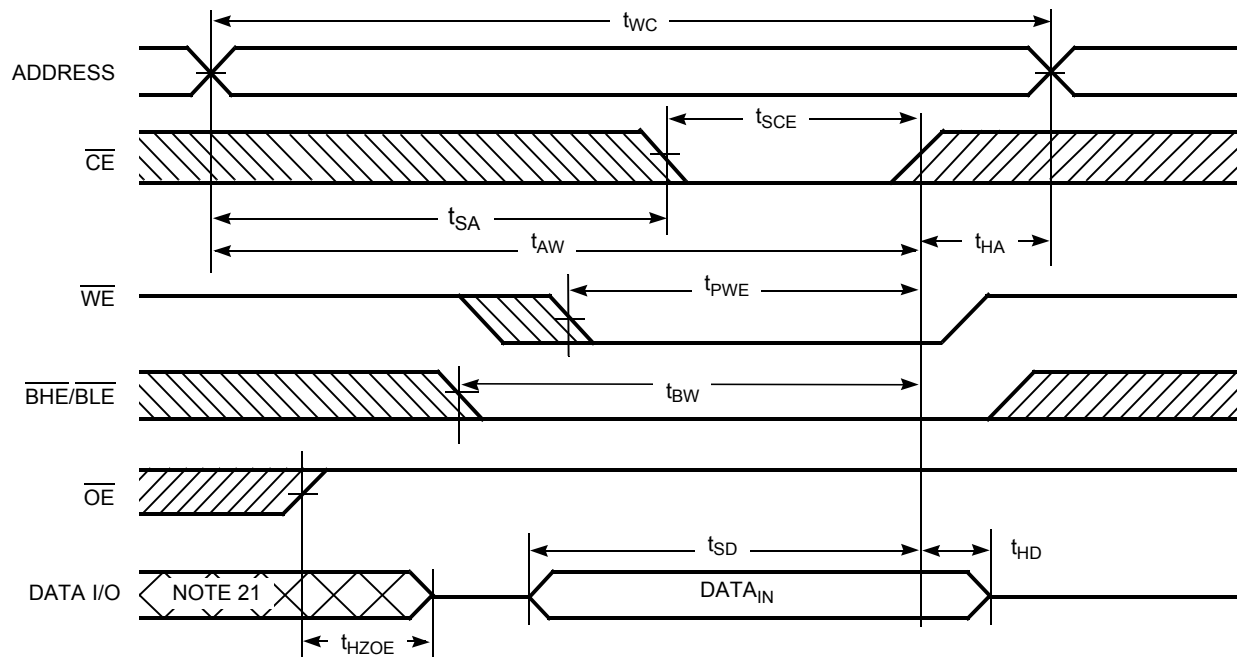


Figure 8. Write Cycle 2: $\overline{\text{CE}}$ Controlled [15, 19, 20]



Notes

19. Data IO is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
20. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\text{WE} = V_{\text{IH}}$, the output remains in a high impedance state.
21. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle 3: $\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW [20]

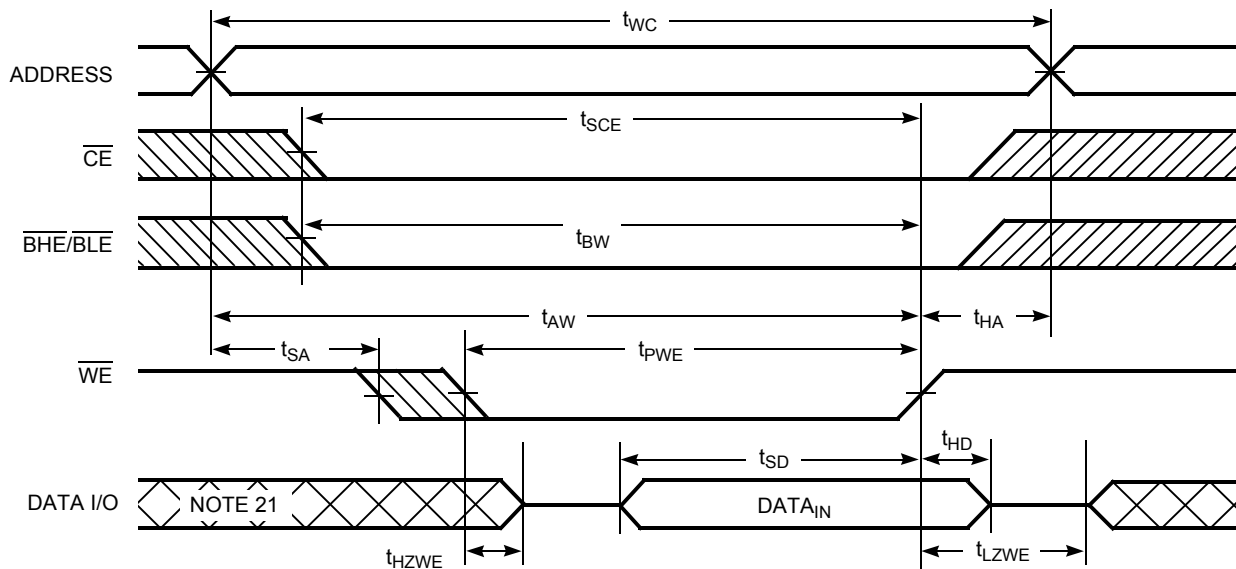
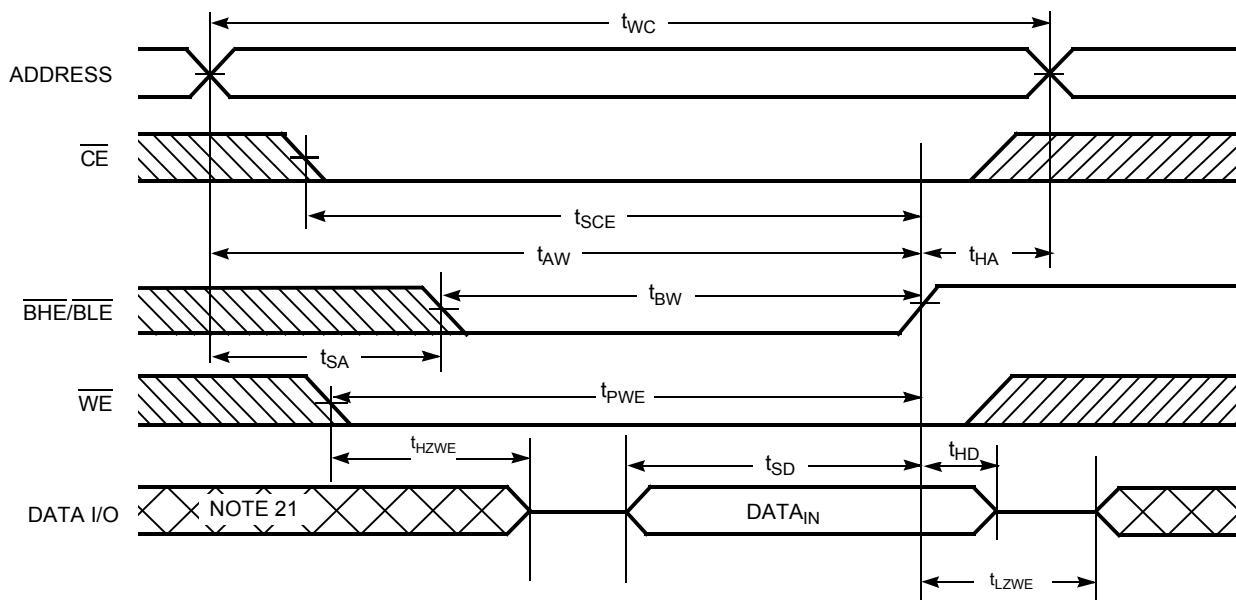


Figure 10. Write Cycle 4: $\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW [20]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs or Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect or Power Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect or Power Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

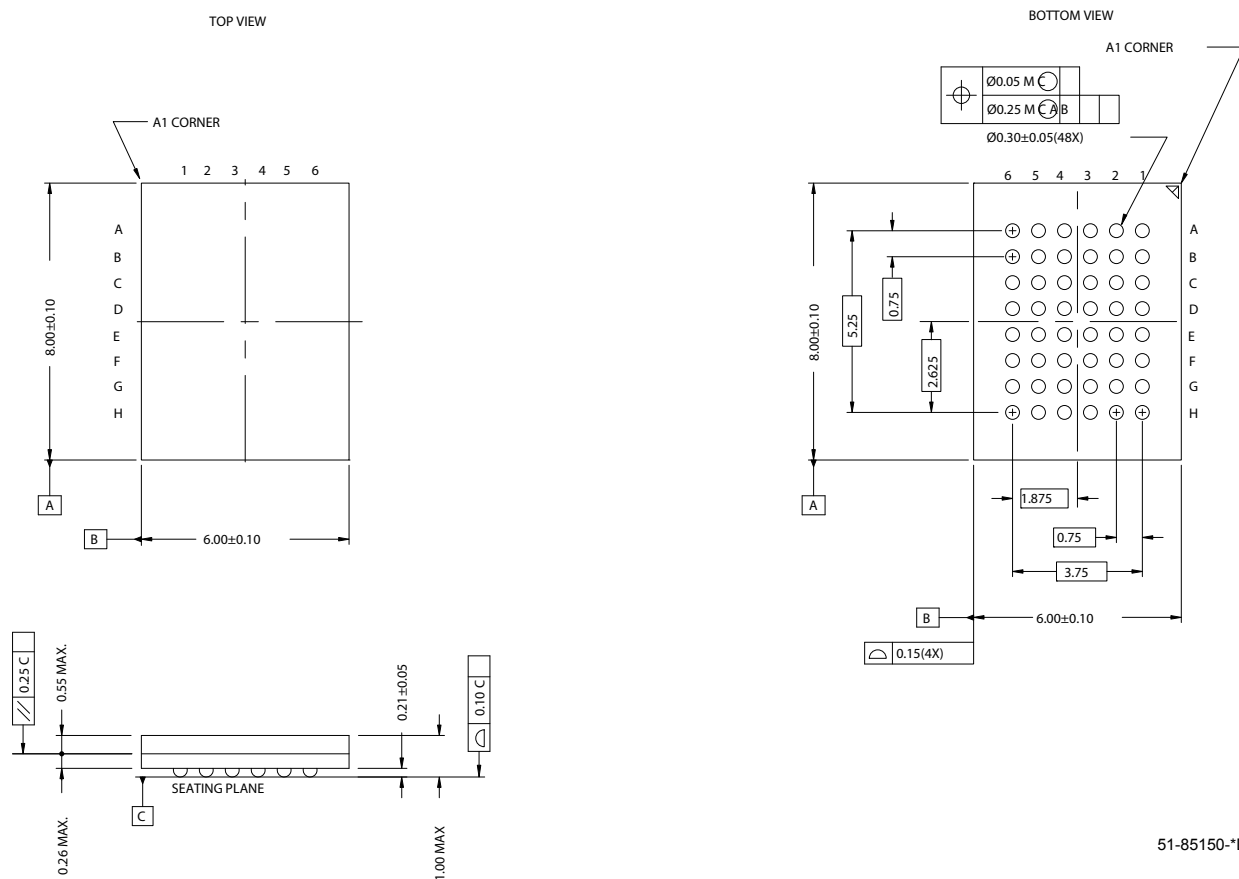
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136FV30LL-45BVXI	51-85150	48-Ball VFBGA (Pb-Free)	Industrial
	CY62136FV30LL-45ZSXI	51-85087	44-Pin TSOP II (Pb-Free)	
	CY62136FV30LL-45ZSXA	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-A
55	CY62136FV30LL-55ZSXE	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

Package Diagrams

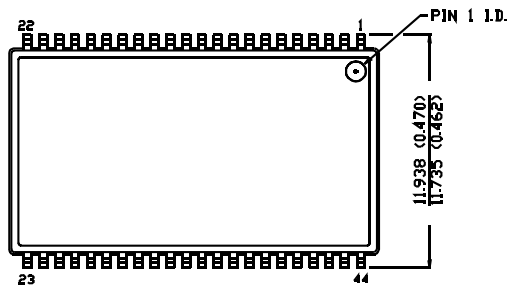
Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm)



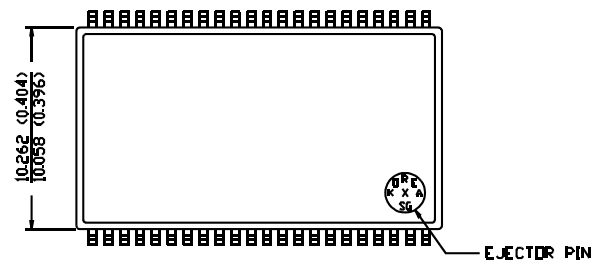
Package Diagrams (continued)

Figure 12. 44-Pin TSOP II

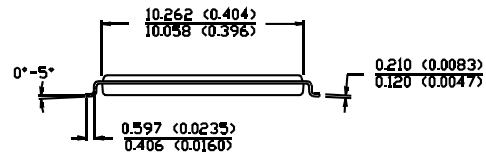
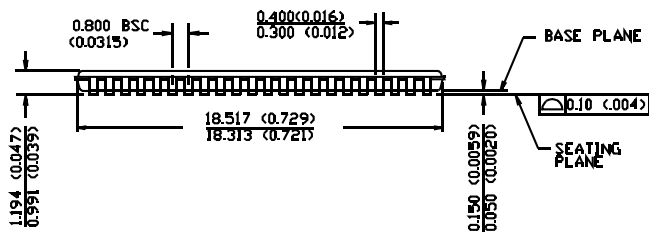
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-*A

Document History Page

Document Title: CY62136FV30 MoBL® 2 Mbit (128K x 16) Static RAM Document Number: 001-08402				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	467351	See ECN	NXR	New datasheet
*A	797956	See ECN	VKN	Converted from preliminary to final Changed $I_{SB1(typ)}$ and $I_{SB1(max)}$ specification from 0.5 μA to 1.0 μA and 2.5 μA to 5.0 μA , respectively Changed $I_{SB2(typ)}$ and $I_{SB2(max)}$ specification from 0.5 μA to 1.0 μA and 2.5 μA to 5.0 μA , respectively Changed $I_{CCDR(typ)}$ and $I_{CCDR(max)}$ specification from 0.5 μA to 1.0 μA and 2.5 μA to 4.0 μA , respectively Changed $I_{CC(max)}$ specification from 2.25 μA to 2.5 μA
*B	869500	See ECN	VKN	Added Automotive information Updated Ordering information table Added footnote 12 related to t_{ACE}
*C	901800	See ECN	VKN	Added footnote 9 related to I_{SB2} and I_{CCDR} Made footnote 13 applicable to AC parameters from t_{ACE}
*D	1371124	See ECN	VKN/AESA	Converted Automotive information from preliminary to final Changed I_{IX} min spec from -1 μA to -4 μA and I_{IX} max spec from +1 μA to +4 μA Changed I_{OZ} min spec from -1 μA to -4 μA and I_{OZ} max spec from +1 μA to +4 μA Changed t_{DBE} spec from 55 ns to 25 ns for automotive part
*E	2594937	10/22/08	NXR/PYRS	Added Automotive-A information Changed t_{LZBE} from 10 ns to 5 ns for -55.
*F	2675375	03/17/2009	VKN/PYRS	Corrected typo on page 2 (Corrected I_{SB2} unit to μA from mA)

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2006-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.