

BUK7Y13-40B

N-channel TrenchMOS standard level FET

Rev. 03 — 26 May 2008

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- 175 °C rated
- Suitable for standard level gate drive sources
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- Automotive ABS systems
- Fuel pump and injection
- Air bag
- Automotive transmission control
- Motors, lamps and solenoids

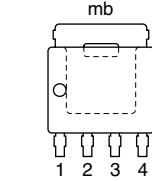
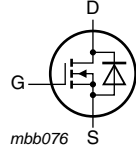
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 and 4	-	-	58	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	85	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 14	-	5	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13 and 12	-	11	13	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 58\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	85	mJ

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1, 2, 3	S	source	 <p>SOT669 (LPAK)</p>	 <p>mbb076</p>
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7Y13-40B	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 4	-	58	A
		$T_{mb} = 175\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	41	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 4	-	234	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	85	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C

Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 58\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	85	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[1] [2] [3]	-	J

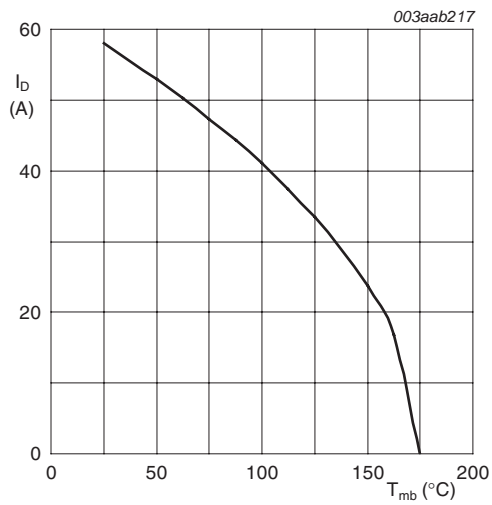
Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$	-	58	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	234	A

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

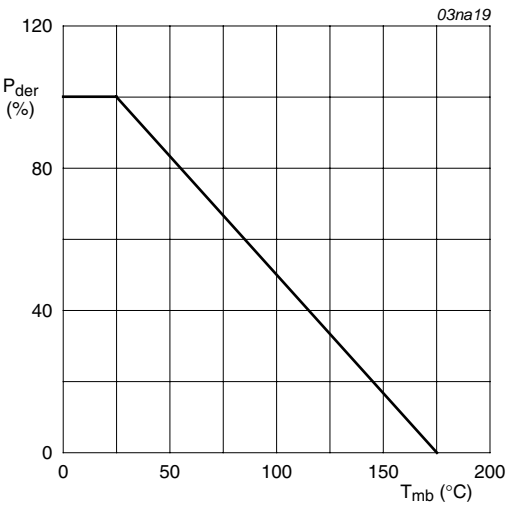
[2] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.



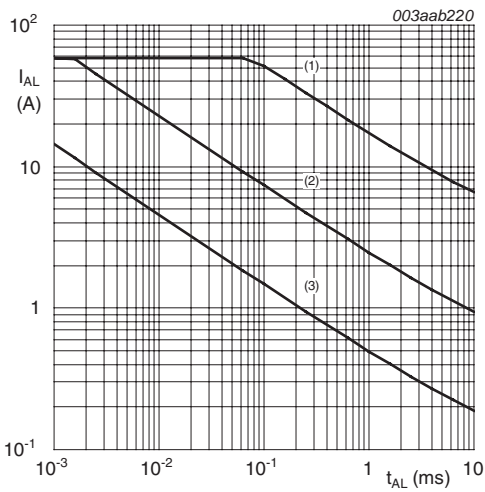
$V_{GS} \geq 10\text{ V}$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



- (1) Single-pulse; $T_j = 25\text{ }^{\circ}C$.
- (2) Single-pulse; $T_j = 150\text{ }^{\circ}C$.
- (3) Repetitive.

Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period

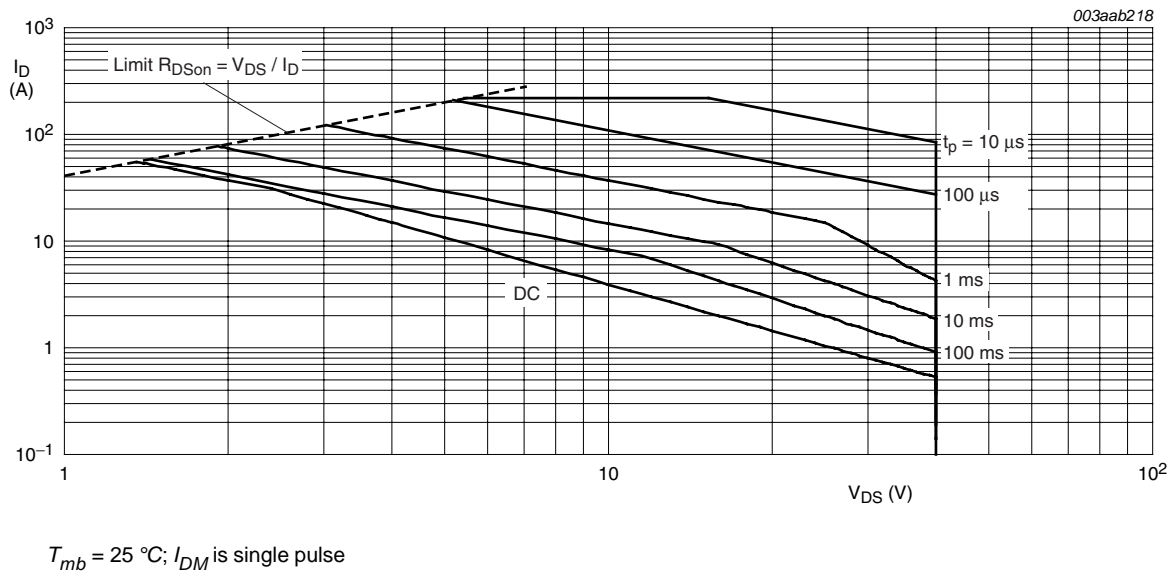


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.8	K/W

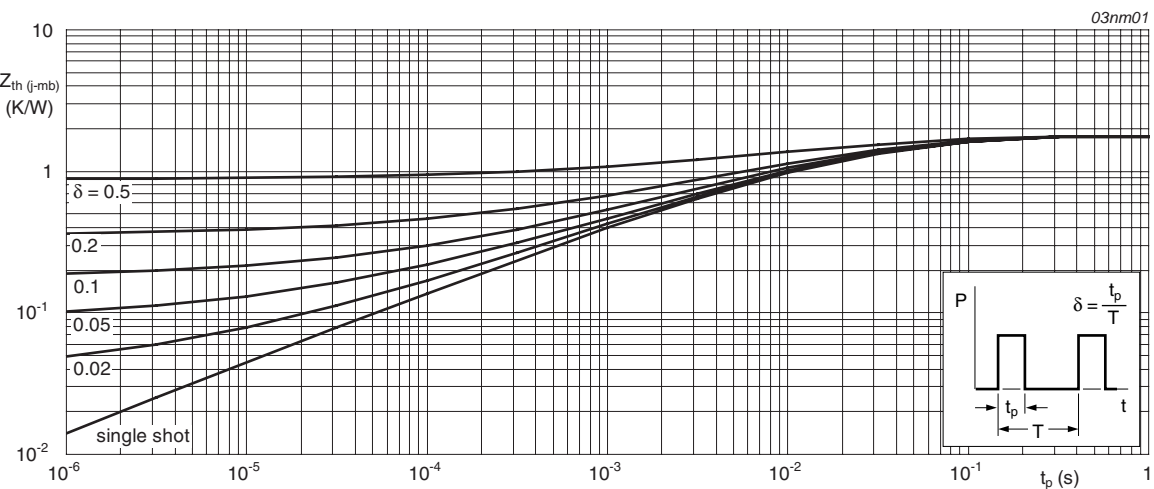


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10 and 11	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	4.4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 20 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -20 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 12	-	-	25	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 13 and 12	-	11	13	mΩ
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 25 V; T _j = 25 °C; see Figure 16	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = 100 A/μs;	-	41	-	ns
Q _r	recovered charge	V _{GS} = 0 V; V _{DS} = 30 V	-	22	-	nC
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V;	-	19	-	nC
Q _{GS}	gate-source charge	V _{GS} = 10 V; see Figure 14	-	6	-	nC
Q _{GD}	gate-drain charge		-	5	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V;	-	983	1311	pF
C _{oss}	output capacitance	f = 1 MHz; T _j = 25 °C; see Figure 15	-	280	336	pF
C _{rss}	reverse transfer capacitance		-	138	189	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 2.5 Ω;	-	9	-	ns
t _r	rise time	V _{GS} = 10 V; R _{G(ext)} = 10 Ω	-	25	-	ns
t _{d(off)}	turn-off delay time		-	35	-	ns
t _f	fall time		-	27	-	ns

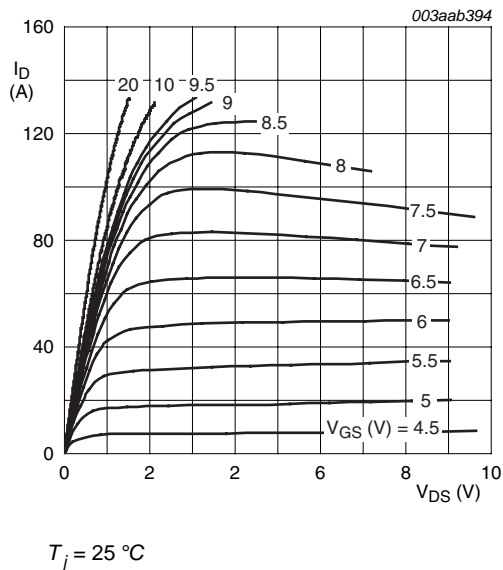


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

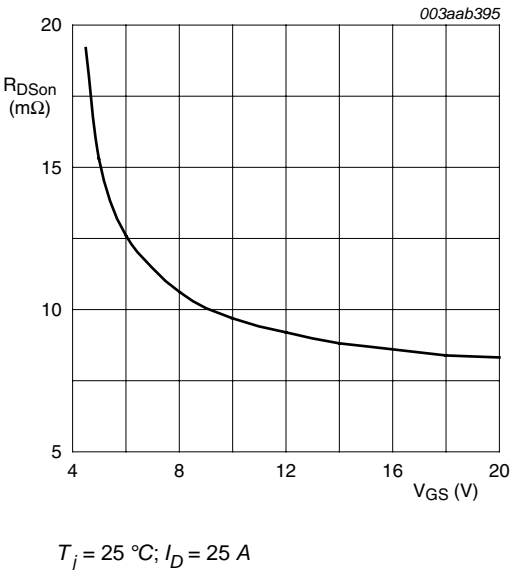


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

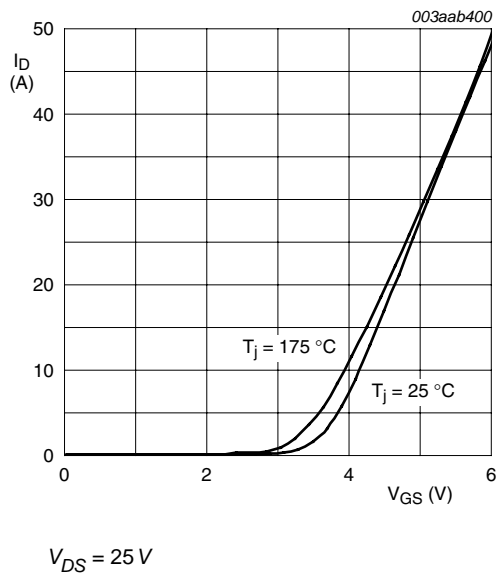


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

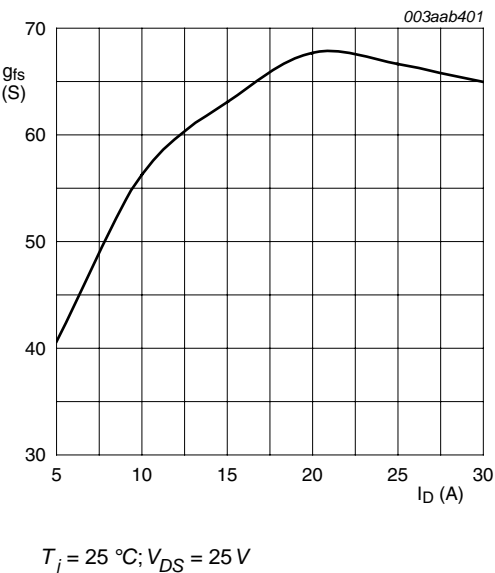
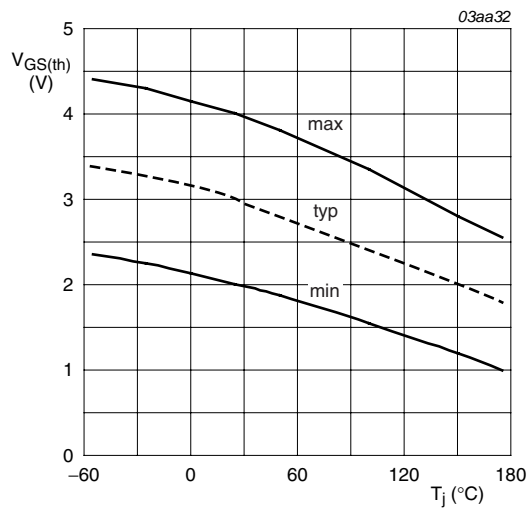
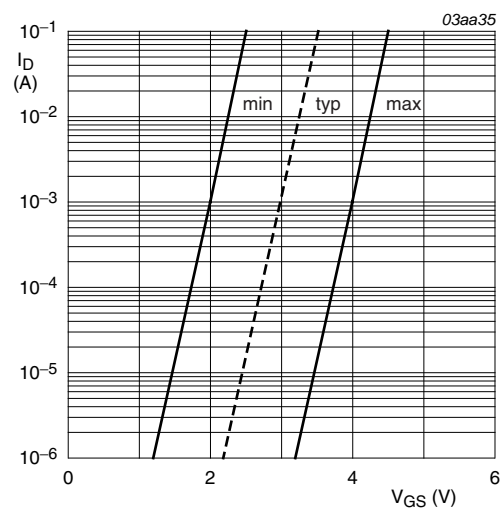


Fig 9. Forward transconductance as a function of drain current; typical values



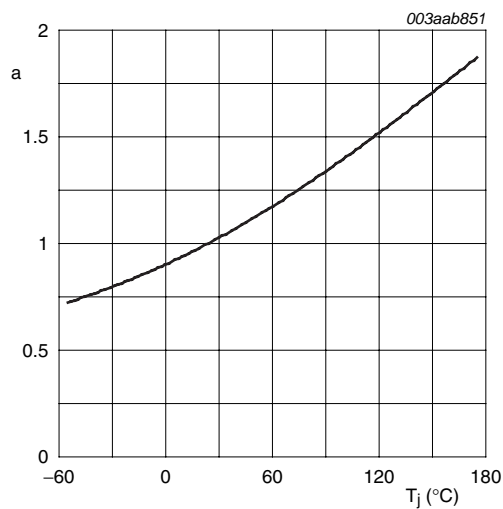
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



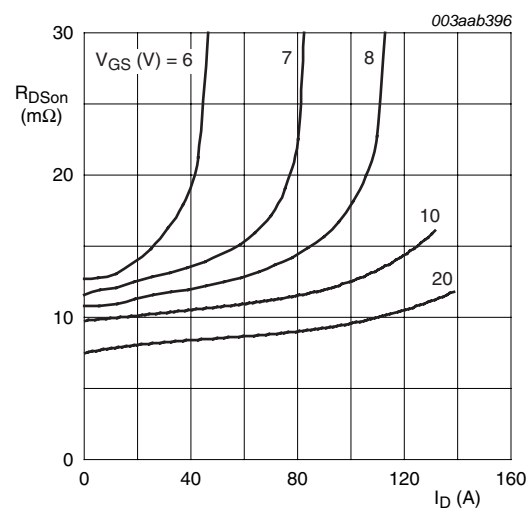
$T_j = 25\text{ °C}; V_{DS} = V_{GS}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



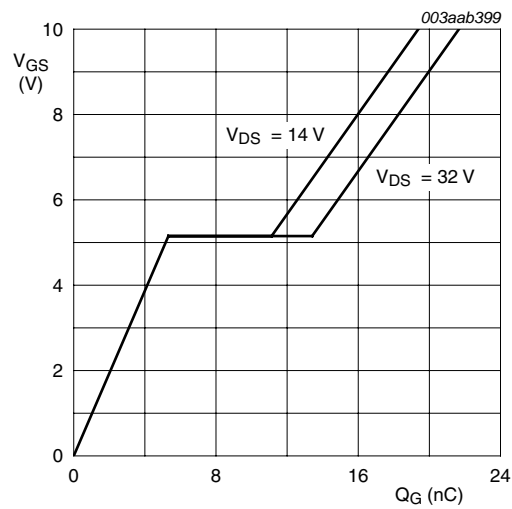
$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



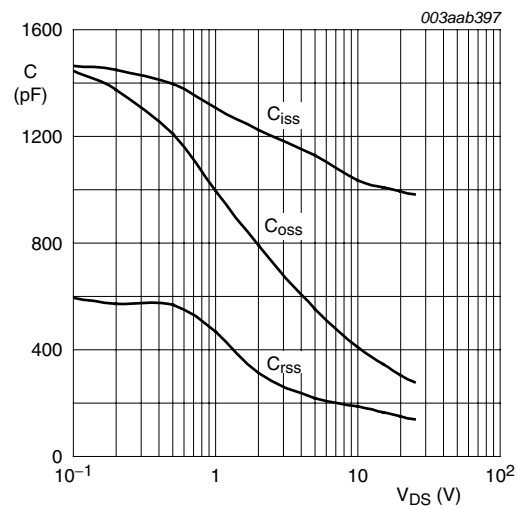
$T_j = 25\text{ °C}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



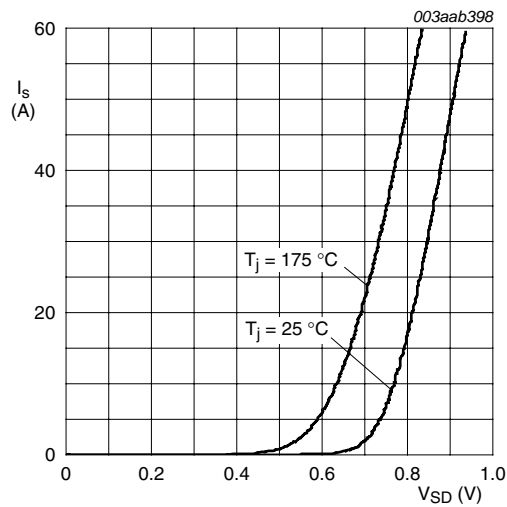
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 10\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

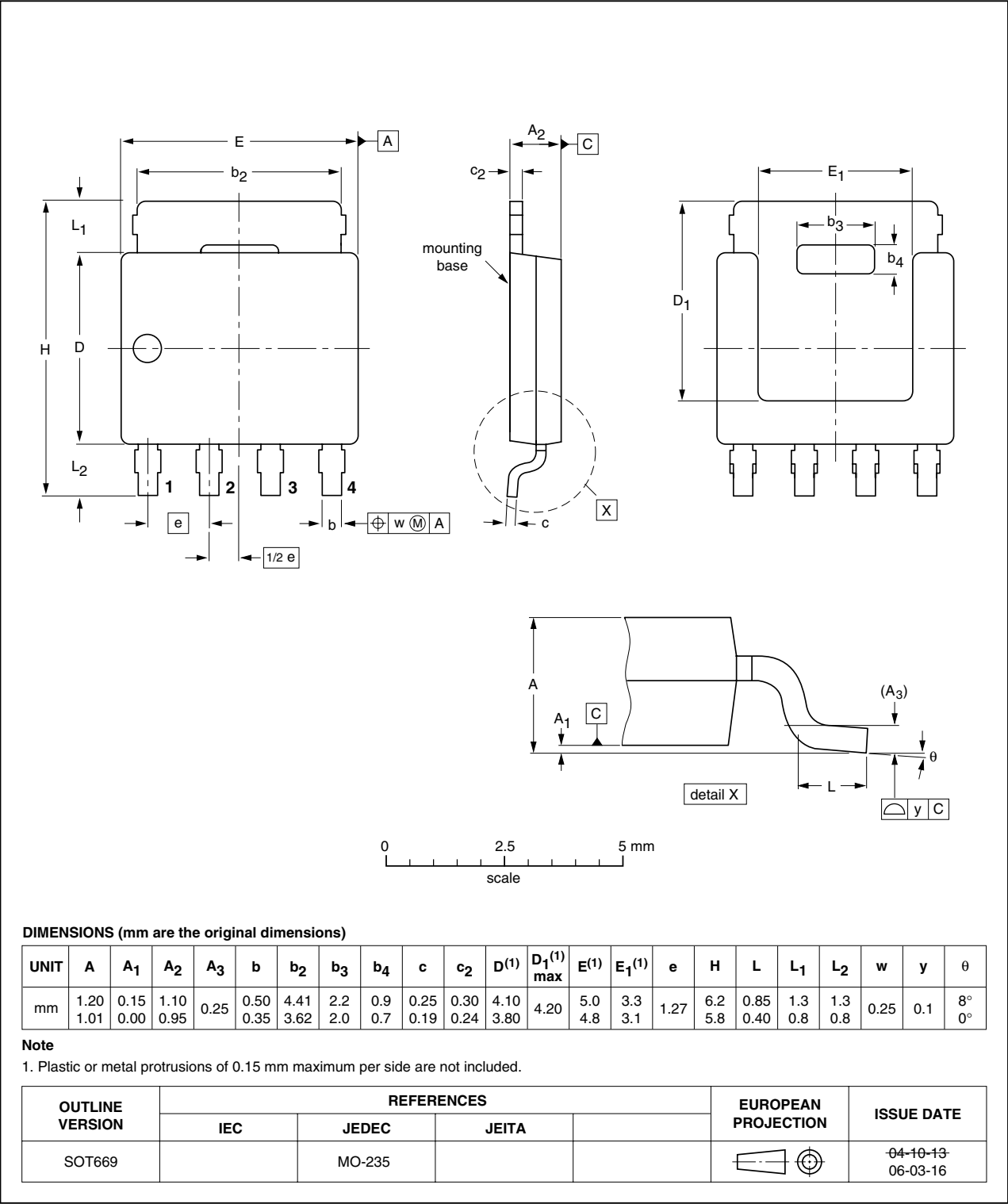


Fig 17. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7Y13-40B_3	20080526	Product data sheet	-	BUK7Y13-40B_2
Modifications:	• Table 5 , maximum thermal resistance value updated			
BUK7Y13-40B_2	20071002	Product data sheet	-	BUK7Y13-40B_1
BUK7Y13-40B_1	20070924	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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