SILICON POWER

C501 / C502
33mm Thyristors
2200V / 550A

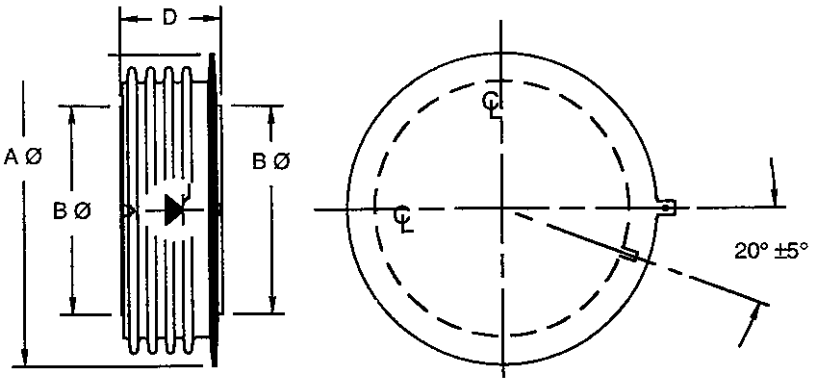
The C501 & C502 are ideal for phase control applications and processed by multidiffusion, untilizing 33mm diameter silicon and a unique pilot gate. They are supplied in a disk package ready to mount using commercially available heat dissipators and mechanical clamping hardware.

MAXIMUM ALLOWABLE VOLTAGE RATINGS

TYPE	Repetitive Peak Off-State and Reverse Voltage V_{DRM} / V_{RRM} Tj = -40° to +125°C	Repetitive Peak Off-State and Reverse Voltage V_{DRM} / V_{RRM} Tj = 0 to +125°C
C501P	1000	1100
C501PA	1100	1200
C501PB	1200	1300
C501PC	1300	1400
C501PD	1400	1500
C501PE	1500	1600
C501PM	1600	1700
C501PS	1700	1800
C502PN	1800	1900
C502PY	1900	2000
C502L	2000	2100
C502LA	2100	2200
C502LB	2200	2300

Average Forward Current, On-State . . . . . Depends on Conduction Angle (See Charts 1 and 3)
Peak One-Cycle Surge On-State Current, I_{TSM} . . . . . 8000 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval (See Chart 11)
(Switching Rates ⩽ 60 Hz) . . . . . Switch From < 500V 175A/μsec
. . . . . Switch From <1000V 100A/μsec
. . . . . Switch From <1300V 80A/μsec
I^2t (for fusing) (for times ⩾ 1.5 milliseconds) . . . . . 130,000 Ampere² Seconds
I^2t (for fusing) (at 8.3 milliseconds) . . . . . 260,000 Ampere² Seconds
Peak Gate Power Dissipation, P_{GM} . . . . . 25 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 5 Watts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 Volts
Storage Temperature, T_{STG} . . . . . -40°C to +125°C
Operating Temperature, T_J . . . . . -40°C to +125°C
Mounting Force Required . . . . . 2200 Lbs. ± 10%
8.9 KN ± 10%

A Ø = 2.00 in (50.8 mm)
B Ø = 1.26 in (32.0 mm)
D = 1.02 in (25.8 mm)



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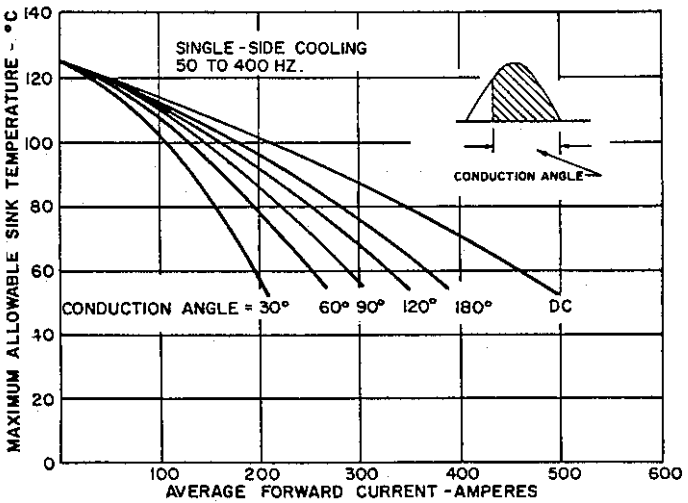
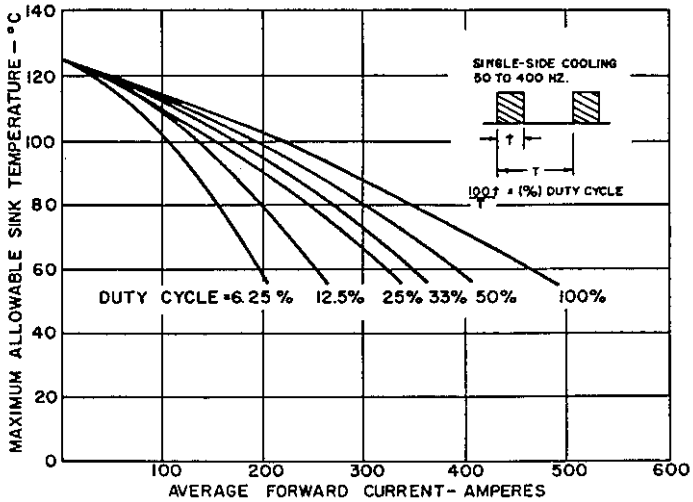
CHARACTERISTICS

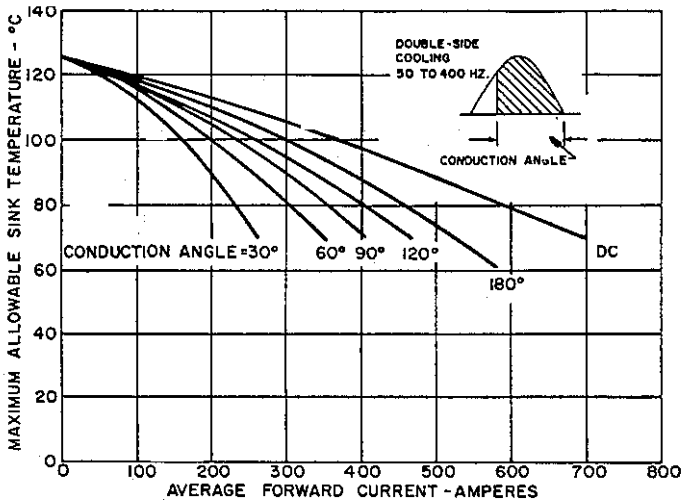
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and Forward Blocking Current	I_{DRM} and I_{RRM}	–	1.0	15	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Peak Reverse and On-State Blocking Current	I_{DRM} and I_{RRM}	–	15	35	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance, Junction-to-Case	$R\theta_{JC}$	–	–	.05	°C/Watt	Junction-to-Case – Double Side Cooling (DC)
Critical Exponential Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	100	–	–	V/μsec	T_J = +125°C, V_{DRM} = 0.8 Rated, Gate Open.
Holding Current	I_H	–	100	250	mAdc	T_C = +25°C, Anode supply = 20 Vdc. Initial forward current = 500 amps.
Latching Current	I_L	–	–	1	Adc	T_C = +25°C, Anode supply = 24 Vdc, Load resistance 12 ohms max.
Delay Time	t_d	–	1.5	3	μsec	T_C = +25°C, Bias voltage = 960V, Gate supply: 20V, 10 ohms, 0.5 μsec max. rise time.
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	T_C = +25°C. Gate Supply: 10 volt open circuit, 5 ohm, 0.1 μsec rise time.
Gate Trigger Current	I_{GT}	–	–	150	mAdc	T_C = +25°C, V_D = 10 Vdc, R_L = 3 ohms
		–	–	225		T_C = -40°C, V_D = 10 Vdc, R_L = 3 ohms
		–	5	75		T_C = +120°C, V_D = 10 Vdc, R_L = 3 ohms
Gate Trigger Voltage	V_{GT}	–	–	6.5	Vdc	T_C = -40°C to +125°C, V_D = 10 Vdc, R_L = 3 ohms
		0.15	–	–		T_C = +125°C, V_D = Rated, R_L = 1000 ohms
Peak On-State Voltage	V_{TM}	–	–	1.53	Volts	T_C = +25°C, I_T = 1000 amps. peak. Duty cycle ≤ 0.01%
Circuited Commutated Turn-Off Time	t_q	–	300	200	μsec	(1) T_C = +125°C (2) I_T = 450 Amps. (3) V_R = 75 Volts min. (4) 0.5 V_{DRM} Reapplied (5) Rate-of-rise of reapplied forward blocking voltage = 25V/μsec (linear) (6) Gate bias during turn-off interval, Duty cycle ≤ 0.01%



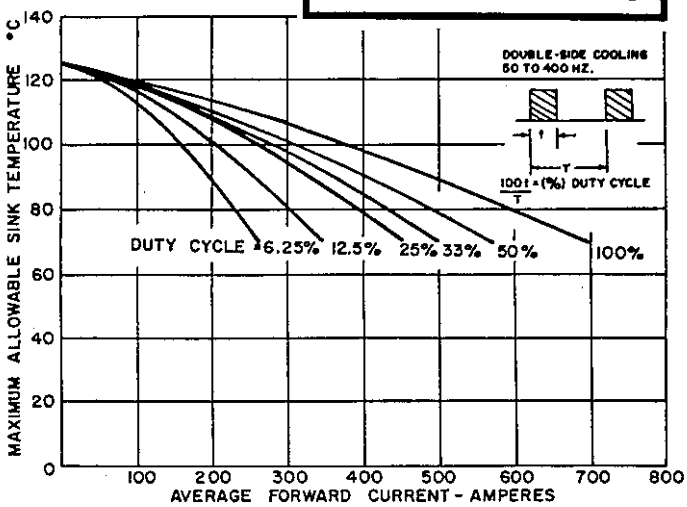
1. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM (SINGLE-SIDE COOLED)



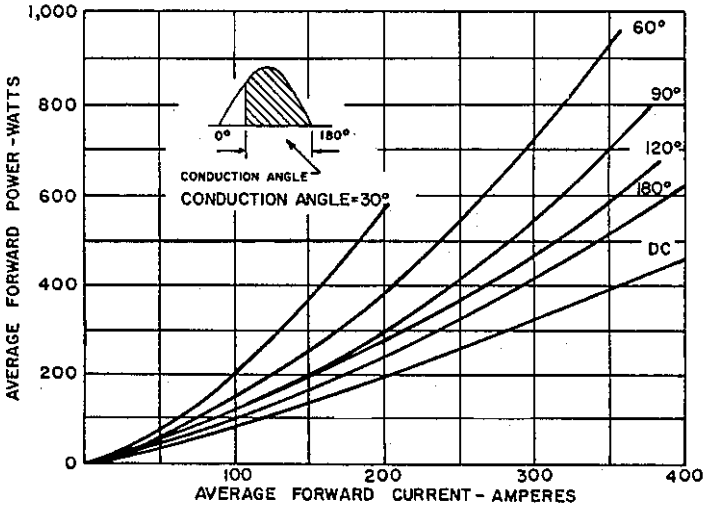
2. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM (SINGLE-SIDE COOLED)



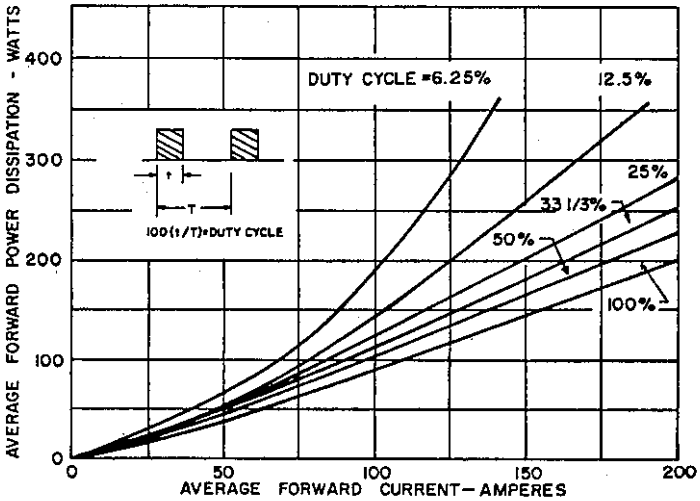
3. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM (DOUBLE-SIDE COOLED)



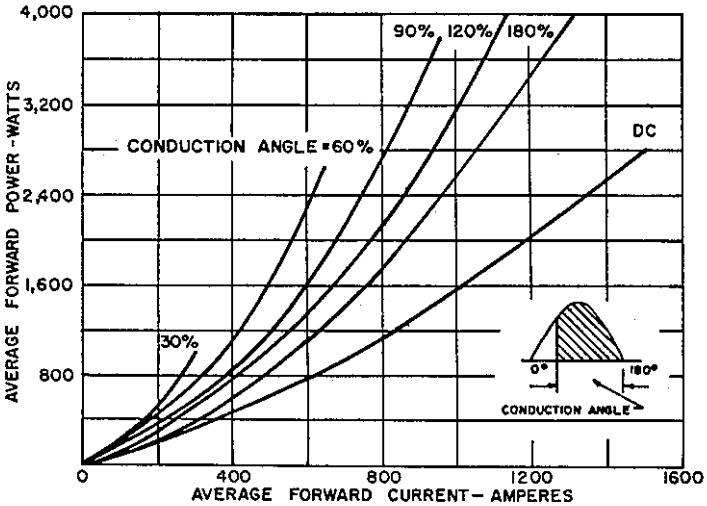
4. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM (DOUBLE-SIDE COOLED)



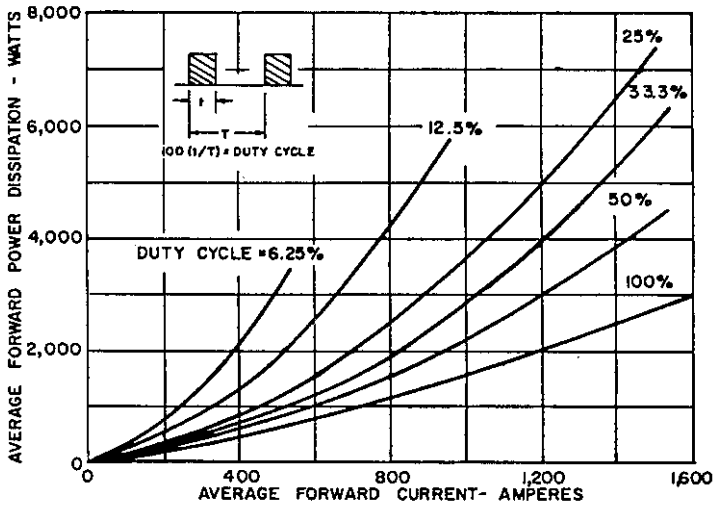
5. AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



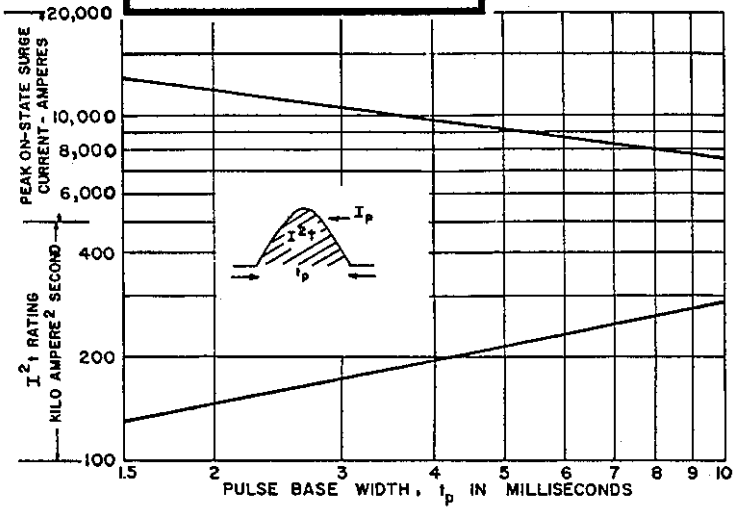
6. AVERAGE FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



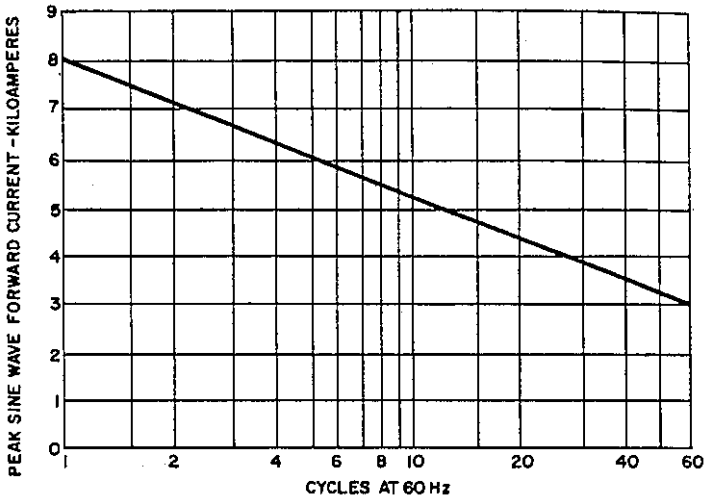
7. EXTENDED FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



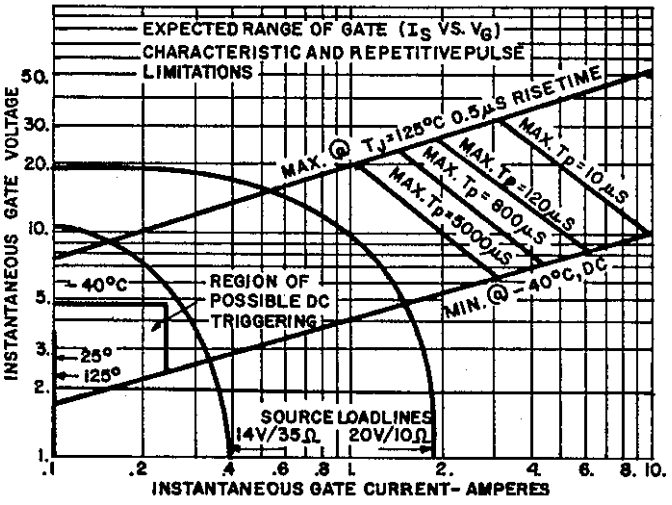
8. EXTENDED FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



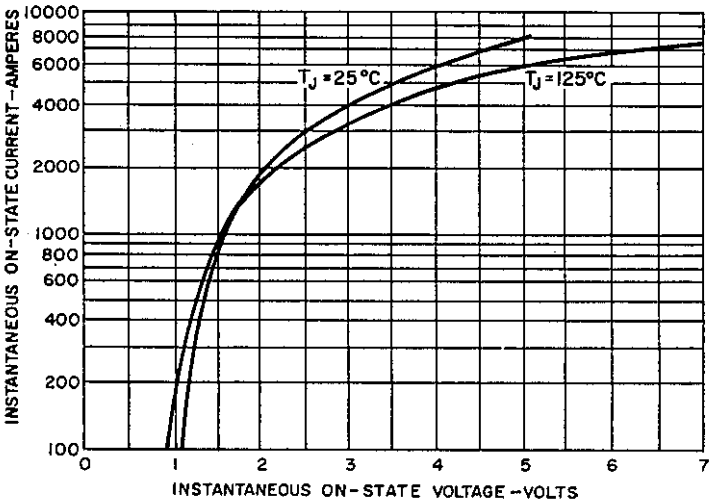
9. SUB-CYCLE SURGE AND I^2t RATING FOLLOWING RATED LOAD CONDITIONS



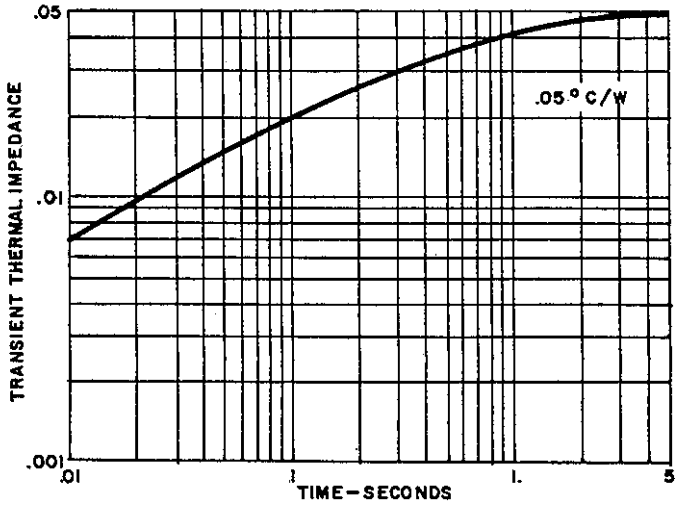
10. MAXIMUM ALLOWABLE SURGE CURRENT FOLLOWING RATED LOAD CONDITIONS



11. GATE TRIGGERING CHARACTERISTICS



12. FORWARD CONDUCTION CHARACTERISTIC (ON-STATE)



13. TRANSIENT THERMAL IMPEDANCE – JUNCTION-TO-CASE

NOTES:

1. Add .01°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R\theta_{JS}$ = .06°C.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
   - end of conducting portion of cycle
     - 120° sq. wave add .0065°C/W along entire curve
     - 180° sq. wave add .0047°C/W along entire curve
     - 180° sine wave add .0026° C/W along entire curve
   - end of full cycle
     - any wave, subtract .0026°C/W along entire curve

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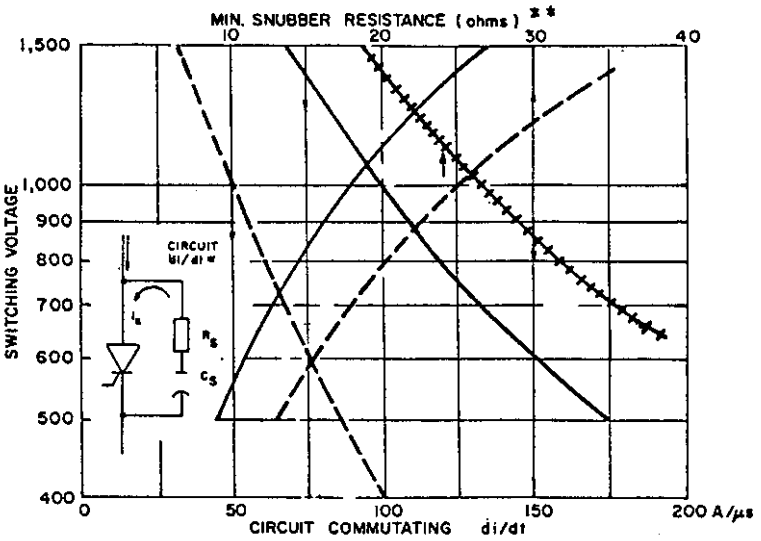

NOTES:

Code:
- +++++ Non-Repetitive High Gate Drive
- ——— Repetitive High Gate Drive
- ——— Non-Repetitive Low Gate Drive
- – – – Repetitive Low Gate Drive

	Low Gate Drive	High Gate Drive
Source	14V/35 ohms	20V/10 ohms
Pulse Width, t_p	$\geqslant$ 20 μs	$\geqslant$ 10 μs
Current Rise Time, t_r	$\leqslant$ 2	$\leqslant$ 0.5 μs

*Permissible circuit di/dt excluding snubber discharge. Repetitive di/dt is recommended maximum condition to achieve most industrial requirements for service life. It meets or exceeds the JEDEC test requirements for certification set forth in NEMA Std. Sk. 516 (1972). Non-repetitive di/dt meets the JEDEC 5 sec. rating.

**Snubber discharge, i_s, is treated separately using the minimum value of snubber resistance indicated above. This applies for long industrial life (20 – 30 years) in combination with circuit di/dt.

14. ALLOWABLE REPETITIVE AND NON-REPETITIVE IN-RUSH CURRENT (DI/DT*) AND REQUIRED SNUBBER RESISTANCE FOR VARYING LEVELS OF SWITCHING VOLTAGE