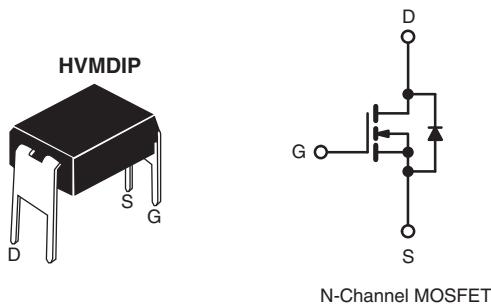


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	400
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V 3.6
$Q_g$ (Max.) (nC)	17
$Q_{gs}$ (nC)	3.4
$Q_{gd}$ (nC)	8.5
Configuration	Single

### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
COMPLIANT


### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD310PbF SiHFD310-E3
SnPb	IRFD310 SiHFD310

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	400	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	0.35	A
		0.22	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	2.8	W/°C
Linear Derating Factor		0.0083	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	46	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$	0.35	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	0.10	mJ
Maximum Power Dissipation	$P_D$	1.0	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 41$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 1.4$  A (see fig. 12).

c.  $I_{SD} \leq 2.0$  A,  $dI/dt \leq 40$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.

d. 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	120	°C/W

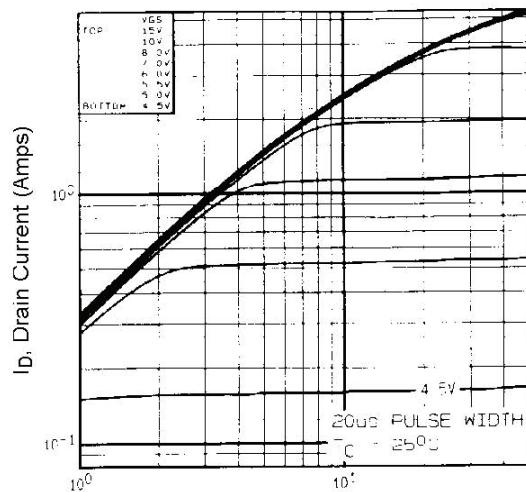
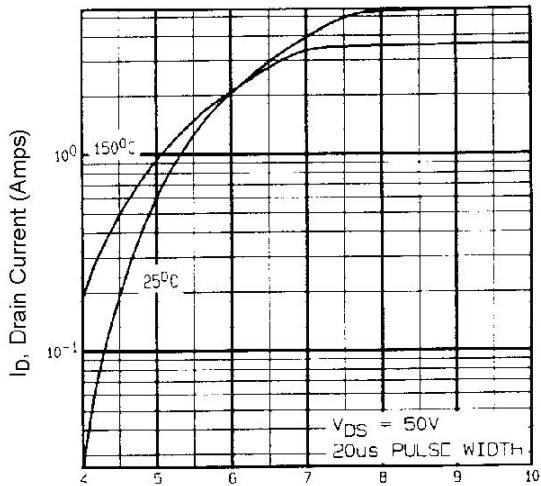
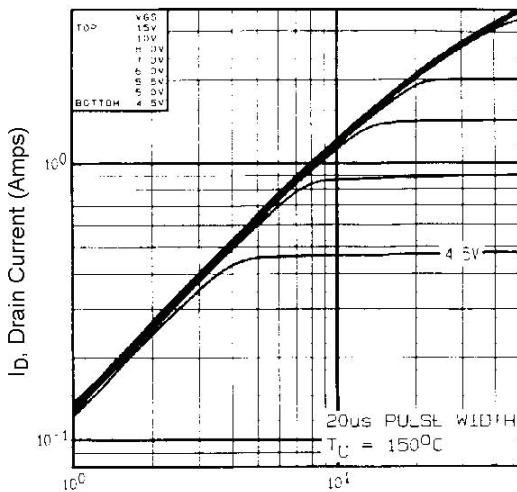
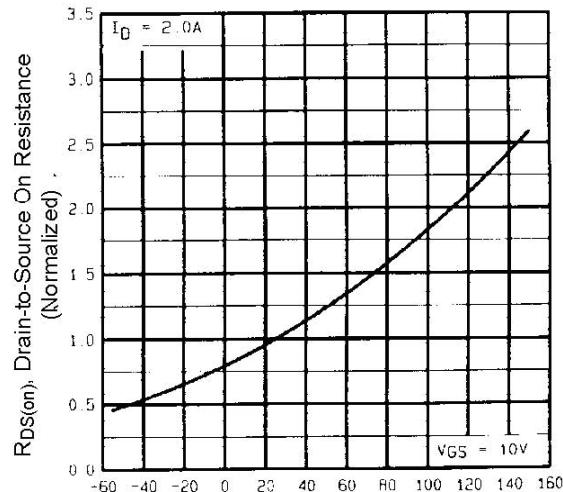
**SPECIFICATIONS** ( $T_J = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A		400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.47	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20$ V		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400$ V, $V_{GS} = 0$ V		-	-	25	$\mu$ A
		$V_{DS} = 320$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 0.21$ A <sup>b</sup>	-	-	3.6	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50$ V, $I_D = 1.2$ A		1.0	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5		-	170	-	pF
Output Capacitance	$C_{oss}$			-	34	-	
Reverse Transfer Capacitance	$C_{rss}$			-	6.3	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10$ V	$I_D = 2.0$ A, $V_{DS} = 320$ V, see fig. 6 and 13 <sup>b</sup>	-	-	17	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.4	
Gate-Drain Charge	$Q_{gd}$			-	-	8.5	
Turn-On Delay Time	$t_{d(on)}$			-	8.0	-	
Rise Time	$t_r$	$V_{DD} = 200$ V, $I_D = 2.0$ A, $R_g = 24$ $\Omega$ , $R_D = 95$ $\Omega$ , see fig. 10 <sup>b</sup>		-	9.9	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	21	-		
Fall Time	$t_f$		-	11	-		
Internal Drain Inductance	$L_D$		-	4.0	-		
Internal Source Inductance	$L_S$	Between lead, 6 mm (0.25") from package and center of die contact		-	6.0	-	nH
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	0.35	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	2.8	
Body Diode Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 0.35$ A, $V_{GS} = 0$ V <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25$ °C, $I_F = 2.0$ A, $dI/dt = 100$ A/ $\mu$ s <sup>b</sup>		-	240	540	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.85	1.6	$\mu$ C
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300$   $\mu$ s; duty cycle  $\leq 2$  %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ }^{\circ}\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_A = 150\text{ }^{\circ}\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

# IRFD310, SiHFD310

Vishay Siliconix

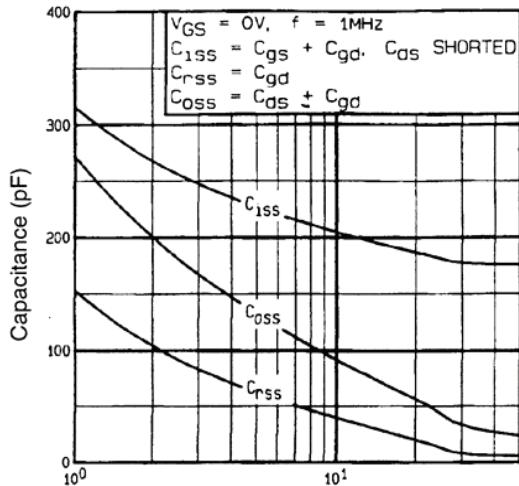


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

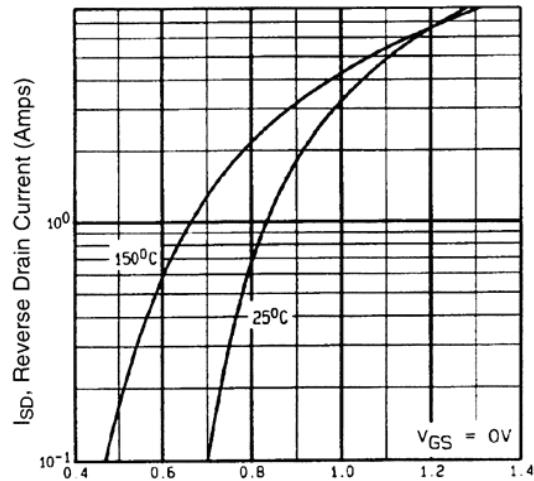


Fig. 7 - Typical Source-Drain Diode Forward Voltage

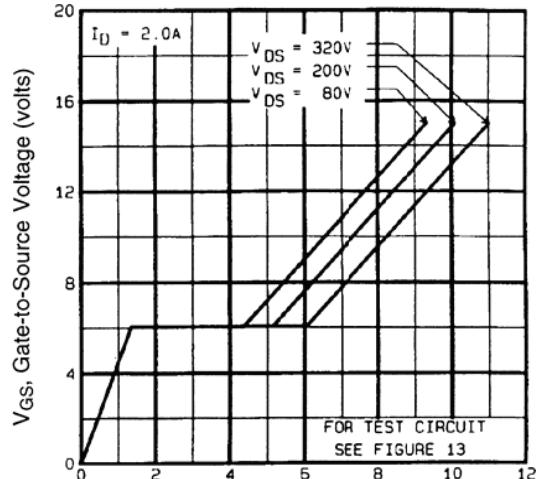


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

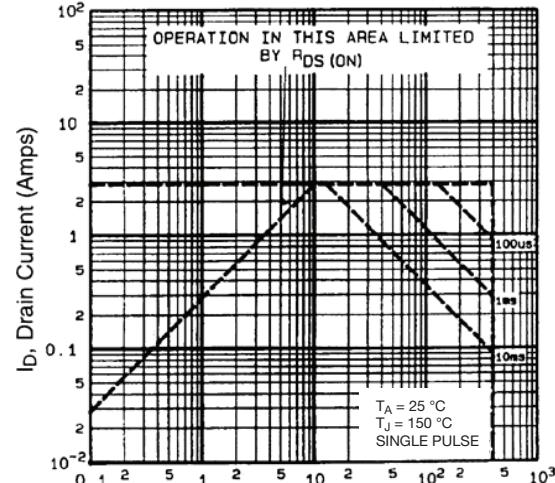


Fig. 8 - Maximum Safe Operating Area

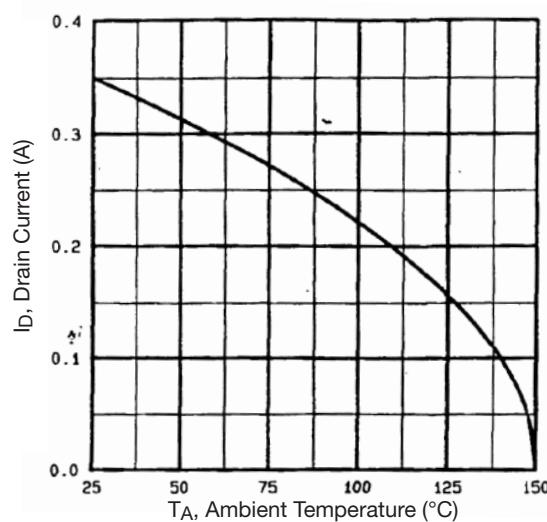


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

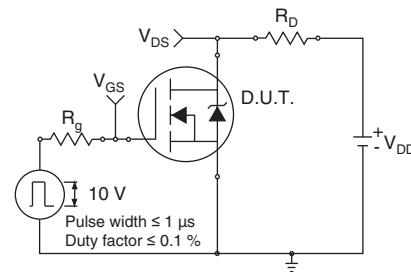


Fig. 10a - Switching Time Test Circuit

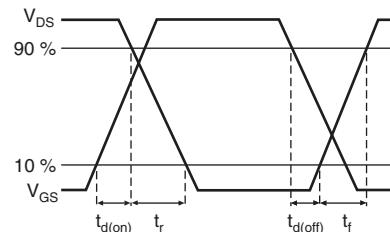


Fig. 10b - Switching Time Waveforms

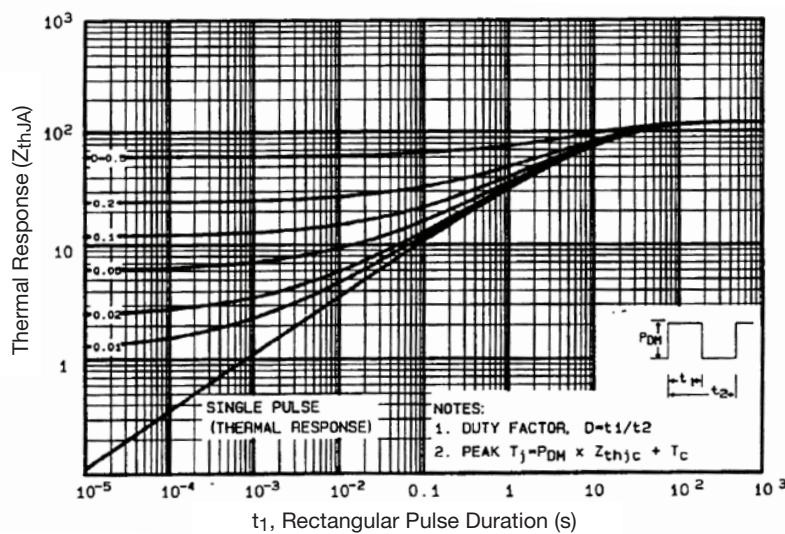


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

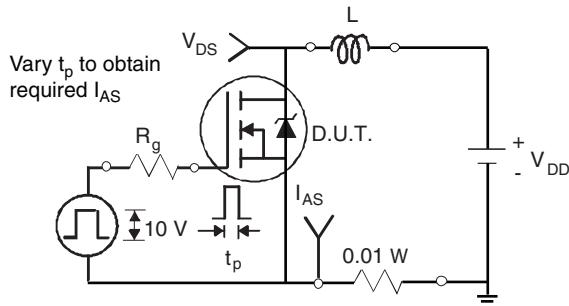


Fig. 12a - Unclamped Inductive Test Circuit

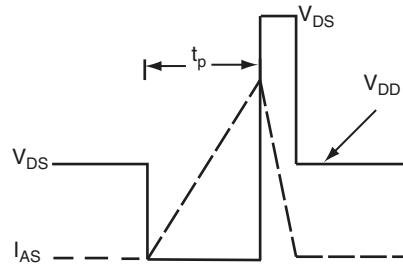


Fig. 12b - Unclamped Inductive Waveforms

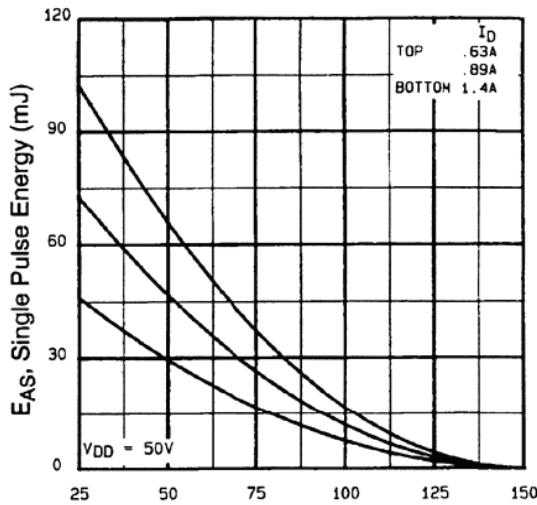


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

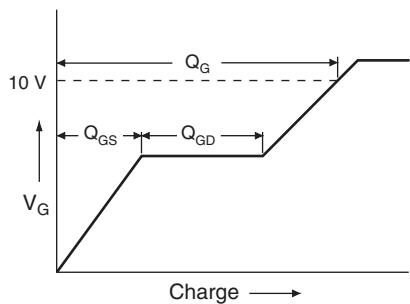


Fig. 13a - Basic Gate Charge Waveform

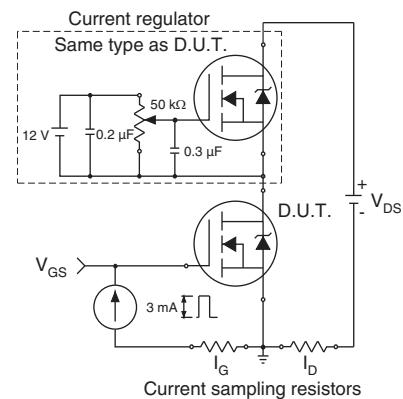
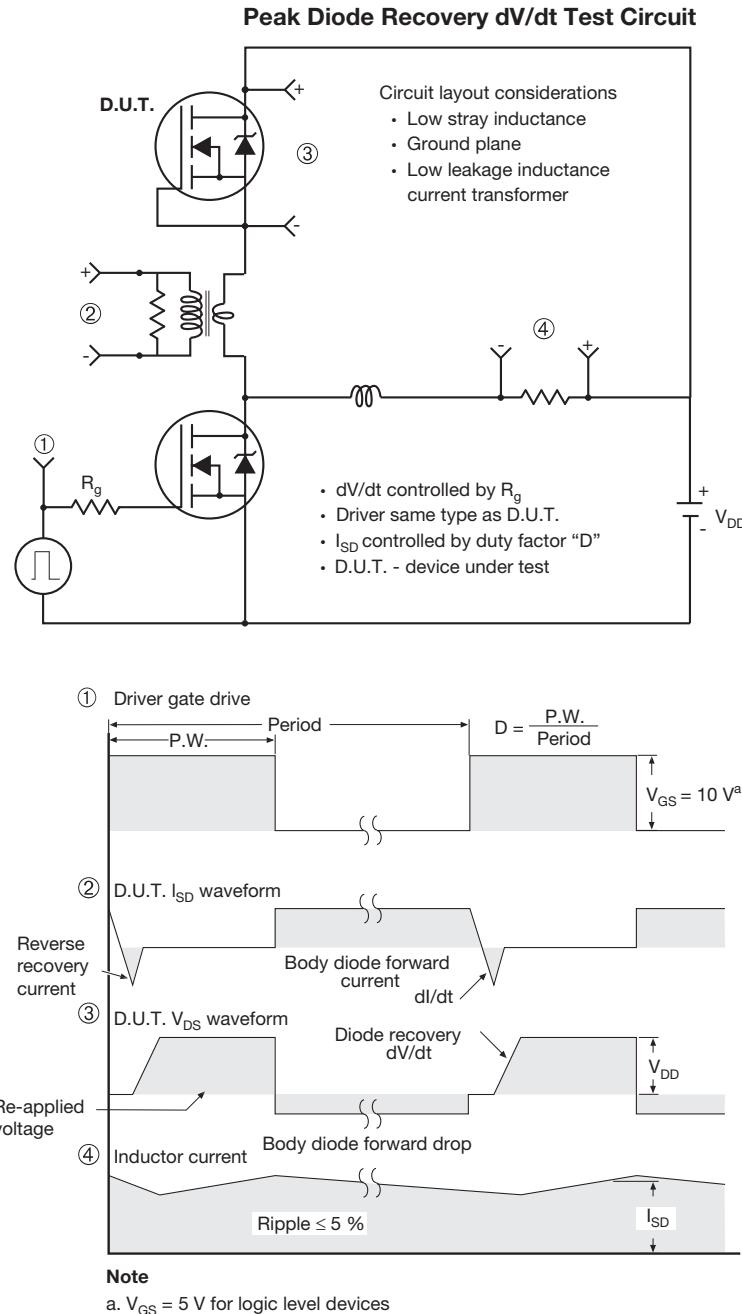
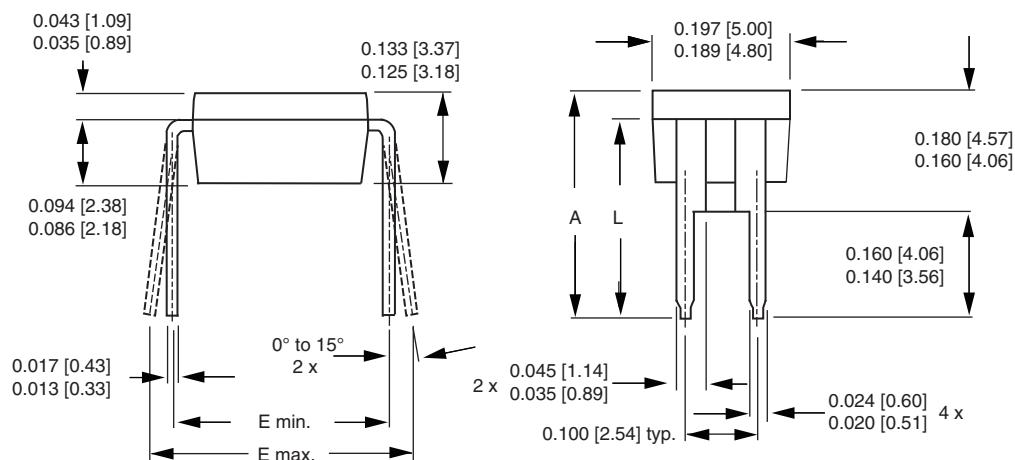
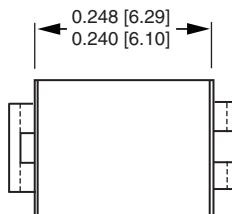


Fig. 13b - Gate Charge Test Circuit


**Fig. 14 - For N-Channel**

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## **HVM DIP** (High voltage)



	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

### Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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