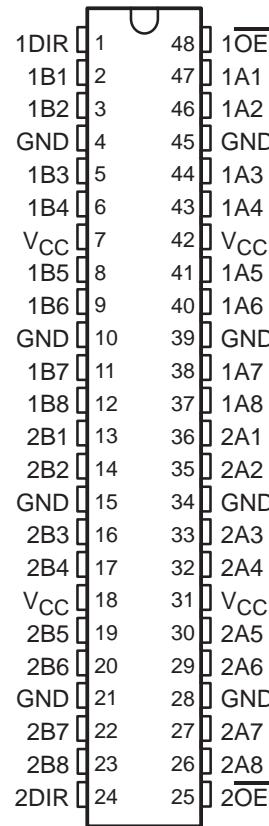


- **Members of the Texas Instruments Widebus™ Family**
- **A-Port Outputs Have Equivalent  $25\Omega$  Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art EPIC-IIIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTH162245 . . . WD PACKAGE  
SN74ABTH162245 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABTH162245 devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent  $25\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162245 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABTH162245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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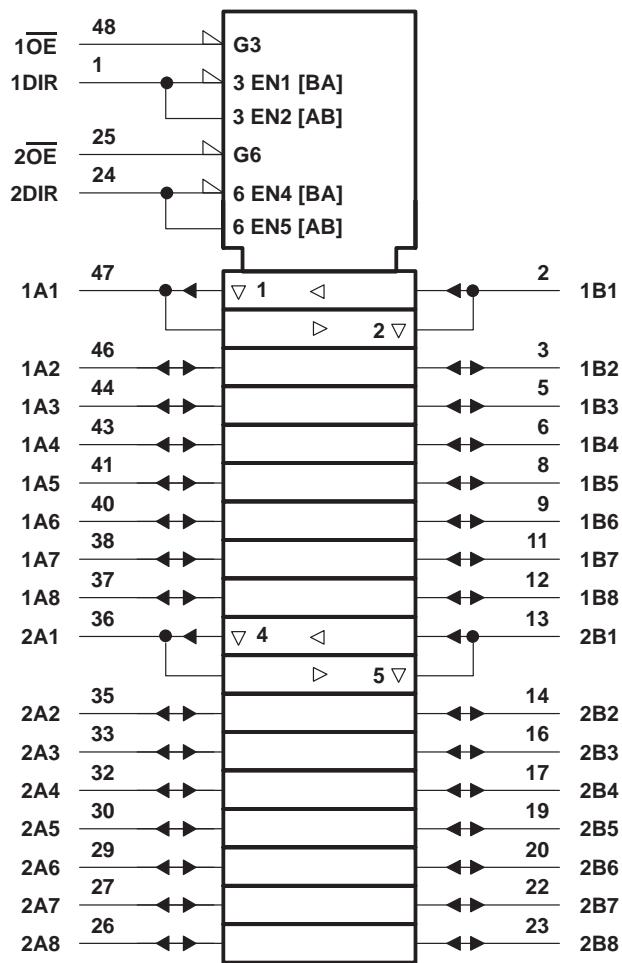
**SN54ABTH162245, SN74ABTH162245  
16-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**FUNCTION TABLE  
(each 8-bit section)**

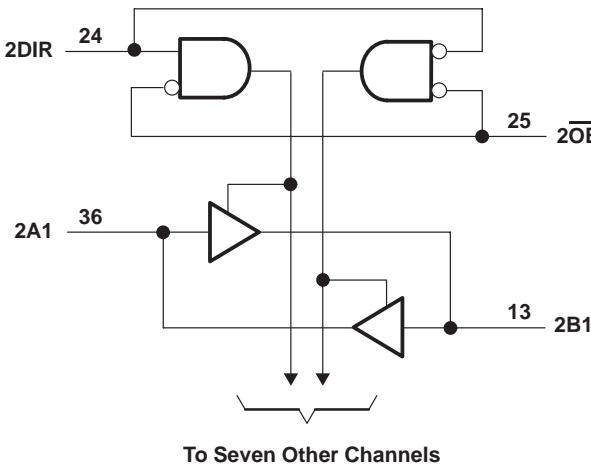
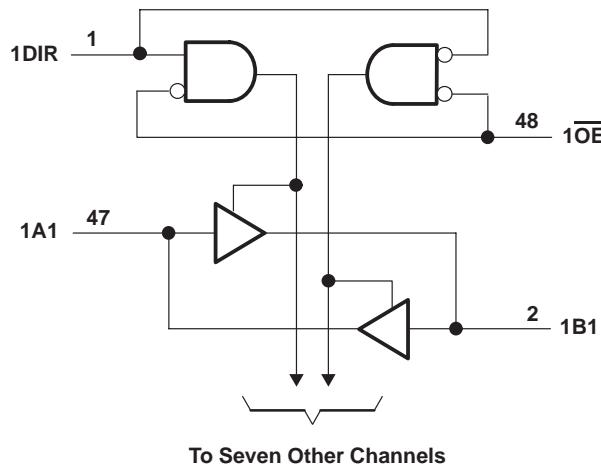
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ :	
SN54ABTH162245 (B port) .....	96 mA
SN74ABTH162245 (B port) .....	128 mA
SN54/74ABTH162245 (A port) .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package .....	89°C/W
DGV package .....	93°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

**SN54ABTH162245, SN74ABTH162245  
16-BIT BUS TRANSCEIVERS  
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**recommended operating conditions (see Note 3)**

		SN54ABTH162245		SN74ABTH162245		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	B port		-24	-32	mA	
		A port		-12	-12		
I <sub>OL</sub>	Low-level output current	B port		48	64	mA	
		A port		12	12		
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH162245			SN74ABTH162245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	A port	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -1 mA	2.5		2.5				V
			3		3				
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	3		3.1				
		I <sub>OH</sub> = -12 mA			2.6				
	B port	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3		3				
			2.5		2.5				
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2						
		I <sub>OH</sub> = -32 mA			2				
V <sub>OL</sub>	A port		I <sub>OL</sub> = 12 mA		0.8		0.8		V
	B port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.45		0.45		
			I <sub>OL</sub> = 64 mA				0.55		
V <sub>hys</sub>				100		100			mV
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		µA
	A or B ports				±20		±20		
I <sub>I</sub> (hold)		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0.8 V	100		100			µA
			V <sub>I</sub> = 2 V	-100		-100			
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V					±100		µA
I <sub>O</sub> ‡	A port	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-25	-90	-25	-100		mA
	B port			-50	-180	-50	-180		
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high		50		50		µA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		2		2		mA
			Outputs low		32		32		
			Outputs disabled		2		2		
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2		2		mA
	Control inputs		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		1.5		1.5		
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V		3		3			pF
C <sub>io</sub>		V <sub>O</sub> = 2.5 V or 0.5 V		6		6			pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**SN54ABTH162245, SN74ABTH162245  
16-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

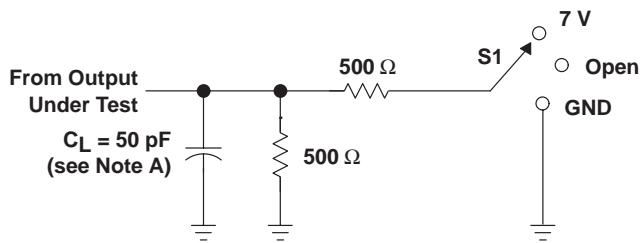
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABTH162245		SN74ABTH162245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	1	2.2	3.4	1	4.1	1	3.9	ns
t <sub>PHL</sub>			1	2.3	3.7	1	4.4	1	4.2	
t <sub>PLH</sub>	B	A	1	2.7	4.1	1	4.9	1	4.6	ns
t <sub>PHL</sub>			1.5	3.1	4.6	1.5	5.2	1.5	5.1	
t <sub>PZH</sub>	OE	B	1	3.6	5.2	1	6.4	1	6.3	ns
t <sub>PZL</sub>			1	3.7	5.4	1	6.5	1	6.4	
t <sub>PHZ</sub>	OE	B	2	4.4	5.8	2	6.4	2	6.3	ns
t <sub>PLZ</sub>			1.5	3.3	4.7	1.5	5.6	1.5	5.2	
t <sub>PZH</sub>	OE	A	1.5	4.1	6	1.5	7.2	1.5	7.1	ns
t <sub>PZL</sub>			1.5	4.3	6.1	1.5	7.3	1.5	7	
t <sub>PHZ</sub>	OE	A	2	4.5	6.1	2	6.8	2	6.6	ns
t <sub>PLZ</sub>			1.5	3.7	5.1	1.5	6.1	1.5	5.7	

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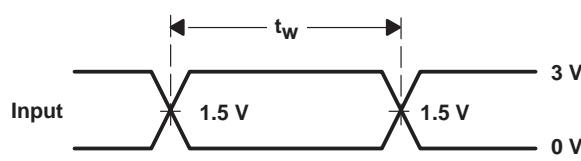
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PARAMETER MEASUREMENT INFORMATION

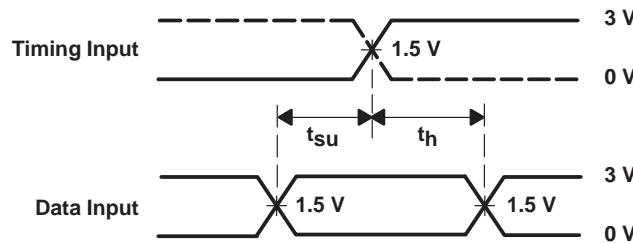


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

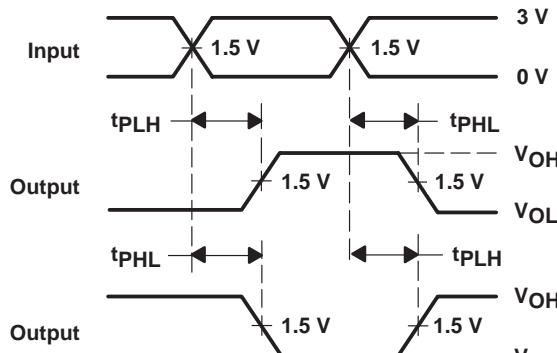
LOAD CIRCUIT



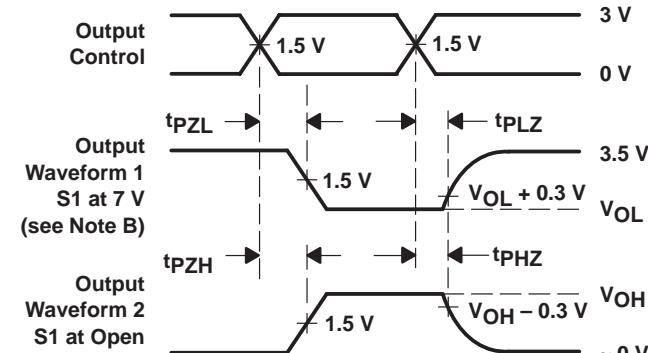
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ABTH162245DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTH162245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTH162245DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTH162245DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABTH162245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH162245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH162245DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABTH162245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

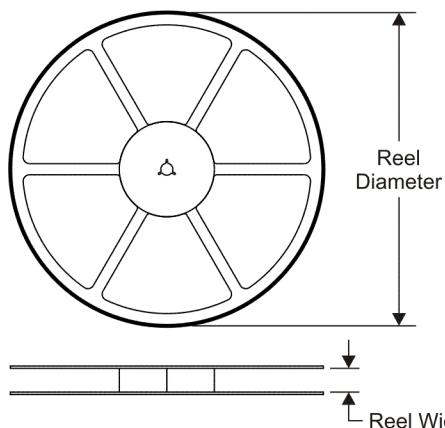
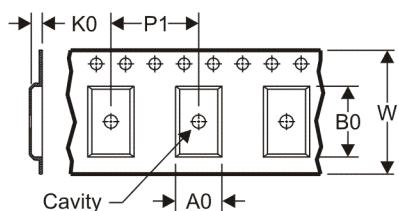
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

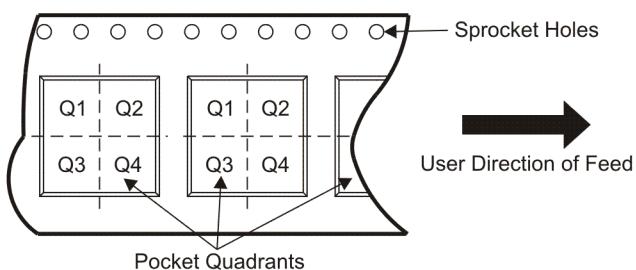
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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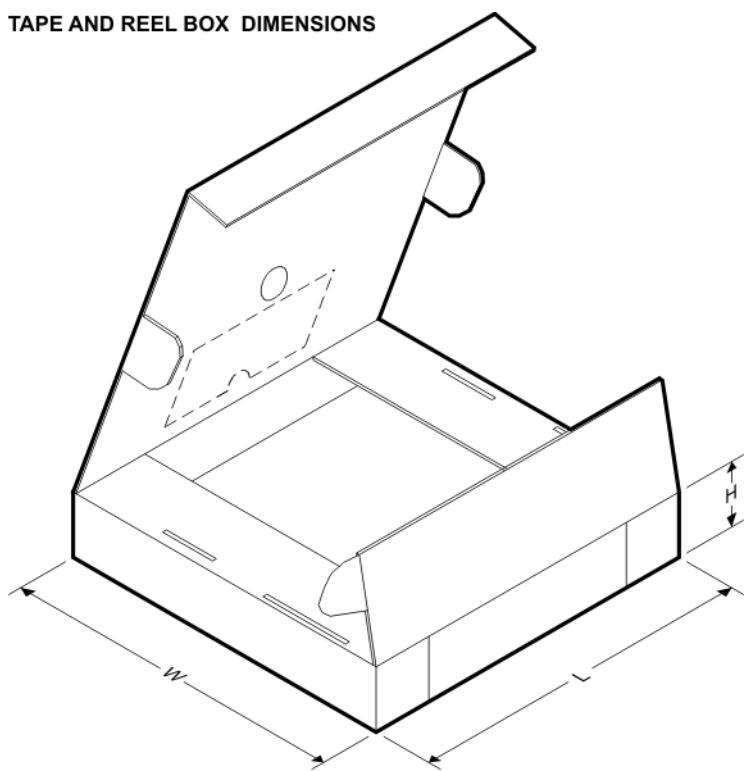
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH162245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABTH162245DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH162245DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ABTH162245DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0

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