Si5330

1.8/2.5/3.3 V Low Jitter, Low Skew Clock Buffer/Level Translator

Features

- Factory-programmed mux selects between 1 of 2 inputs and provides multiple precision, low-skew outputs
  - LVPECL, LVDS, HCSL: 4 outputs
  - CMOS, SSTL, HSTL: 8 outputs
- Versions available that support level translation in addition to clock buffering
  - Differential to single-ended
  - Single-ended to differential
- Ultra-low additive jitter: 0.055 ps rms typ
- Separate core and output supplies to minimize power consumption
- Wide frequency range
  - LVPECL, LVDS: 5 to 710 MHz
  - HCSL: 5 to 250 MHz
  - SSTL, HSTL: 5 to 350 MHz
  - CMOS: 5 to 200 MHz
- Output-output skew: ±100 ps
- Propagation delay: 2.5 ns
- Low power, DC coupled LVPECL mode available
- Small size: 24-lead, 4 x 4 mm QFN
- Low power: 10 mA core supply
- 3.3/2.5/1.8 V supply

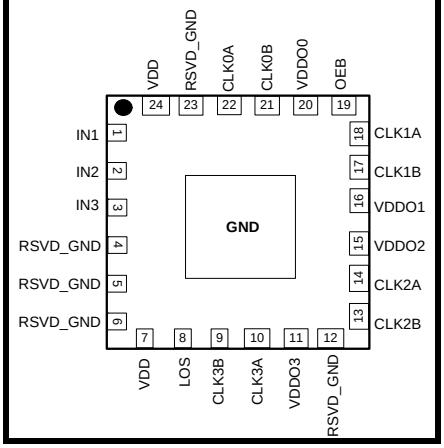
Ordering Information:

See page 13.

Pin Assignments

Si5330

Transparent Top View



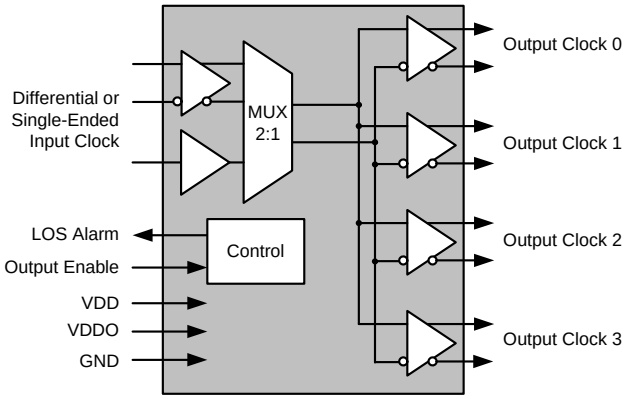
Applications

- Gigabit Ethernet
- OC-3/12, SFI-5
- Processor, memory clocking
- PCI Express 2.0
- Broadcast Video
- xDSL
- PON
- T1/E1

Description

The Si5330 is a low-jitter, low-skew fanout buffer optimized for clock distribution applications. The device produces four differential or eight single-ended low-jitter output clocks at the same frequency as the input clock. All specifications are guaranteed over temperature and voltage. To minimize power consumption, the device core and output clocks have independent supplies. The output clocks can be powered by a 1.5, 1.8, 2.5, or 3.3 V supply, depending on the selected signal format. Operating from a 1.8, 2.5, or 3.3 V core supply, the Si5330 is guaranteed over the industrial temperature range of –40 to +85 °C.

Functional Block Diagram



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Notes
Ambient Temperature	T_A		–40	25	85	°C	
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.							

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	2.5	3.63	V
Core Supply Current	I_{DD}	100 MHz on all outputs, 25 MHz on the input	—	TBD	10	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	TBD	30	mA
		Low Power LVPECL, 710 MHz	—	TBD	15	mA
		LVDS, 710 MHz	—	TBD	8	mA
		HCSL, 250 MHz 2 pF load capacitance	—	TBD	20	mA
		SSTL, 350 MHz	—	TBD	28	mA
		CMOS, 50 MHz 15 pF load capacitance	—	TBD	28	mA
		CMOS, 200 MHz 2 pF load capacitance	—	TBD	28	mA
		HSTL, 350 MHz	—	TBD	22	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	TBD	30	mA
VDD POR Threshold Voltage	V_{PORTHR}		1.55	—	—	V
Propagation Delay	t_{PROP}		—	2.5	—	ns
Output Clock Duty Cycle	t_{ODC}	CLKn < 350 MHz	40	—	60	%
		350 MHz < CLKn < 710 MHz	—	—	100	ps
Output-Output Skew	t_{DSKEW}	Outputs at same frequency, signal format	—	—	100	ps

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKIN Loss of Signal Detect Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Release Time	t_{LOSRLS}		0.01	0.2	1	µs
POR to Output Clock Valid	t_{RDY}	V_{PORTHR} = 1.55 V	—	—	2	ms

Table 3. Input and Output Clock Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pins 1, 2)						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage	V_{PP}		0.5	—	2.4	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (Single-Ended Input Clock on Pin 3)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
		SSTL/HSTL	5	—	350	MHz
Input Voltage	V_I		–0.1	—	3.63	V
Input Voltage Swing (HSTL Standard)		Input = 350 MHz, Tr/Tf = .6 ns	0.6	—	—	V_{PP}
Input Voltage Swing (CMOS Standard)		200 MHz, Tr/Tf = 1.3 ns	0.8	—	3.73	V
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks (Differential)						
Frequency	f_{OUT}	LVPECL, LVDS	5	—	710	MHz
		HCSL	5	—	250	MHz
LVPECL Output Option	V_{OC}	common mode	—	V_{DDO} – 1.4 V	—	V
	V_{OD}	diff swing	1.1	1.6	1.92	V_{PP}
LVDS Output Option (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{OD}	diff swing	0.50	0.70	0.90	V_{PP}
LVDS Output Option (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{OD}	diff swing	0.5	0.7	0.9	V_{PP}
HCSL Output Option	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{OD}	diff swing	1.15	1.45	1.7	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps

Table 3. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Duty Cycle	DC	50% CLKIN duty cycle CLKn < 350 MHz	45	—	55	%
		350 MHz < CLKn < 710 MHz	40	—	60	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	5	—	200	MHz
		SSTL, HSTL	5	—	350	MHz
CMOS 20%-80% Rise/Fall Time 2 pF load	t_R/t_F		—	0.35	TBD	ns
Duty Cycle	DC	40–60% CLKIN duty cycle	45	—	55	%
CMOS Output Voltage	V_{OH}	4 mA load	V_{DDO}–0.3	—	—	V
	V_{OL}	4 mA load	—	—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3, VDDOx = 2.97 to 3.63 V	$0.45xV_{DDO}+0.41$	—	—	V
	V_{OL}		—	—	$0.45xV_{DDO}-0.41$	V
	V_{OH}	SSTL-2, VDDOx = 2.25 to 2.75 V	$0.5xV_{DDO}+0.41$	—	—	V
	V_{OL}		—	—	$0.5xV_{DDO}-0.41$	V
	V_{OH}	SSTL-18, VDDOx = 1.71 to 1.98 V	$0.5xV_{DDO}+0.34$	—	—	V
	V_{OL}		—	—	$0.5xV_{DDO}-0.34$	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	$0.5xV_{DDO}+0.30$	—	—	V
	V_{OL}		—	—	$0.5xV_{DDO}-0.30$	V
OEB						
Input Voltage Low	V_{IL}		–0.1	—	0.3	V
Input Voltage High	V_{IH}		0.9	—	3.63	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		20	—	—	kΩ
Enable/Disable Rate	f_{INI}		—	—	100	kHz
LOS						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time	t_R/t_F	C_L < 10 pf, pull up ≤ 1 kΩ	—	—	10	ns

Table 4. Jitter Specifications

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additive Phase Jitter (12 kHz–20 MHz)	t_{RPHASE}	0.8 V pk-pk input clock with rise/fall time = 150 ps CLKn = 175 MHz, LVDS/LVPECL format	—	0.055	0.15	ps RMS
Additive Phase Jitter (12 kHz–20 MHz)	$t_{RPHASESN}$	0.8 V pk-pk input clock with rise/fall time = 150 ps CLKn = 175 MHz, LVDS/LVPECL format, 100 mV sinusoidal supply noise @ 1 MHz.	—	0.065	—	ps RMS
Additive Phase Jitter (12 kHz–350 MHz)	$t_{RPHASEWB}$	0.8 V pk-pk input clock with rise/fall time = 150 ps CLKn = 710 MHz, LVDS/LVPECL format.	—	0.3	0.4	ps RMS

Table 5. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	Theta JA	Still Air	37	°C/W

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

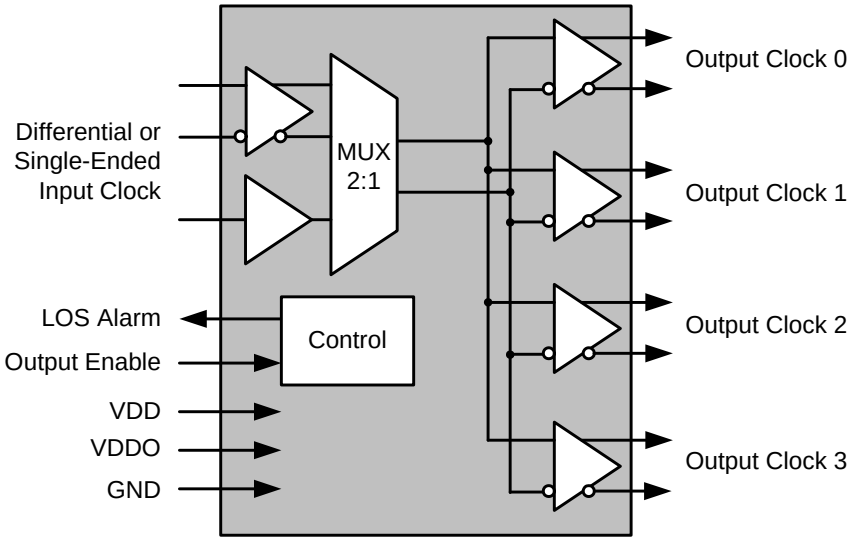


Figure 1. Si5330 Block Diagram

The Si5330 is a low jitter, low skew fanout buffer optimized for clock distribution applications. The device includes an internal mux that is factory-programmed to support either a single-ended or differential input clock source. From a single input, the device distributes four differential clocks from 5 to 710 MHz (LVPECL, LVDS, HCSL), eight single-ended clocks from 5 to 350 MHz (SSTL, HSTL), or eight single-ended clocks from 5 to 200 MHz (CMOS).

All output clocks are at the same frequency and supply voltage. LVDS, HCSL, CMOS, and SSTL buffers are available in 1.8, 2.5, and 3.3 V options. LVPECL buffers are available in 2.5 V and 3.3 V options. HSTL buffers are available in 1.5 V. Output to output skew is guaranteed between all output clocks as specified in Table 3.

The device also supports an option to provide format translation in addition to clock distribution. In this mode, the device can accept one differential input clock and generate eight CMOS clocks at the same frequency. Alternatively, the device can accept one single-ended input clock and generate four differential output clocks at the same frequency. In this mode of operation, the device can accept any single-ended or differential clock that meets the input voltage requirements as specified in Table 3.

The device includes an output enable pin that disables all output clocks. The Si5330 also includes a loss of signal indicator that monitors the quality of the input clock. The device core operates from a 1.8, 2.5, or 3.3 V supply. The device outputs operate from a dedicated supply. All outputs operate at the same voltage, as specified by the selected signal format of the ordered device. Device operation is guaranteed over the industrial temperature range of –40 to +85 °C.

2.1. Si5330 Device Evaluation

Silicon Labs offers evaluation hardware and software that enables the rapid evaluation of any Si5330 clock buffer. The device evaluation board is the Si5338-EVB and is available to order from all Silicon Labs distributors and representatives. The evaluation board ships with device configuration software. The user can select any member of the Si5330 product family from a product selector guide and the software configures the Si5330 DUT to operate as that specific device, enabling easy evaluation.

2.2. Device Reset

To completely reset the device, a power cycle must be performed.

2.3. Loss of Signal Indicator

The Si5330 monitors the input clock for loss of signal (LOS). The LOS algorithm monitors input clock edges and declares an LOS alarm when signal edges are not detected over a 5 µsec observation period. When a loss of signal event is detected, the device output clocks are squelched. When the input clock returns and is revalidated, the output clocks will reappear and normal operation will resume.

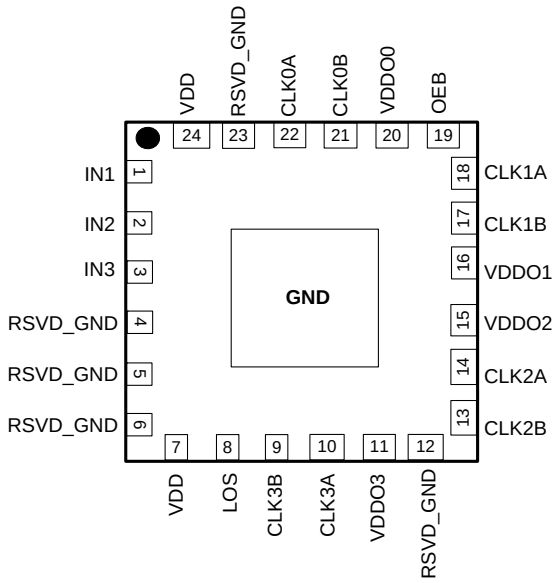
2.4. Self-Calibration

The device performs an internal self-calibration before operation to optimize performance. The output clocks appear after the device finishes self calibration.

The following events will trigger a self-calibration:

- Power on reset
- Input clock loss of signal

3. Pin Descriptions—Si5330



Note: Center pad must be tied to GND for normal operation.

Table 7. Si5330 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1	IN1	I	Multi	**Differential Input Clock** When Pin 3 is not used as a clock input, this pin functions as a differential input clock (positive terminal) for LVPECL, LVDS, and HCSL clock buffers. If unused, this pin must be tied to GND.
2	IN2	I	Multi	**Differential Input Clock** When Pin 3 is not used as a clock input, this pin functions as a differential input clock (negative terminal) for LVPECL, LVDS, and HCSL clock buffers. If unused, this pin must be tied to GND.
3	IN3	I	Multi	**Clock Input** When pins 1 and 2 are not used as clock inputs, this pin functions as an input receiver for CMOS/SSTL/HSTL clock signals. This input must be dc-coupled.
4	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
5	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
6	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
7	VDD	VDD	Supply	**Core Supply Voltage** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.

Table 7. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
8	LOS	O	Open Drain	**Loss of Signal Indicator.** 0 = CLKIN present. 1 = Loss of signal (LOS). This pin requires an external ≤1 kΩ pull-up resistor.
9	CLK3B	O	Multi	**Output Clock B for Channel 3** May be a single-ended output or half of a differential output with CLK3A being the other differential half.
10	CLK3A	O	Multi	**Output Clock A for Channel 3** May be a single-ended output or half of a differential output with CLK3B being the other differential half.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK3A,B. If CLK3 is not used, this pin must be tied to pin 7 and/or pin 24.
12	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
13	CLK2B	O	Multi	**Output Clock B for Channel 2** May be a single-ended output or half of a differential output with CLK2A being the other differential half.
14	CLK2A	O	Multi	**Output Clock A for Channel 2** May be a single-ended output or half of a differential output with CLK2B being the other differential half.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK2A,B. If CLK2 is not used, this pin must be tied to pin 7 and/or pin 24.
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK1A,B. If CLK1 is not used, this pin must be tied to pin 7 and/or pin 24.
17	CLK1B	O	Multi	**Output Clock B for Channel 1** May be a single-ended output or half of a differential output with CLK1A being the other differential half. If unused, this pin must be tied to VDD pin 24.
18	CLK1A	O	Multi	**Output Clock A for Channel 1** May be a single-ended output or half of a differential output with CLK1B being the other differential half.
19	OEB	I	CMOS	**Output Enable Low.** When low, all outputs are enabled. This input is 3.3 V tolerant.
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage** Supply voltage for CLK0A,B. If CLK2 is not used, this pin must be tied to pin 7 and/or pin 24.
21	CLK0B	O	Multi	**Output Clock B for Channel 0** May be a single-ended output or half of a differential output with CLK0A being the other differential half.

Table 7. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
22	CLK0A	O	Multi	**Output Clock A for Channel 0** May be a single-ended output or half of a differential output with CLK0B being the other differential half.
23	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	Supply	**Ground Pad.** This is the large pad in the center of the package. Nine or more vias should be used to connect this pad to a ground plane. Device specifications cannot be guaranteed unless the ground pad is properly connected to a ground plane on the PCB.

4. Orderable Part Numbers and Device Functionality

Part Number	Input	Output Format	Outputs	Frequency
LVPECL Buffers				
Si5330A-A00200-GM	Differential	3.3 V LVPECL	4	5 to 710 MHz
Si5330A-A00201-GM	Differential	3.3 V Low Power LVPECL	4	5 to 710 MHz
Si5330A-A00202-GM	Differential	2.5 V LVPECL	4	5 to 710 MHz
Si5330A-A00203-GM	Differential	2.5 V Low Power LVPECL	4	5 to 710 MHz
LVDS Buffers				
Si5330B-A00204-GM	Differential	3.3 V LVDS	4	5 to 710 MHz
Si5330B-A00205-GM	Differential	2.5 V LVDS	4	5 to 710 MHz
Si5330B-A00206-GM	Differential	1.8 V LVDS	4	5 to 710 MHz
HCSL Buffers				
Si5330C-A00207-GM	Differential	3.3 V HCSL	4	5 to 250 MHz
Si5330C-A00208-GM	Differential	2.5 V HCSL	4	5 to 250 MHz
Si5330C-A00209-GM	Differential	1.8 V HCSL	4	5 to 250 MHz
SSTL Buffers				
Si5330D-A00210-GM	Single-Ended	3.3 V SSTL	8	5 to 350 MHz
Si5330D-A00211-GM	Single-Ended	2.5 V SSTL	8	5 to 350 MHz
Si5330D-A00212-GM	Single-Ended	1.8 V SSTL	8	5 to 350 MHz
HSTL Buffers				
Si5330E-A00213-GM	Single-Ended	1.5 V HSTL	8	5 to 350 MHz
CMOS Buffers				
Si5330F-A00214-GM	Single-Ended	3.3 V CMOS	8	5 to 200 MHz
Si5330F-A00215-GM	Single-Ended	2.5 V CMOS	8	5 to 200 MHz
Si5330F-A00216-GM	Single-Ended	1.8 V CMOS	8	5 to 200 MHz
CMOS Buffers (Differential Input)				
Si5330G-A00217-GM	Differential	3.3 V CMOS	8	5 to 200 MHz
Si5330G-A00218-GM	Differential	2.5 V CMOS	8	5 to 200 MHz
Si5330G-A00219-GM	Differential	1.8 V CMOS	8	5 to 200 MHz
SSTL Buffers (Differential Input)				
Si5330H-A00220-GM	Differential	3.3 V SSTL	8	5 to 350 MHz
Si5330H-A00221-GM	Differential	2.5 V SSTL	8	5 to 350 MHz
Si5330H-A00222-GM	Differential	1.8 V SSTL	8	5 to 350 MHz

HSTL Buffers (Differential Input)				
Si5330J-A00223-GM	Differential	1.5 V HSTL	8	5 to 350 MHz
LVPECL Buffers (Single-Ended Input)				
Si5330K-A00224-GM	Single-Ended	3.3 V LVPECL	4	5 to 350 MHz
Si5330K-A00225-GM	Single-Ended	3.3 V Low Power LVPECL	4	5 to 350 MHz
Si5330K-A00226-GM	Single-Ended	2.5 V LVPECL	4	5 to 350 MHz
Si5330K-A00227-GM	Single-Ended	2.5 V Low Power LVPECL	4	5 to 350 MHz
LVDS Buffers (Single-Ended Input)				
Si5330L-A00228-GM	Single-Ended	3.3 V LVDS	4	5 to 350 MHz
Si5330L-A00229-GM	Single-Ended	2.5 V LVDS	4	5 to 350 MHz
Si5330L-A00230-GM	Single-Ended	1.8 V LVDS	4	5 to 350 MHz
HCSL Buffers (Single-Ended Input)				
Si5330M-A00231-GM	Single-Ended	3.3 V HCSL	4	5 to 250 MHz
Si5330M-A00232-GM	Single-Ended	2.5 V HCSL	4	5 to 250 MHz
Si5330M-A00233-GM	Single-Ended	1.8 V HCSL	4	5 to 250 MHz

5. Package Outline: 24-Lead QFN

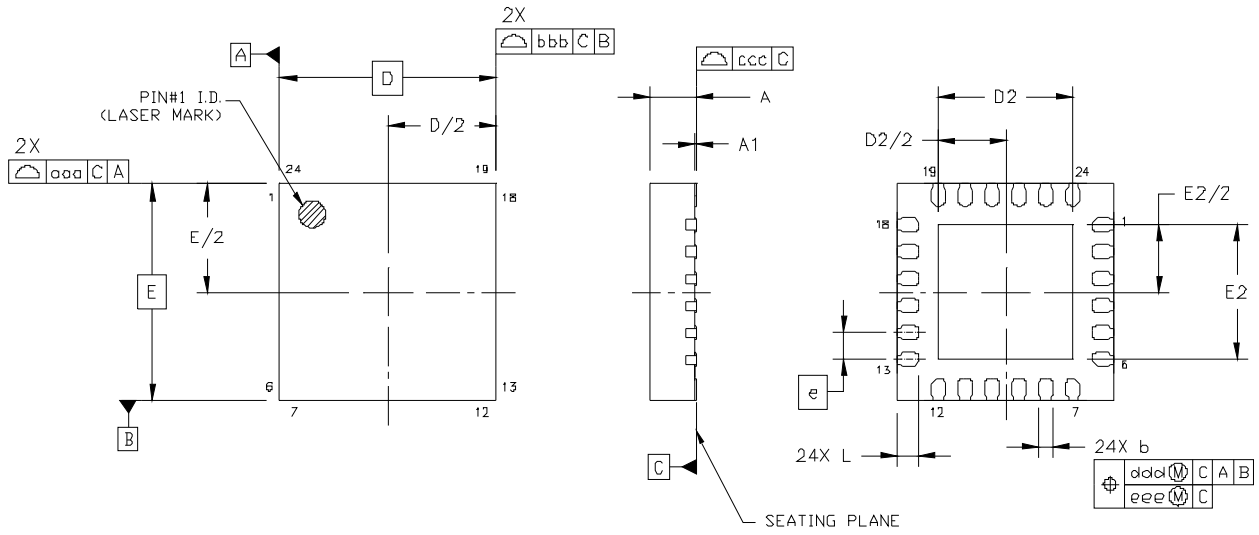


Figure 2. 24-Lead Quad Flat No-lead (QFN)

Table 8. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. Recommended PCB Layout

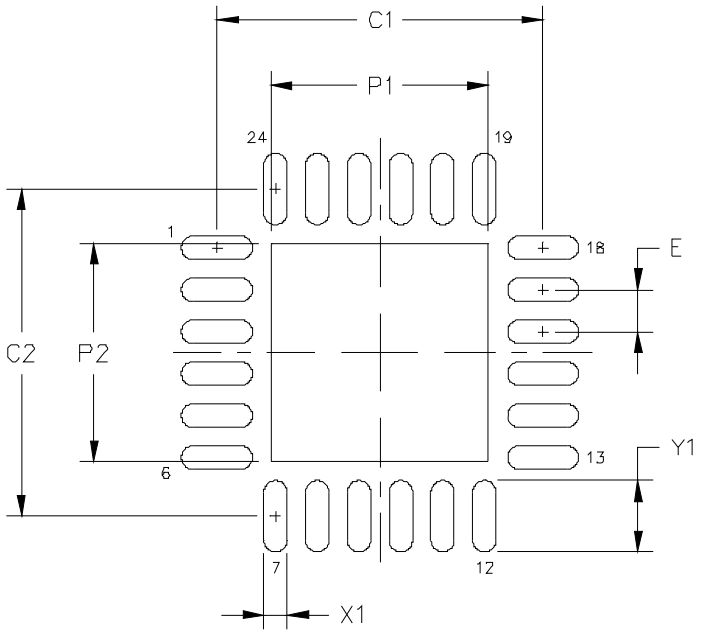


Table 9. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 2x2 array of 1.0 mm square openings on 1.25mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Clarified documentation to reflect that Pin 19 is OEB (OE Enable Low).
- Updated Table 4, “Jitter Specifications,” on page 7.

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