

# 74VCX00

## Low Voltage Quad 2-Input NAND Gate with 3.6V Tolerant Inputs and Outputs

### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ 
  - 2.8ns max. for 3.0V to 3.6V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Static Drive ( $I_{OH}/I_{OL}$ )
  - $\pm 24mA$  @ 3.0V  $V_{CC}$
- Uses proprietary noise/EMI reduction circuitry
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:
  - Human body model > 2000V
  - Machine model > 250V
- Leadless DQFN package

### General Description

The VCX00 contains four 2-input NAND gates. This product is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The VCX00 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

### Ordering Information

Order Number	Package Number	Package Description
74VCX00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX00BQX <sup>(1)</sup>	MLP14A	14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74VCX00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

#### Note:

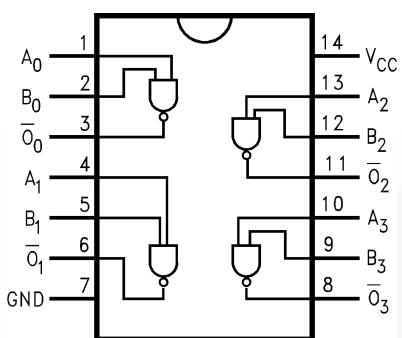
1. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

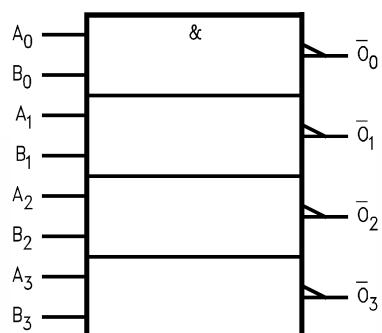
## Connection Diagrams

### Pin Assignments for SOIC and TSSOP

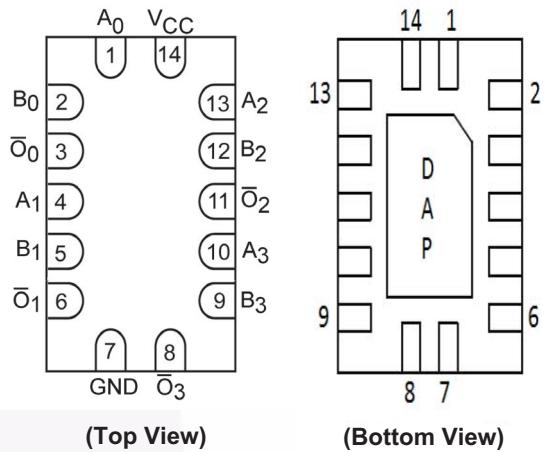


## Logic Symbol

### IEEE/IEC



### Pad Assignments for DQFN



(Top View)

(Bottom View)

## Pin Description

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +4.6V
$V_I$	DC Input Voltage	−0.5V to 4.6V
$V_O$	DC Output Voltage HIGH or LOW State <sup>(2)</sup>	−0.5V to $V_{CC}$ + 0.5V
	$V_{CC} = 0V$	−0.5V to 4.6V
$I_{IK}$	DC Input Diode Current, $V_I < 0V$	−50mA
$I_{OK}$	DC Output Diode Current $V_O < 0V$	−50mA
	$V_O > V_{CC}$	+50mA
$I_{OH} / I_{OL}$	DC Output Source/Sink Current	±50mA
$I_{CC}$ or GND	DC $V_{CC}$ or Gound Current per Supply Pin	±100mA
$T_{STG}$	Storage Temperature Range	−65°C to +150°C

**Note:**

2.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(3)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Power Supply Operating	1.2V to 3.6V
$V_I$	Input Voltage	−0.3V to 3.6V
$V_O$	Output Voltage, HIGH or LOW State	0V to $V_{CC}$
$I_{OH} / I_{OL}$	Output Current $V_{CC} = 3.0V$ to 3.6V	±24mA
	$V_{CC} = 2.3V$ to 2.7V	±18mA
	$V_{CC} = 1.65V$ to 2.3V	±6mA
	$V_{CC} = 1.4V$ to 1.6V	±2mA
	$V_{CC} = 1.2V$	± 100µA
$T_A$	Free Air Operating Temperature	−40°C to +85°C
$\Delta t / \Delta V$	Minimum Input Edge Rate, $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10ns/V

**Note:**

3. Floating or unused inputs must be held HIGH or LOW

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage	2.7–3.6		2.0		V
		2.3–2.7		1.6		
		1.65–2.3		0.65 × V <sub>CC</sub>		
		1.4–1.6		0.65 × V <sub>CC</sub>		
		1.2		0.65 × V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input Voltage	2.7–3.6			0.8	V
		2.3–2.7			0.7	
		1.65–2.3			0.35 × V <sub>CC</sub>	
		1.4–1.6			0.35 × V <sub>CC</sub>	
		1.2			0.05 × V <sub>CC</sub>	
V <sub>OH</sub>	HIGH Level Output Voltage	2.7–3.6	I <sub>OH</sub> = -100µA	V <sub>CC</sub> – 0.2		V
		2.7	I <sub>OH</sub> = -12mA	2.2		
		3.0	I <sub>OH</sub> = -18mA	2.4		
		3.0	I <sub>OH</sub> = -24mA	2.2		
		2.3–2.7	I <sub>OH</sub> = -100µA	V <sub>CC</sub> – 0.2		
		2.3	I <sub>OH</sub> = -6mA	2.0		
		2.3	I <sub>OH</sub> = -12mA	1.8		
		2.3	I <sub>OH</sub> = -18mA	1.7		
		1.65–2.3	I <sub>OH</sub> = -100µA	V <sub>CC</sub> – 0.2		
		1.65	I <sub>OH</sub> = -6mA	1.25		
		1.4–1.6	I <sub>OH</sub> = -100µA	V <sub>CC</sub> – 0.2		
		1.4	I <sub>OH</sub> = -2mA	1.05		
		1.2	I <sub>OH</sub> = -100µA	V <sub>CC</sub> – 0.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7–3.6	I <sub>OL</sub> = 100µA		0.2	V
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 18mA		0.4	
		3.0	I <sub>OL</sub> = 24mA		0.55	
		2.3–2.7	I <sub>OL</sub> = 100µA		0.2	
		2.3	I <sub>OL</sub> = 12mA		0.4	
		2.3	I <sub>OL</sub> = 18mA		0.6	
		1.65–2.3	I <sub>OL</sub> = 100µA		0.2	
		1.65	I <sub>OL</sub> = 6mA		0.3	
		1.4–1.6	I <sub>OL</sub> = 100µA		0.2	
		1.4	I <sub>OL</sub> = 2mA		0.35	
		1.2	I <sub>OL</sub> = 100µA		0.05	
I <sub>I</sub>	Input Leakage Current	1.4–3.6	0 ≤ V <sub>I</sub> ≤ 3.6V		±5.0	µA
I <sub>OZ</sub>	3-STATE Output Leakage	1.4–3.6	0 ≤ V <sub>O</sub> ≤ 3.6V, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±10	µA
I <sub>OFF</sub>	Power-OFF Leakage Current	0	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V		10	µA
I <sub>CC</sub>	Quiescent Supply Current	1.4–3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		20	µA
			V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V <sup>(4)</sup>		±20	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7–3.6	V <sub>IH</sub> = V <sub>CC</sub> – 0.6V		750	µA

## Note:

4. Outputs disabled or 3-STATE only.

AC Electrical Characteristics<sup>(5)</sup>

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min.	Max.		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	3.3 ± 0.3	C <sub>L</sub> = 30pF, R <sub>L</sub> = 500Ω	0.6	2.8	ns	Fig. 1 Fig. 2
		2.5 ± 0.2		0.8	3.7		
		1.8 ± 0.15		1.0	7.4		
		1.5 ± 0.1	C <sub>L</sub> = 15pF, R <sub>L</sub> = 2kΩ	1.0	14.8	ns	Fig. 3
		1.2		1.5	37.0		Fig. 4
t <sub>OShL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(6)</sup>	3.3 ± 0.3	C <sub>L</sub> = 30pF, R <sub>L</sub> = 500Ω		0.5	ns	
		2.5 ± 0.2			0.5		
		1.8 ± 0.15			0.75		
		1.5 ± 0.1	C <sub>L</sub> = 15pF, R <sub>L</sub> = 2kΩ		1.5		
		1.2			1.5		

## Note:

5. For C<sub>L</sub> = 50pF, add approximately 300ps to the AC Maximum specification.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OShL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

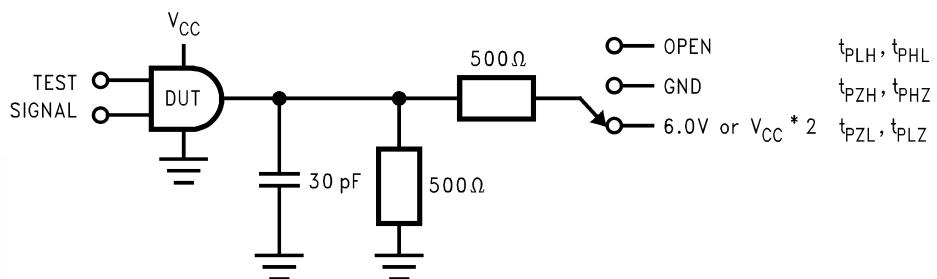
## Dynamic Switching Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C		Unit
				Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	1.8	C <sub>L</sub> = 30pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	0.25		V
		2.5		0.6		
		3.3		0.8		
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	1.8	C <sub>L</sub> = 30pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	-0.25		V
		2.5		-0.6		
		3.3		-0.8		
V <sub>OHV</sub>	Quiet Output Dynamic Valley V <sub>OH</sub>	1.8	C <sub>L</sub> = 30pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.5		V
		2.5		1.9		
		3.3		2.2		

## Capacitance

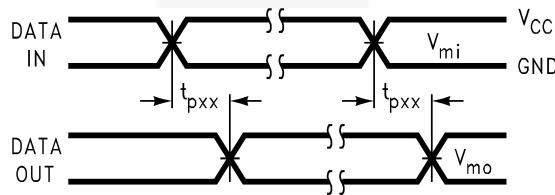
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units
			Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	6		pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20		pF

**AC Loading and Waveforms** ( $V_{CC}$  3.3V  $\pm$  0.3V to 1.8V  $\pm$  0.15V)



Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open

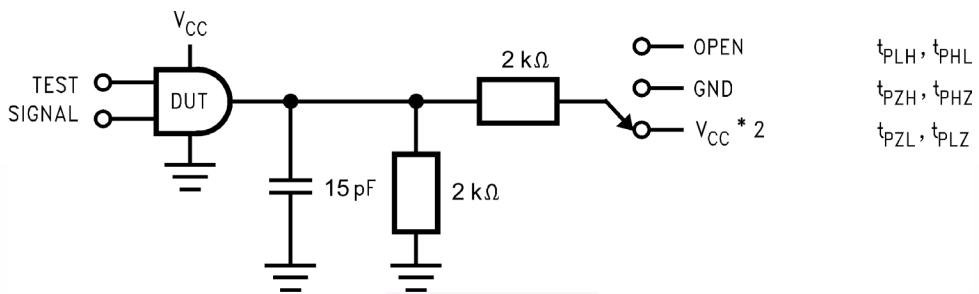
Figure 1. AC Test Circuit



Symbol	$V_{CC}$		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
$V_{mi}$	1.5V	$V_{CC} / 2$	$V_{CC} / 2$
$V_{mo}$	1.5V	$V_{CC} / 2$	$V_{CC} / 2$

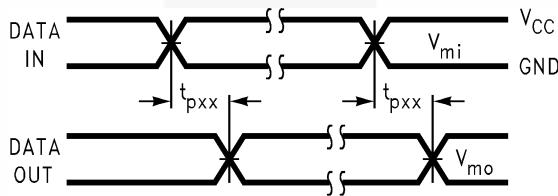
Figure 2. Waveform for Inverting and Non-inverting Functions

**AC Loading and Waveforms ( $V_{CC}$  1.5 ± 0.1V to 1.2V)**



Test	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC} \times 2$ at $V_{CC} = 1.5V \pm 0.1V$
$t_{PZH}, t_{PHZ}$	GND

Figure 3. AC Test Circuit



Symbol	$V_{CC}$
	$1.5V \pm 0.1V$
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$

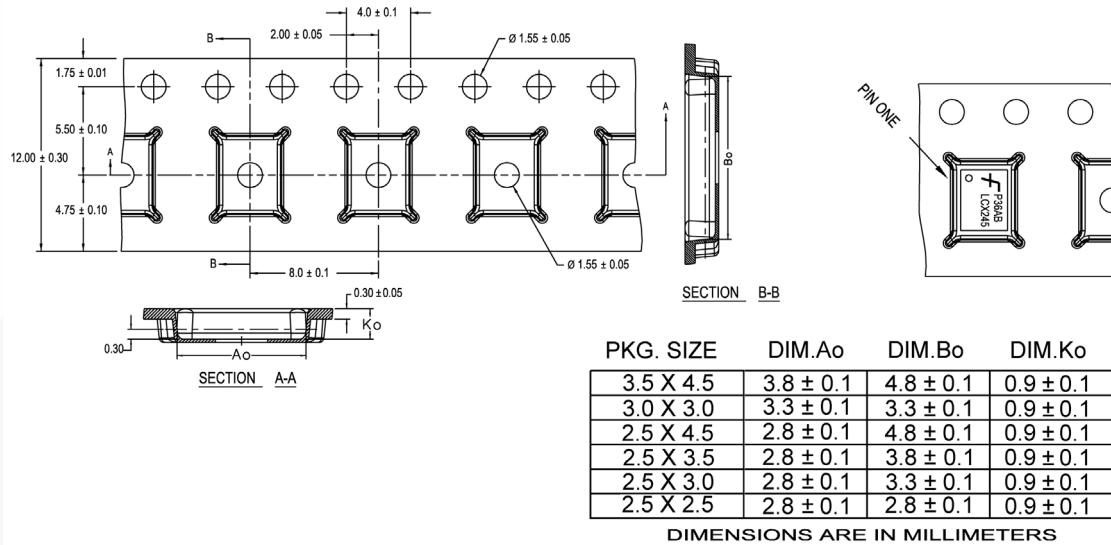
Figure 4. Waveform for Inverting and Non-Inverting Functions

## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (Typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typ.)	Empty	Sealed

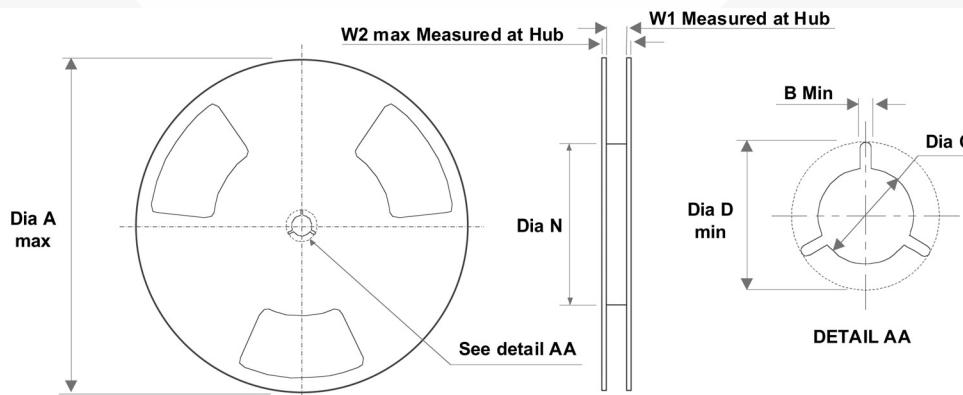
### Tape Dimensions inches (millimeters)



NOTES: unless otherwise specified

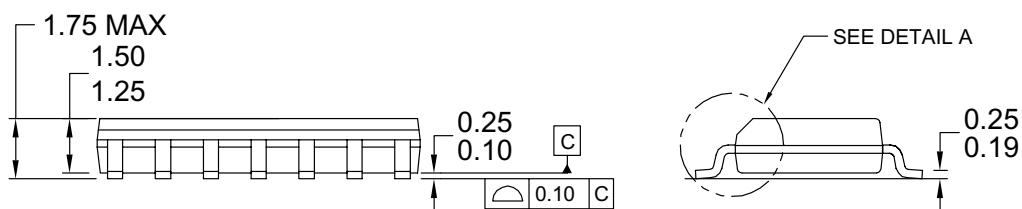
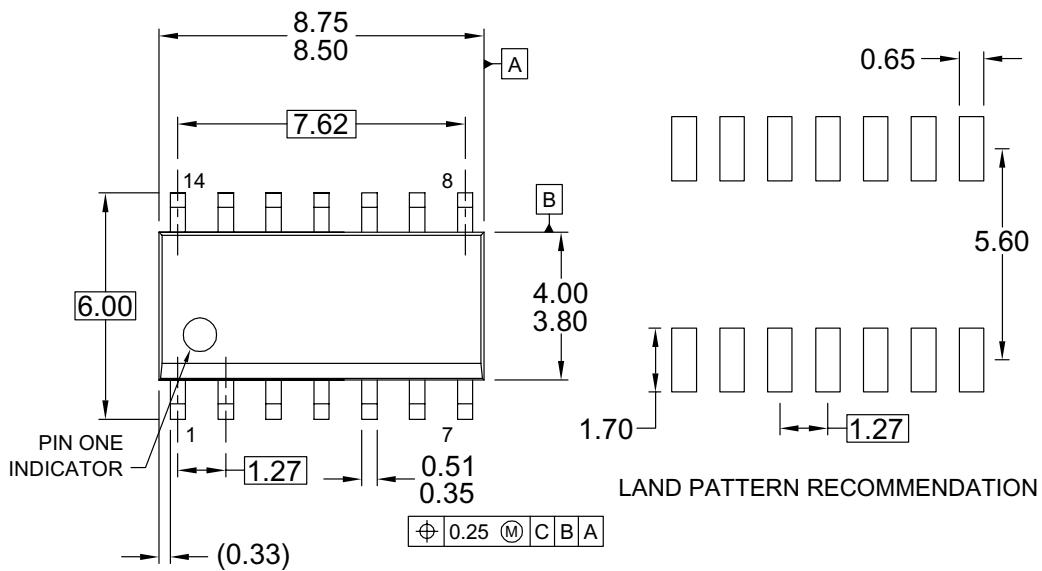
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

## Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD:  
SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

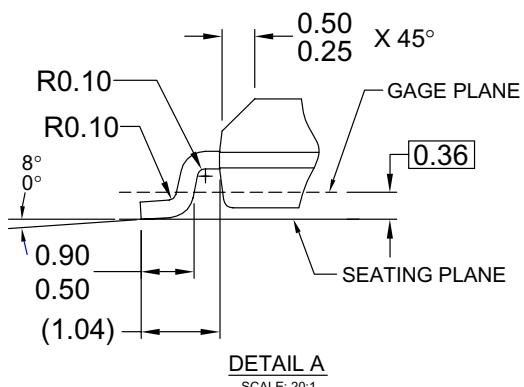


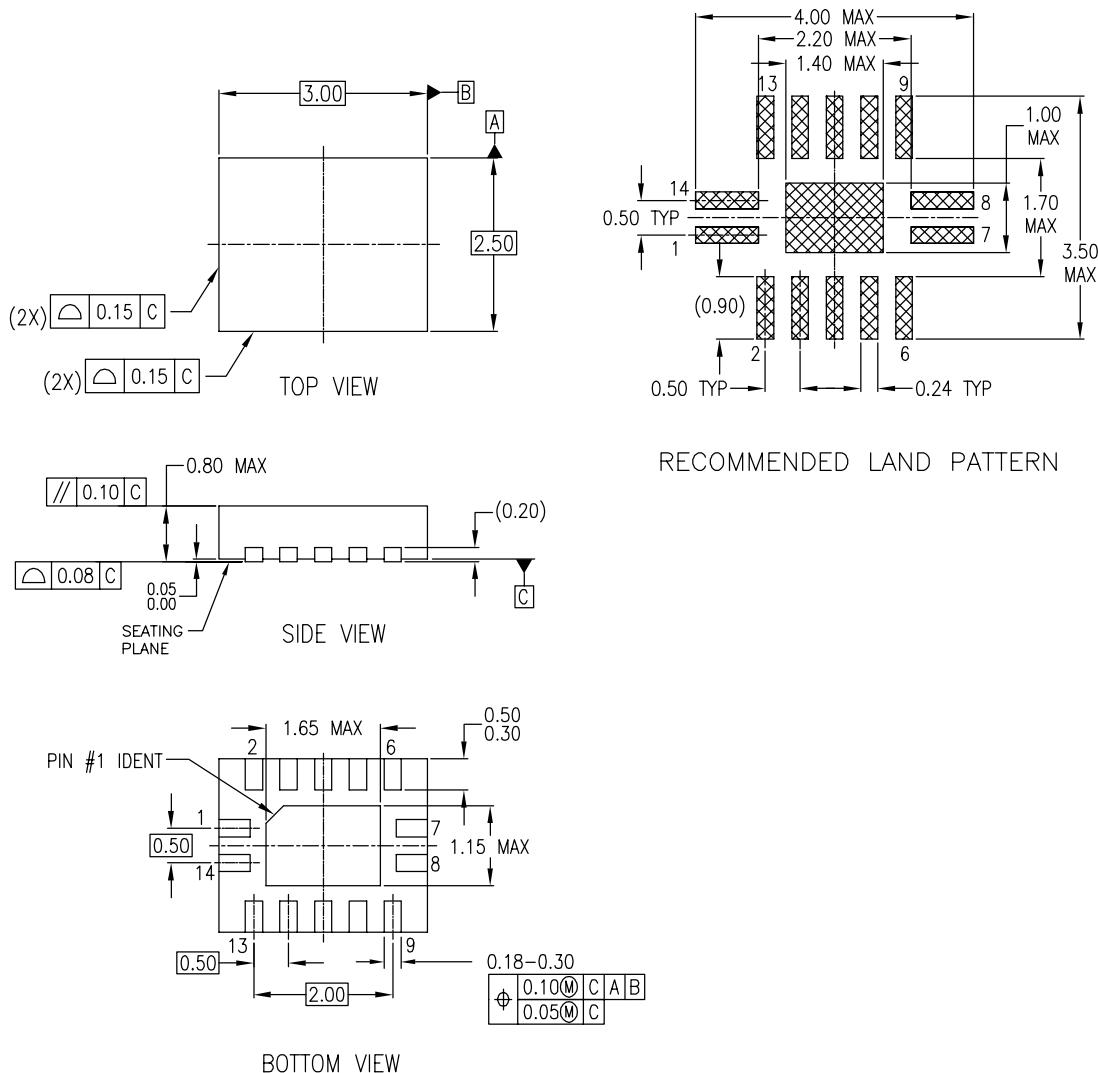
Figure 5. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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**Physical Dimensions (Continued)**



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

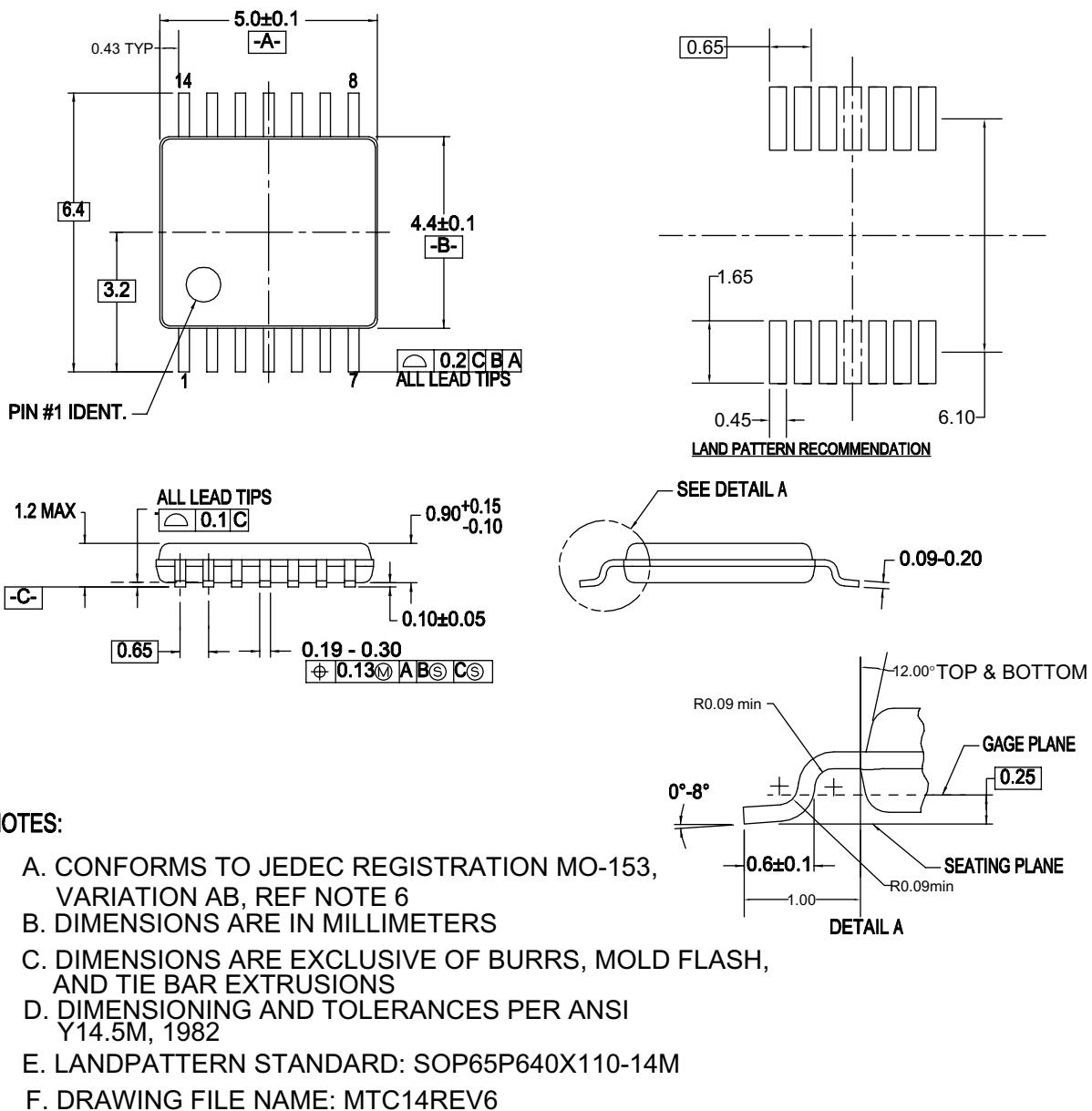
**Figure 6. 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm**

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**Physical Dimensions (Continued)**



**Figure 7. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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