



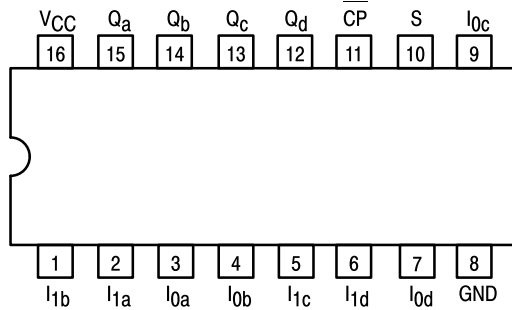
QUAD 2-INPUT MULTIPLEXER WITH STORAGE

The SN54/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

<u>S</u>	Common Select Input
<u>CP</u>	Clock (Active LOW Going Edge) Input
I0a-I0d	Data Inputs From Source 0
I1a-I1d	Data Inputs From Source 1
Qa-Qd	Register Outputs (Note b)

NOTES:

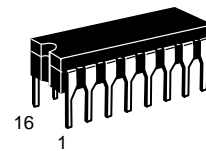
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)	
HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

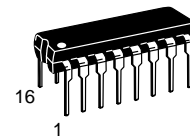
SN54/74LS298

QUAD 2-INPUT MULTIPLEXER WITH STORAGE

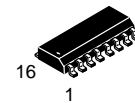
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

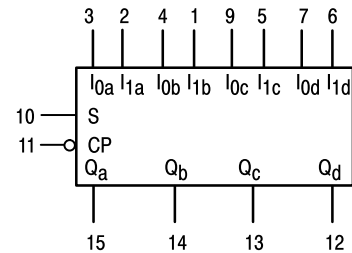


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

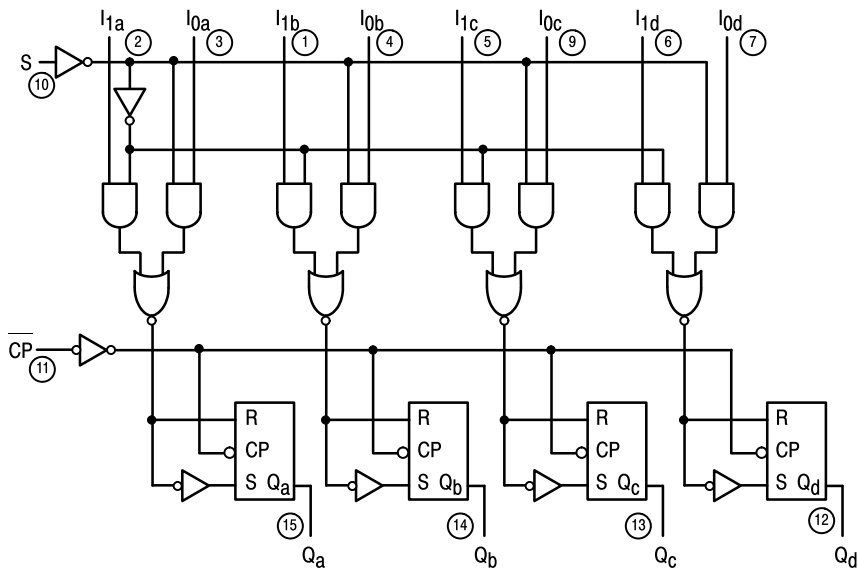
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS298

LOGIC OR BLOCK DIAGRAM



V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW

transition of the Clock input (CP). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I ₀	I ₁	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS298

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current				20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
					0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current				-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)		-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current				21	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t_{PLH}	Propagation Delay, Clock to Output			18	27	ns	$V_{CC} = 5.0 \text{ V}$, $C_L = 15 \text{ pF}$
t_{PHL}				21	32	ns	

AC SET-UP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t_W	Clock Pulse Width		20			ns	$V_{CC} = 5.0 \text{ V}$
t_s	Data Setup Time		15			ns	
t_s	Select Setup Time		25			ns	
t_h	Data Hold Time		5.0			ns	
t_h	Select Hold Time		0				

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

SN54/74LS298

AC WAVEFORMS

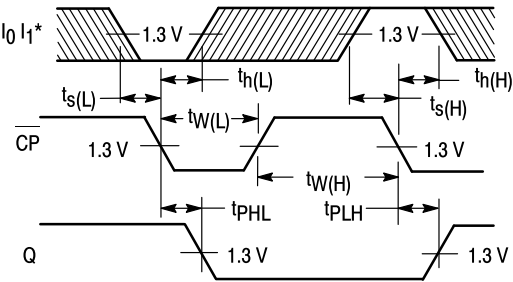


Figure 1

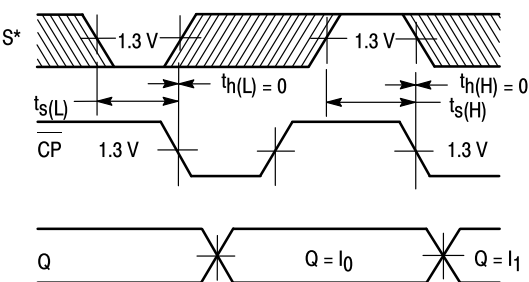
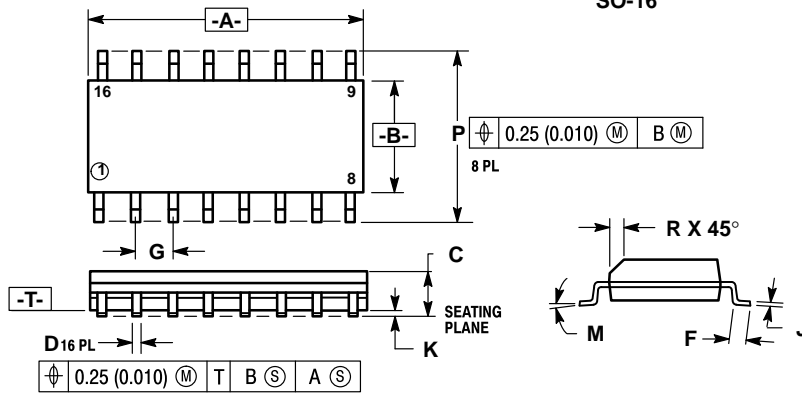


Figure 2

*The shaded areas indicate when the input is permitted to change for predictable output performance.

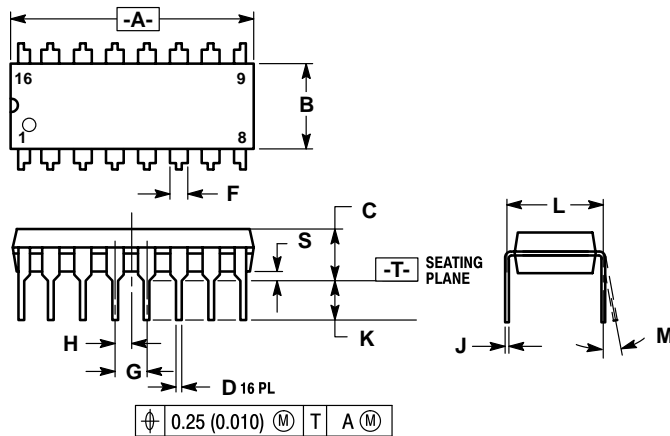
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

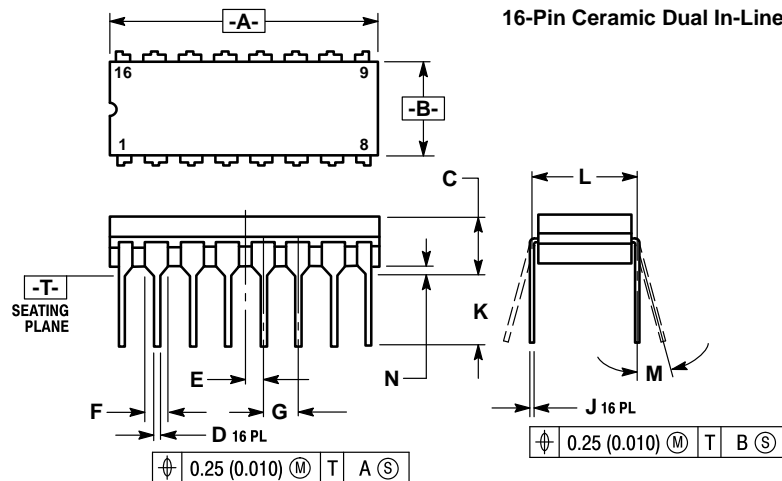
Case 648-08 N Suffix
16-Pin Plastic



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.
 6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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