Si9100/Si9101
3-W High-Voltage Switchmode Regulators

FEATURES

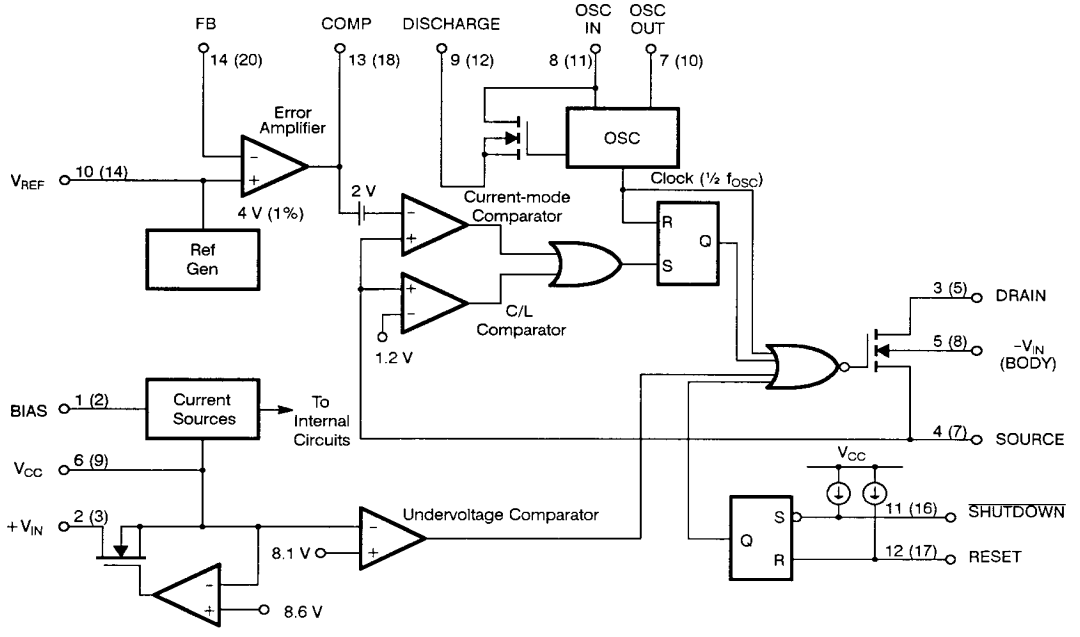
- 10 to 70 V Input Range
- Current-mode Control
- On chip 150 V, 5 Ω MOSFET Switch
- Reference Selection
  Si9100 – ±1%
  Si9101 – ±10%
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

DESCRIPTION

The Si9100/Si9101 high-voltage switchmode regulators are monolithic BiC/DMOS integrated circuits which contain most of the components necessary to implement high-efficiency dc-to-dc converters up to 3 watts. They can either be operated from a low-voltage dc supply, or directly from a 10- to 70-V unregulated dc power source. The Si9100/Si9101 may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward), or by using a level shift circuit can generate a +5 V or a -5 V non-isolated output from a -48 V source.

The Si9100/Si9101 is available in 14-pin plastic, CerDIP and PLCC 20-pin packages, and is specified over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 70 V

V_{DS} ..... 150 V

I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2.5 A

I_D (rms) ..... 350 mA

Logic Inputs (RESET, SHUTDOWN, OSC IN) ..... -0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V

HV Preregulator Input Current (continuous) ..... 3 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)*
14-Pin Ceramic DIP (K Suffix)** ..... 1000 mW
14-Pin Plastic DIP (J Suffix)*** ..... 750 mW
20-Pin PLCC (N Suffix)**** ..... 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Ceramic DIP ..... 100°C/W
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 10 mW/°C above 50°C
***Derate 6 mW/°C above 25°C
****Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 13.5 V

$+V_{IN}$ ..... 10 V to 70 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to 7 V

Digital Inputs ..... 0 to V_{CC}

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	1 = 25°C 2 = 85,125°C 3 = -40,-55°C		LIMITS A SUFFIX -55 to 125°C		LIMITS D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
REFERENCE									
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	1	4.0	3.92	4.08	3.92	4.08	V
Output Impedance[c]	Z_{OUT}		1	30	15	45	15	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	1	100	70	130	70	130	µA
Temperature Stability[c]	T_{REF}		2,3	0.1		0.25		0.25	mV/°C
OSCILLATOR									
Maximum Frequency[c]	f_{MAX}	R_{OSC} = 0	1	3	1		1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note e	1	100	80	120	80	120	kHz
		R_{OSC} = 150 k, See Note e	1	200	160	240	160	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) - f(9.5 V) / f(9.5 V)	1	10		15		15	%
Temperature Coefficient[c]	T_{OSC}		2,3	200		500		500	ppm/°C

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ERROR AMPLIFIER										
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Si9100 Si9101	1 1	4.00 4.00	3.96 3.60	4.04 4.40	3.96 3.60	4.04 4.40	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V		1	25		500		500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$, (OSC Disabled)		1	±15		±40		±40	mV
Open Loop Voltage Gain[c]	A_{VOL}			1	80	60		60		dB
Unity Gain Bandwidth[c]	BW			1	1					MHz
Dynamic Output Impedance[c]	Z_{OUT}			1	1000		2000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)		1	-2.0		-1.4		-1.4	mA
		Sink (V_{FB} = 4.5 V)		1	0.15	0.12		0.12		
Power Supply Rejection	PSRR	OSC IN = $-V_{IN}$, (OSC Disabled)		1	70	50		50		dB
CURRENT LIMIT										
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V		1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output[c]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1		1	100		200		200	ns
PREREGULATOR/STARTUP										
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA		1			70		70	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 9.4 V		1			10		10	µA
Preregulator Startup Current	I_{START}	Pulse Width $\leq$ 300 µs V_{CC} = V_{UVLO}		1	15	8		8		mA
V_{CC} Preregulator Turn-OFF Threshold Voltage	V_{REG}	$I_{PREREGULATOR}$ = 10 µA		1	8.6	7.8	9.4	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description		1	8.1	7.0	8.9	7.0	8.9	
V_{REG} - V_{UVLO}	V_{DELTA}			1	0.6	0.3		0.3		
SUPPLY										
Supply Current	I_{CC}			1	0.6	0.45	1.0	0.45	1.0	mA
Bias Current	I_{BIAS}			1	15	10	20	10	20	µA
LOGIC										
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2		1	50		100		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3		1		50		50		

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			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
LOGIC (Cont'd)									
RESET Pulse Width	t_{RW}	See Figure 3	1		50		50		ns
Latching Pulse Width SHUTDOWN and RESET LOW	t_{LW}	See Figure 3	1		25		25		ns
Input LOW Voltage	V_{IL}		1			2.0		2.0	V
Input HIGH Voltage	V_{IH}		1		8.0		8.0		V
Input Current Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1		5		5	µA
Input Current Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25	-35		-35		µA
MOSFET SWITCH									
Breakdown Voltage	$V_{(BR)DSS}$	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V I_{DRAIN} = 100 µA	2,3	180	150		150		V
Drain-Source ON Resistance[f]	$r_{DS(ON)}$	V_{SOURCE} = 0 V I_{DRAIN} = 100 mA	1	3		5		5	Ω
Drain OFF Leakage Current	I_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V V_{DRAIN} = 100 V	1			10		10	µA
Drain Capacitance	C_{DS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V	1	35					pF

[a]Refer to PROCESS OPTION FLOWCHART for additional information.
[b]The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
[c]Guaranteed by design, not subject to production test.
[d]Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
[e]C_{STRAY} Pin 8 = ≤ 5 pF
[f]Temperature coefficient of $r_{DS(ON)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

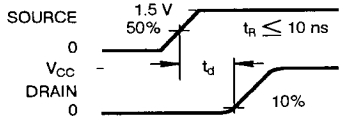


Figure 1

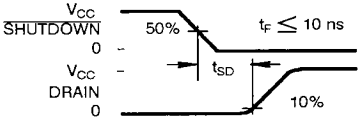


Figure 2

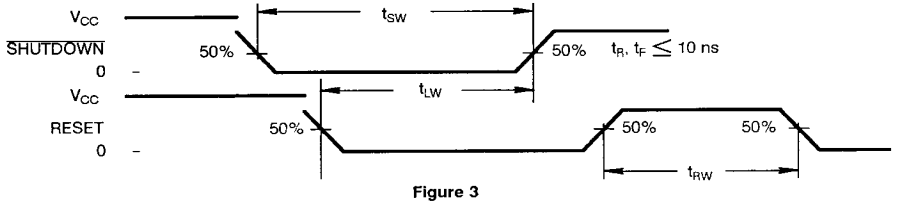


Figure 3

TYPICAL CHARACTERSITICS

Figure 4. $+V_{IN}$ vs. $+I_{IN}$ at Startup

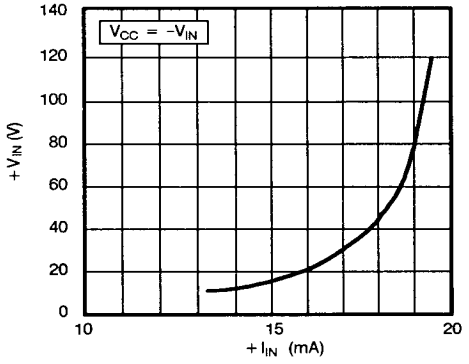
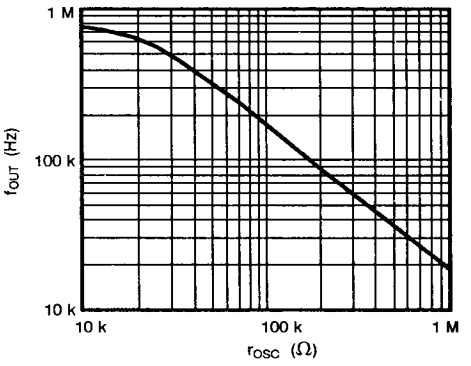
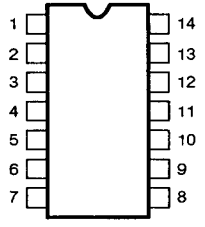


Figure 5. Output Switching Frequency vs. Oscillator Resistance



PIN CONFIGURATION

Dual-In-Line Package

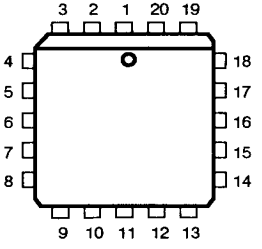


Top View

Order Numbers:

CerDIP:
Si9100AK
Plastic:
Si9100DJ, SI9101DJ

PLCC Package



Top View

Order Number:

Si9100DN, SI9101DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical preregulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9100, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. During the reference trimming procedure the error amplifier is connected for unity gain in order to compensate for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude and 0.5 μs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

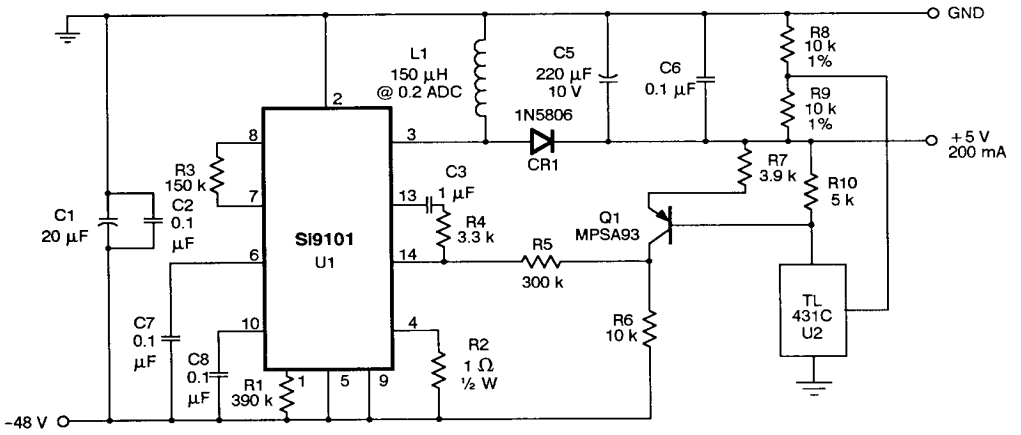
Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

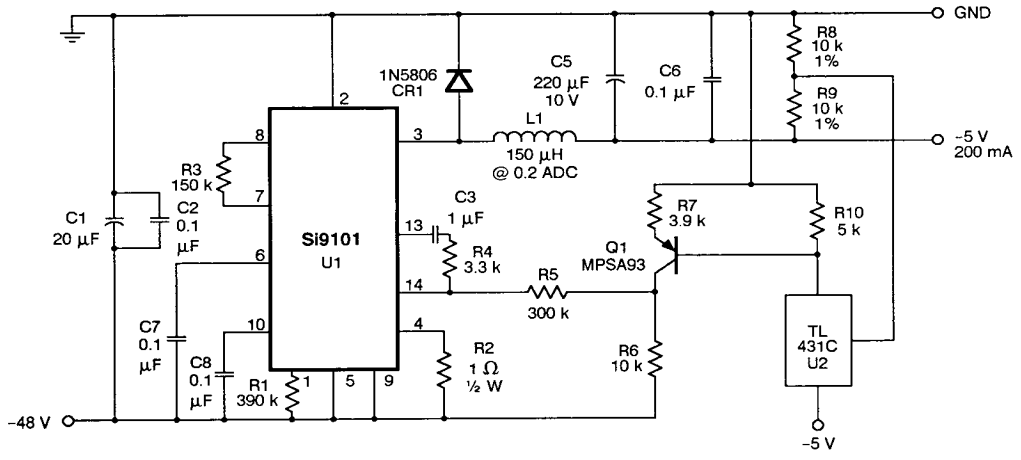
OUTPUT SWITCH

The output switch is a 5 Ω, 150 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

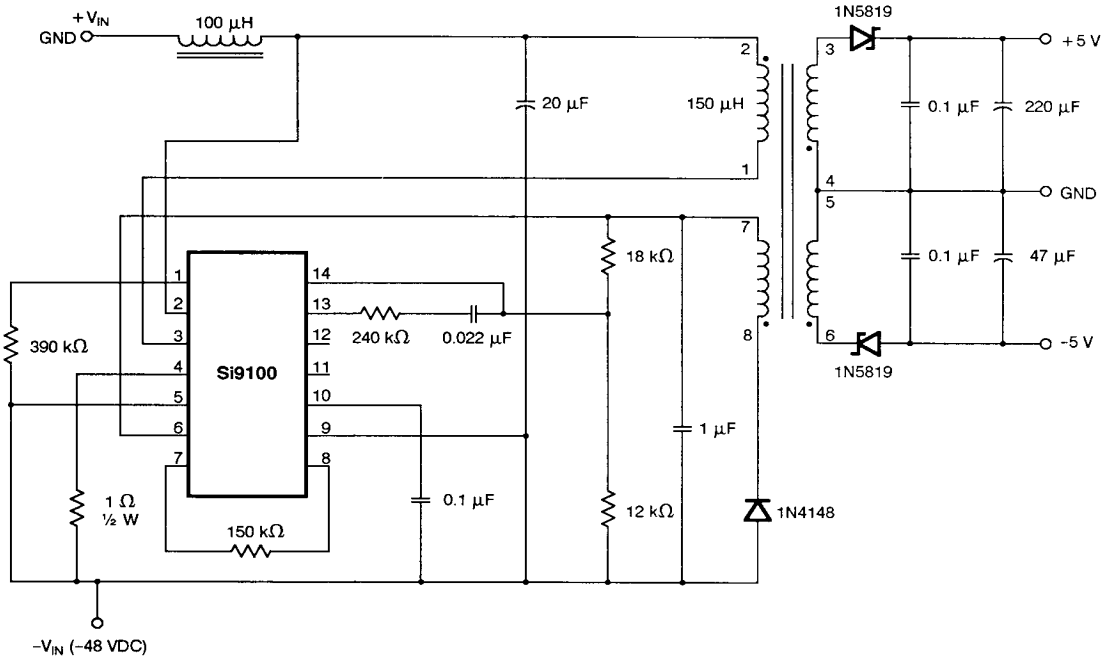
Buck-boost
Non-isolated 1-W Supply



Non-isolated 1-W Supply (Buck)



One-watt Flyback Converter for Telecommunications Power Supplies*



* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN87-1 and AN87-2.