

# DATA SHEET



## TSA5059

2.7 GHz I<sup>2</sup>C-bus controlled  
low phase noise frequency  
synthesizer

Preliminary specification  
File under Integrated Circuits, IC02

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## 2.7 GHz I<sup>2</sup>C-bus controlled low phase noise frequency synthesizer

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### FEATURES

- Complete 2.7 GHz single chip system
- Optimized for low phase noise
- Selectable divide-by-two prescaler
- Operation up to 2.7 GHz with and without divide-by-two prescaler
- Selectable reference divider ratio
- Compatible with UK-DTT (Digital Terrestrial Television) offset requirements
- Selectable crystal/comparison frequency output
- Four selectable charge pump currents
- Four selectable I<sup>2</sup>C-bus addresses
- Standard and fast mode I<sup>2</sup>C-bus
- I<sup>2</sup>C-bus compatible with 3.3 and 5 V microcontrollers
- 5-level Analog-to-Digital Converter (ADC)
- Low power consumption
- 33 V tuning voltage drive
- Three I/O ports and one output port.

### APPLICATIONS

- SAT, TV, VCR and cable tuning systems
- Digital set-top boxes.

### GENERAL DESCRIPTION

The TSA5059 is a single chip PLL frequency synthesizer designed for satellite and terrestrial tuning systems up to 2.7 GHz.

The RF preamplifier drives the 17-bit main divider enabling a step size equal to the comparison frequency, for an input frequency up to 2.7 GHz. A fixed divide-by-two additional prescaler can be inserted between the preamplifier and the main divider to give a software compatibility with

existing ICs. In this case, the step size is twice the comparison frequency.

The comparison frequency is obtained from an on-chip crystal oscillator that can also be driven from an external source. Either the crystal frequency or the comparison frequency can be switched to the XT/COMP output pin to drive the reference input of another synthesizer or the clock input of a digital demodulation IC.

Both divided and comparison frequency are compared into the fast phase detector which drives the charge pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the 33 V tuning voltage, without the need of an external transistor.

Control data is entered via the I<sup>2</sup>C-bus; five serial bytes are required to address the device, select the main divider ratio, the reference divider ratio, program the four output ports, set the charge pump current, select the prescaler by two, select the signal to switch to the XT/COMP output pin and/or select a specific test mode. Three of the four output ports can also be used as input ports and a 5-level ADC is provided. Digital information concerning the input ports and the ADC can be read out of the TSA5059 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is 'in-lock' and is read during a READ operation, as well as the Power-on reset flag. The device has four programmable addresses, programmed by applying a specific voltage at pin AS, enabling the use of multiple synthesizers in the same system.

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### QUICK REFERENCE DATA

$V_{CC}$  = 4.5 to 5.5 V;  $T_{amb}$  = -20 to +85 °C; unless otherwise specified.

| SYMBOL           | PARAMETER                    | CONDITIONS                                  | MIN. | TYP. | MAX. | UNIT |
|------------------|------------------------------|---|------|------|------|------|
| $V_{CC}$         | supply voltage               |   | 4.5  | 5.0  | 5.5  | V    |
| $I_{CC}$         | supply current               | $T_{amb}$ = 25 °C                           | 30   | 37   | 45   | mA   |
| $f_{i(RF)}$      | RF input frequency           |   | 64   | —    | 2700 | MHz  |
| $V_{i(RF)(rms)}$ | RF input voltage (RMS value) | $f_{i(RF)}$ from 64 to 150 MHz;<br>note 1   | 12.6 | —    | 300  | mV   |
|                  |                              |   | -25  | —    | +2.5 | dBm  |
|                  |                              | $f_{i(RF)}$ from 150 to 2200 MHz;<br>note 1 | 7.1  | —    | 300  | mV   |
|                  |                              |   | -30  | —    | +2.5 | dBm  |
|                  |                              | $f_{i(RF)}$ from 2.2 to 2.7 GHz;<br>note 1  | 22.4 | —    | 300  | mV   |
|                  |                              |   | -20  | —    | +2.5 | dBm  |
| $f_{xtal}$       | crystal frequency            |   | 4    | —    | 16   | MHz  |
| $T_{amb}$        | ambient temperature          |   | -20  | —    | +85  | °C   |
| $T_{stg}$        | storage temperature          |   | -40  | —    | +150 | °C   |

### Note

1. Asymmetrical drive on pin RFA or RFB; see Fig.3.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |   |          |
|-------------|---------|---|----------|
|             | NAME    | DESCRIPTION   | VERSION  |
| TSA5059T    | SO16    | plastic small outline package; 16 leads; body width 3.9 mm        | SOT109-1 |
| TSA5059TS   | SSOP16  | plastic shrink small outline package; 16 leads; body width 4.4 mm | SOT369-1 |

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### BLOCK DIAGRAM

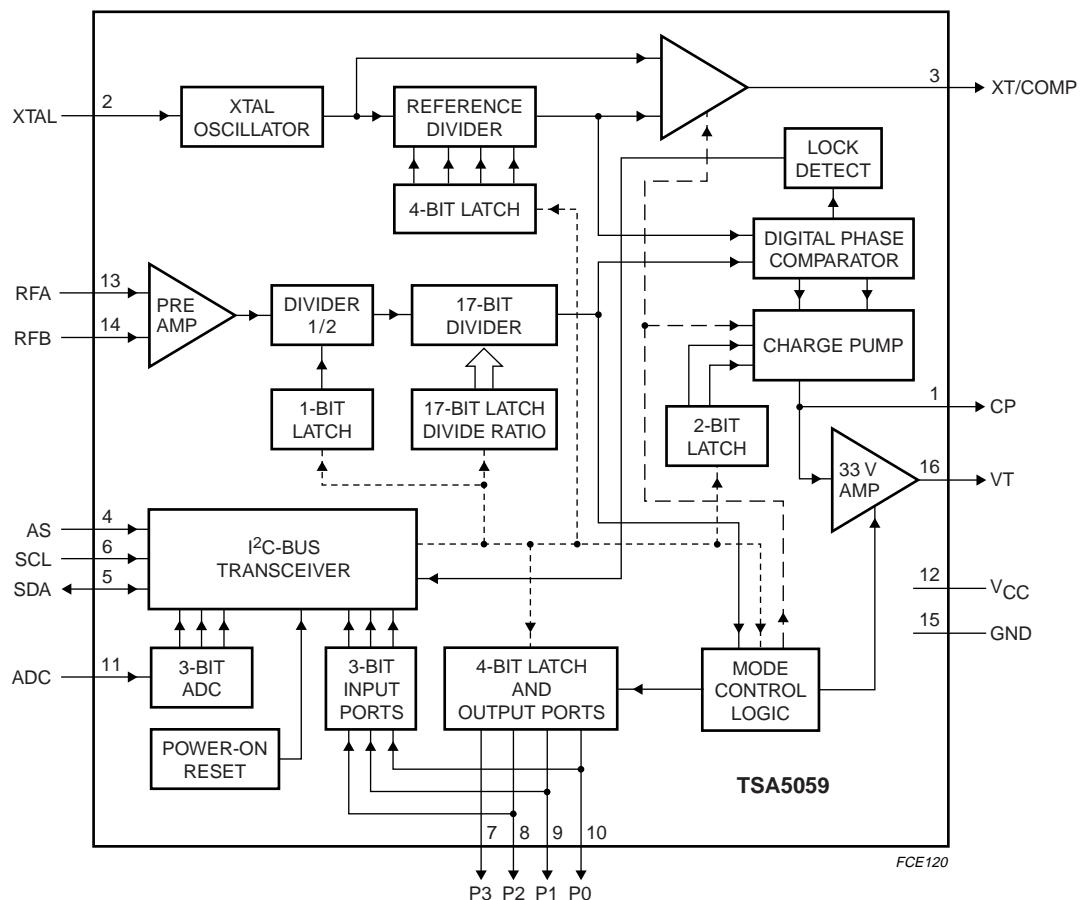


Fig.1 Block diagram.

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### PINNING

| SYMBOL          | PIN | DESCRIPTION                                   |
|-----------------|-----|---|
| CP              | 1   | charge pump output                            |
| XTAL            | 2   | crystal oscillator input                      |
| XT/COMP         | 3   | $f_{xtal}$ or $f_{comp}$ signal output        |
| AS              | 4   | I <sup>2</sup> C-bus address selection input  |
| SDA             | 5   | I <sup>2</sup> C-bus serial data input/output |
| SCL             | 6   | I <sup>2</sup> C-bus serial clock input       |
| P3              | 7   | general purpose output Port 3                 |
| P2              | 8   | general purpose input/output Port 2           |
| P1              | 9   | general purpose input/output Port 1           |
| P0              | 10  | general purpose input/output Port 0           |
| ADC             | 11  | analog-to-digital converter input             |
| V <sub>cc</sub> | 12  | supply voltage                                |
| RFA             | 13  | RF signal input A                             |
| RFB             | 14  | RF signal input B                             |
| GND             | 15  | ground supply                                 |
| VT              | 16  | tuning voltage output                         |

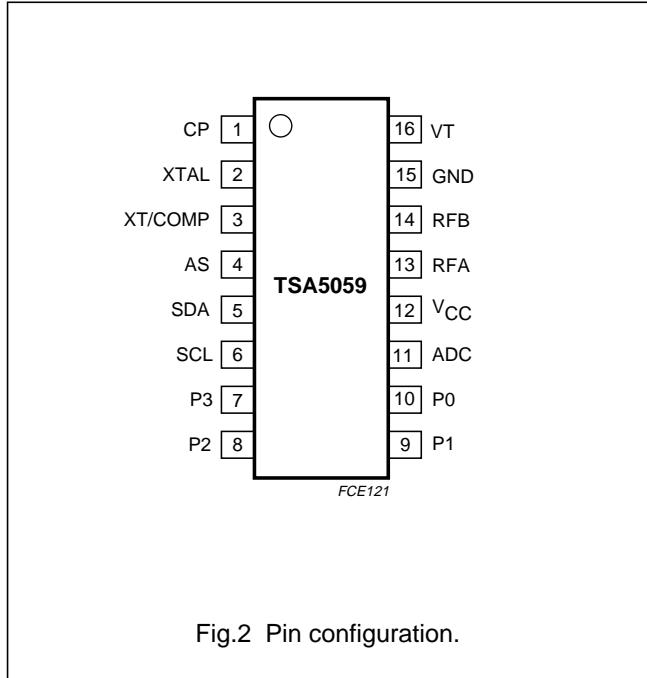


Fig.2 Pin configuration.

### FUNCTIONAL DESCRIPTION

The TSA5059 contains all the necessary elements but a reference source and a loop filter to control a varicap tuned local oscillator forming a phase locked loop frequency synthesized source. The IC is designed in a high speed process with a fast phase detector to allow a high comparison frequency to reach a low phase noise level on the oscillator.

The block diagram is shown in Fig.1. The RF signal is applied at pins RFA and RFB. Thanks to the input preamplifier a good sensitivity is provided. The output of the preamplifier is fed to the 17-bit programmable divider either through a divide-by-two prescaler or directly. Because of the internal high speed process, the RF divider is working for a frequency up to 2.7 GHz, without the need for the divide-by-two prescaler to be used. This prescaler is present on chip for compatibility reasons with existing circuits.

The output of the 17-bit programmable divider  $f_{DIV}$  is fed into the phase comparator, where it is compared in both phase and frequency with the comparison frequency  $f_{comp}$ . This frequency is derived from the signal present at pin XTAL,  $f_{xtal}$ , divided down in the reference divider. It is possible either to connect a quartz crystal to pin XTAL and then using the on-chip crystal oscillator, or to feed this pin

with a reference signal from an external source.

The reference divider can have a dividing ratio selected from 16 different values between 2 and 320, including the ratio 24 to cope with the offset requirement of the UK-DTT system, see Table 8.

The output of the phase comparator drives the charge pump and the loop amplifier section. This amplifier has an on-chip high voltage drive transistor which avoids the use of an additional external component. Pin CP is the output of the charge pump, and pin VT is the pin to drive the tuning voltage to the varicap diode of the Voltage Controlled Oscillator (VCO). The loop filter has to be connected between pins CP and VT.

In addition, it is possible to drive another PLL synthesizer, or the clock input of a digital demodulation IC, from the pin XT/COMP. It is possible to select by software either  $f_{xtal}$ , the crystal oscillator frequency or  $f_{comp}$ , the frequency present after the reference divider at this pin. It is also possible to switch off this output, in case it is not used.

For test and alignment purposes, it is possible to release the tuning voltage output to be able to apply an external voltage on it, to select one of the three charge pump test modes, and to monitor half the  $f_{DIV}$  at Port P0. See Table 10 for all possible modes.

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Four open-collector output ports are provided on the IC for general purpose; three of these can also be used as input ports. A 3-bit ADC is also available.

The TSA5059 is controlled via the two-wire I<sup>2</sup>C-bus. For programming, there is one 7-bit module address and the R/W bit for selecting READ or WRITE mode. To be able to have more than one synthesizer in an I<sup>2</sup>C-bus system, one of four possible addresses is selected depending on the voltage applied at pin AS (see Table 3).

The TSA5059 fulfills the fast mode I<sup>2</sup>C-bus, according to the Philips I<sup>2</sup>C-bus specification. The I<sup>2</sup>C-bus interface is designed in such a way that pins SCL and SDA can be connected either to 5 or to 3.3 V pulled-up I<sup>2</sup>C-bus lines, allowing the PLL synthesizer to be connected directly to the bus lines of a 3.3 V microcontroller.

### WRITE mode: R/W = 0

After the address transmission (first byte), data bytes can be sent to the device (see Table 1). Four data bytes are needed to fully program the TSA5059. The bus transceiver has an auto-increment facility that permits programming of the TSA5059 within one single transmission (address + 4 data bytes).

The TSA5059 can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether byte 2 (first bit is logic 0) or byte 4 (first bit is logic 1) will follow. Until an I<sup>2</sup>C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. To allow a smooth frequency sweep for fine tuning, and while the data of the dividing ratio of the main divider is in data bytes 2, 3 and 4, it is necessary for changing the frequency to send the data bytes 2 to 5 in a repeated sending, or to finish an incomplete transmission by a STOP condition. Repeated sending of data bytes 2 and 3 without ending the transmission does not change the dividing ratio. To illustrate, the following data sequences will change the dividing ratio:

- Bytes 2, 3, 4 and 5
- Bytes 4, 5, 2 and 3
- Bytes 2, 3, 4 and STOP
- Bytes 4, 5, 2 and STOP
- Bytes 2, 3 and STOP
- Bytes 2 and STOP
- Bytes 4 and STOP.

**Table 1** Write data format

| BYTE | DESCRIPTION          | MSB <sup>(1)</sup> |     |     |     |     |       |       |       | LSB | CONTROL BIT |
|------|----------------------|--------------------|-----|-----|-----|-----|-------|-------|-------|-----|-------------|
| 1    | address              | 1                  | 1   | 0   | 0   | 0   | MA1   | MA0   | 0     |     | A           |
| 2    | programmable divider | 0                  | N14 | N13 | N12 | N11 | N10   | N9    | N8    |     | A           |
| 3    | programmable divider | N7                 | N6  | N5  | N4  | N3  | N2    | N1    | N0    |     | A           |
| 4    | control data         | 1                  | N16 | N15 | PE  | R3  | R2    | R1    | R0    |     | A           |
| 5    | control data         | C1                 | C0  | XCE | XCS | P3  | P2/T2 | P1/T1 | P0/T0 |     | A           |

### Note

1. MSB is transmitted first.

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**Table 2** Explanation of Table 1

| BIT           | DESCRIPTION  |
|---------------|--|
| MA1 and MA0   | programmable address bits; see Table 3   |
| A             | acknowledge bit  |
| N16 to N0     | programmable main divider ratio control bits; $N = N16 \times 2^{16} + N15 \times 2^{15} + \dots + N1 \times 2^1 + N0$ |
| PE            | prescaler enable (prescaler by 2 is active when bit PE = 1)  |
| R3 to R0      | programmable reference divider ratio control bits; see Table 8   |
| C1 and C0     | charge pump current select bits; see Table 9   |
| XCE           | XT/COMP enable; XT/COMP output active when bit XCE = 1; see Table 10   |
| XCS           | XT/COMP select; signal select when bit XCE = 1, test mode enable when bit XCE = 0; see Table 10                        |
| T2, T1 and T0 | test mode select when bit XCE = 0 and bit XCS = 1; see Table 10  |
| P3, P2 and P1 | Port P3, P2 and P1 output states   |
| P0            | Port P0 output state, except in test mode; see Table 10  |

**Address selection** (see Table 3)

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having up to 4 synthesizers in one system. The relationship between MA1 and MA0 and the input voltage at pin AS is given in Table 3.

**Table 3** Address selection

| MA1 | MA0 | VOLTAGE APPLIED TO PIN AS                         |
|-----|-----|---|
| 0   | 0   | 0 to 0.1V <sub>CC</sub>                           |
| 0   | 1   | open-circuit                                      |
| 1   | 0   | 0.4V <sub>CC</sub> to 0.6V <sub>CC</sub> ; note 1 |
| 1   | 1   | 0.9V <sub>CC</sub> to V <sub>CC</sub>             |

**Note**

1. This address is selected by connecting a 15 kΩ resistor between pin AS and pin V<sub>CC</sub>.

**Status at Power-On Reset (POR)**

At power-on or when the supply voltage drops below approximately 2.75 V, internal registers are set according to Table 4.

**Table 4** Status at Power-on reset; note 1

| BYTE | DESCRIPTION          | MSB |   |   |   |                  |                  | LSB              | CONTROL BIT      |
|------|----------------------|-----|---|---|---|------------------|------------------|------------------|------------------|
| 1    | address              | 1   | 1 | 0 | 0 | 0                | MA1              | MA0              | 0                |
| 2    | programmable divider | 0   | X | X | X | X                | X                | X                | X                |
| 3    | programmable divider | X   | X | X | X | X                | X                | X                | X                |
| 4    | control data         | 1   | X | X | X | X                | X                | X                | X                |
| 5    | control data         | 0   | 0 | 0 | 1 | X <sup>(2)</sup> | 1 <sup>(2)</sup> | X <sup>(2)</sup> | X <sup>(2)</sup> |

**Notes**

1. X = don't care.
2. At Power-on reset, all output ports are in high-impedance state.

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### READ mode: R/W = 1

Data can be read out of the TSA5059 by setting the bit R/W to logic 1 (see Table 5). After the slave address has been recognized, the TSA5059 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH-level of the SCL clock signal.

A second data byte can be read out of the TSA5059 if the controller generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the controller occurs. The TSA5059 will then release the data line to allow the controller to generate a STOP condition. When ports P0 to P2 are used as inputs, they must be programmed in their high-impedance state.

The POR flag is set to logic 1 when V<sub>CC</sub> drops below approximately 2.75 V and at power-on.

It is reset to logic 0 when an end of data is detected by the TSA5059 (end of a READ sequence).

Control of the loop is made possible with the in-lock flag which indicates (bit FL = 1) when the loop is phase-locked.

The bits I2, I1 and I0 represent the status of the I/O ports P2, P1 and P0 respectively. A logic 0 indicates a LOW-level and a logic 1 indicates a HIGH-level.

A built-in 5-level ADC is available at pin ADC. This converter can be used to feed AFC information to the microcontroller through the I<sup>2</sup>C-bus. The relationship between bits A2, A1, A0 and the input voltage at pin ADC is given in Table 7.

**Table 5** Read data format

| BYTE | DESCRIPTION | MSB <sup>(1)</sup> |    |    |    |    |     |     |    | LSB | CONTROL BIT |
|------|-------------|--------------------|----|----|----|----|-----|-----|----|-----|-------------|
| 1    | address     | 1                  | 1  | 0  | 0  | 0  | MA1 | MA0 | 1  | A   |             |
| 2    | status byte | POR                | FL | I2 | I1 | I0 | A2  | A1  | A0 | –   |             |

### Note

1. MSB is transmitted first.

**Table 6** Explanation of Table 5

| BIT           | DESCRIPTION  |
|---------------|--|
| A             | acknowledge bit  |
| MA1 and MA0   | programmable address bits; see Table 3                       |
| POR           | Power-on reset flag (bit POR = 1 on power-on)                |
| FL            | in-lock flag (bit FL = 1 when the loop is phase-locked)      |
| I2, I1 and I0 | digital information for I/O ports P2, P1 and P0 respectively |
| A2, A1 and A0 | digital outputs of the 5-level ADC; see Table 7              |

**Table 7** ADC levels

| A2 | A1 | A0 | VOLTAGE APPLIED TO PIN ADC <sup>(1)</sup> |
|----|----|----|---|
| 1  | 0  | 0  | 0.6V <sub>CC</sub> to V <sub>CC</sub>     |
| 0  | 1  | 1  | 0.45V <sub>CC</sub> to 0.6V <sub>CC</sub> |
| 0  | 1  | 0  | 0.3V <sub>CC</sub> to 0.45V <sub>CC</sub> |
| 0  | 0  | 1  | 0.15V <sub>CC</sub> to 0.3V <sub>CC</sub> |
| 0  | 0  | 0  | 0 to 0.15V <sub>CC</sub>                  |

### Note

1. Accuracy is  $\pm 0.03V_{CC}$ .

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### Reference divider ratio

The reference divider ratio is set by 4 bits in the WRITE mode, giving 16 different ratios which allow to adjust the comparison frequency to different values, depending on the compromise which has to be found between step size and phase noise.

Table 8 shows the different dividing ratios and the corresponding comparison frequencies and step size, assuming the device is provided with a 4 MHz signal at pin XTAL.

The dividing ratio of 24 is implemented to fulfil the UK-DTT recommendation regarding offset frequency of  $\frac{1}{6}$  MHz.

**Table 8** Reference dividing ratios

| R3 | R2 | R1 | R0 | RATIO | COMPARISON FREQUENCY <sup>(1)</sup> | STEP                      |                           |
|----|----|----|----|-------|-------------------------------------|---------------------------|---------------------------|
|    |    |    |    |       |                                     | BIT PE = 0 <sup>(1)</sup> | BIT PE = 1 <sup>(1)</sup> |
| 0  | 0  | 0  | 0  | 2     | 2 MHz                               | 2 MHz                     | 4 MHz                     |
| 0  | 0  | 0  | 1  | 4     | 1 MHz                               | 1 MHz                     | 2 MHz                     |
| 0  | 0  | 1  | 0  | 8     | 500 kHz                             | 500 kHz                   | 1 MHz                     |
| 0  | 0  | 1  | 1  | 16    | 250 kHz                             | 250 kHz                   | 500 kHz                   |
| 0  | 1  | 0  | 0  | 32    | 125 kHz                             | 125 kHz                   | 250 kHz                   |
| 0  | 1  | 0  | 1  | 64    | 62.5 kHz                            | 62.5 kHz                  | 125 kHz                   |
| 0  | 1  | 1  | 0  | 128   | 31.25 kHz                           | 31.25 kHz                 | 62.5 kHz                  |
| 0  | 1  | 1  | 1  | 256   | 15.625 kHz                          | 15.625 kHz                | 31.25 kHz                 |
| 1  | 0  | 0  | 0  | 24    | 166.67 kHz                          | 166.67 kHz                | 333.33 kHz                |
| 1  | 0  | 0  | 1  | 5     | 800 kHz                             | 800 kHz                   | 1.6 MHz                   |
| 1  | 0  | 1  | 0  | 10    | 400 kHz                             | 400 kHz                   | 800 kHz                   |
| 1  | 0  | 1  | 1  | 20    | 200 kHz                             | 200 kHz                   | 400 kHz                   |
| 1  | 1  | 0  | 0  | 40    | 100 kHz                             | 100 kHz                   | 200 kHz                   |
| 1  | 1  | 0  | 1  | 80    | 50 kHz                              | 50 kHz                    | 100 kHz                   |
| 1  | 1  | 1  | 0  | 160   | 25 kHz                              | 25 kHz                    | 50 kHz                    |
| 1  | 1  | 1  | 1  | 320   | 12.5 kHz                            | 12.5 kHz                  | 25 kHz                    |

### Note

- Only valid when the IC is used with a 4 MHz crystal.

### Charge pump current

The charge pump current can be chosen from 4 different values depending on the value of bits C1 and C0 in the I<sup>2</sup>C-bus byte 4, according to Table 9.

**Table 9** Charge pump current

| C1 | C0 | I <sub>cp</sub> ( $\mu$ A) (absolute value) |      |      |
|----|----|---|------|------|
|    |    | MIN.  | TYP. | MAX. |
| 0  | 0  | 100   | 135  | 170  |
| 0  | 1  | 210   | 280  | 350  |
| 1  | 0  | 450   | 600  | 750  |
| 1  | 1  | 920   | 1230 | 1560 |

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### XT/COMP frequency output

It is possible to output either the crystal or the comparison frequency at this pin to be used in the application, for example to drive a second PLL synthesizer, saving a quartz crystal in the bill of material. To output  $f_{xtal}$ , it is necessary to set bit XCE to logic 1 and bit XCS to logic 0, or bit XCE to logic 0 and bit XCS to logic 1 during a test mode, while to output  $f_{comp}$ , it is necessary to set both bits XCE and XCS to logic 1.

If the output signal at this pin is not used, it is recommended to disable it, setting both bits XCE and XCS to logic 0. Table 10 shows how this pin is programmed. At power-on, the XT/COMP output is set, with the  $f_{xtal}$  signal selected.

### Prescaler enable

Even if the TSA5059 is able to work with the relation  $f_{comp} = \text{step size for an input frequency up to 2.7 GHz}$ , this IC is designed to be backward compatible with existing ICs

for which this relation is only valid for an RF frequency up to 2.0 GHz and in which it is necessary to select a fixed divide-by-two prescaler for frequencies between 2.0 and 2.7 GHz.

The prescaler is selected by setting bit PE to logic 1 and it is not in use if bit PE is set to logic 0.

For new designs, and especially if it is important to reach a low phase noise on the controlled VCO, it is recommended to set bit PE to logic 0, and not to use the prescaler, allowing the comparison frequency to be equal to the step size, whatever the RF frequency is between 64 and 2700 MHz.

### Test modes

It is possible to access the test modes setting bit XCE to logic 0 and bit XCS to logic 1. One specific test mode is then selected using bits T2, T1 and T0, as described in Table 10.

**Table 10** XT/COMP and test mode selection; note 1

| XCE | XCS | T2 | T1 | T0 | XT/COMP OUTPUT | TEST MODE   |
|-----|-----|----|----|----|----------------|---|
| 0   | 0   | X  | X  | X  | disabled       | normal operation  |
| 1   | 0   | X  | X  | X  | $f_{xtal}$     | normal operation  |
| 1   | 1   | X  | X  | X  | $f_{comp}$     | normal operation  |
| 0   | 1   | 0  | 0  | 0  | $f_{xtal}$     | test operation: charge pump sink;<br>status byte: bit FL = 1            |
| 0   | 1   | 0  | 0  | 1  | $f_{xtal}$     | test operation: charge pump source;<br>status byte: bit FL = 0          |
| 0   | 1   | 0  | 1  | 0  | $f_{xtal}$     | test operation: charge pump disabled;<br>status byte: bit FL = 0        |
| 0   | 1   | 0  | 1  | 1  | $f_{xtal}$     | test operation: $\frac{1}{2}f_{\text{DIV}}$ switched to Port P0         |
| 0   | 1   | 1  | X  | X  | $f_{xtal}$     | test operation: tuning voltage (pin VT) is off (high-impedance); note 2 |

### Notes

1. X = don't care.
2. Status at Power-on reset.

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

| SYMBOL             | PARAMETER  | CONDITIONS                  | MIN. | MAX.           | UNIT |
|--------------------|--|-----------------------------|------|----------------|------|
| $V_{CC}$           | supply voltage   |                             | -0.3 | +6.0           | V    |
| $V_{(n)}$          | voltage on pins<br>CP, XTAL, XT/COMP, AS, P0, P1,<br>P2, P3, ADC, RFA and RFB<br>SCL and SDA<br>VT |                             | -0.3 | $V_{CC} + 0.3$ | V    |
| $I_{O(SDA)}$       | serial data output current   |                             | -1.0 | +10.0          | mA   |
| $I_{O(Px)}$        | P0, P1, P2 and P3 output current   | port switched on            | -1.0 | +20.0          | mA   |
| $I_{O(\Sigma Px)}$ | sum of currents in P0, P1, P2 and P3   |                             | -    | 50.0           | mA   |
| $T_{amb}$          | ambient temperature  |                             | -20  | +85            | °C   |
| $T_{stg}$          | storage temperature  |                             | -40  | +150           | °C   |
| $T_{j(max)}$       | maximum junction temperature   |                             | -    | 150            | °C   |
| $t_{sc}$           | short-circuit time   | each pin to $V_{CC}$ or GND | -    | 10             | s    |

### Note

1. Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.

### HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

### THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER  | CONDITIONS  | VALUE | UNIT |
|---------------|--|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient<br>TSA5059T (SOT109-1; SO16)<br>TSA5059TS (SOT369-1; SSOP16) | in free air | 115   | K/W  |
|               |  |             | 144   | K/W  |

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### CHARACTERISTICS

$V_{CC}$  = 4.5 to 5.5 V;  $T_{amb}$  = -20 to +85 °C;  $f_{xtal}$  = 4 MHz; measured according to Fig.4; unless otherwise specified.

| SYMBOL                                  | PARAMETER   | CONDITIONS  | MIN. | TYP. | MAX.   | UNIT   |
|---|---|---|------|------|--------|--------|
| <b>Supply (pin <math>V_{CC}</math>)</b> |   |   |      |      |        |        |
| $V_{CC}$                                | supply voltage  |   | 4.5  | 5.0  | 5.5    | V      |
| $I_{CC}$                                | supply current  | $T_{amb}$ = 25 °C   | 30   | 37   | 45     | mA     |
| $V_{CC(POR)}$                           | supply voltage below which POR is active              | $T_{amb}$ = 25 °C   | -    | 2.75 | -      | V      |
| <b>RF inputs (pins RFA and RFB)</b>     |   |   |      |      |        |        |
| $f_{i(RF)}$                             | RF input frequency                                    |   | 64   | -    | 2700   | MHz    |
| $V_{i(RF)(rms)}$                        | RF input voltage (RMS value)                          | $f_{i(RF)}$ between 64 and 150 MHz; note 1                        | 12.6 | -    | 300    | mV     |
|   |   |   | -25  | -    | +2.5   | dBm    |
|   |   | $f_{i(RF)}$ between 150 and 2200 MHz; note 1                      | 7.1  | -    | 300    | mV     |
|   |   |   | -30  | -    | +2.5   | dBm    |
| $Z_{i(RF)}$                             | RF input impedance                                    | $f_{i(RF)}$ between 2.2 and 2.7 GHz; note 1                       | 22.4 | -    | 300    | mV     |
|   |   |   | -20  | -    | +2.5   | dBm    |
| $C_{i(RF)}$                             | RF input capacitance                                  | see Fig.7   | -    | -    | -      | Ω      |
| MDR                                     | main divider ratio                                    | prescaler disabled  | 64   | -    | 131071 |        |
|   |   | prescaler enabled   | 128  | -    | 262142 |        |
| <b>Crystal oscillator (pin XTAL)</b>    |   |   |      |      |        |        |
| $f_{xtal}$                              | crystal frequency                                     |   | 4    | -    | 16     | MHz    |
| $ Z_{XTAL} $                            | crystal oscillator negative impedance                 | 4 MHz crystal   | 400  | 680  | -      | Ω      |
| $Z_{XTAL}$                              | recommended crystal series resistance                 | 4 MHz crystal   | -    | -    | 200    | Ω      |
| $P_{XTAL}$                              | crystal drive level                                   | 4 MHz crystal; note 2   | -    | 40   | -      | μW     |
| $f_{i(ext)}$                            | external reference input frequency                    | note 3  | 2    | -    | 20     | MHz    |
| $V_{i(ext)(p-p)}$                       | external reference input voltage (peak-to-peak value) | note 3  | 200  | -    | 500    | mV     |
| <b>Phase comparator and charge pump</b> |   |   |      |      |        |        |
| $f_{comp}$                              | comparison frequency                                  |   | -    | -    | 2      | MHz    |
| $N_{comp}$                              | equivalent phase noise at the phase detector input    | $f_{comp}$ = 250 kHz;<br>$C1 = C0 = 1$ ;<br>in the loop bandwidth | -    | -157 | -      | dBc/Hz |
| $ I_{cp} $                              | charge pump current                                   | $C1 = 0$ ; $C0 = 0$   | 100  | 135  | 170    | μA     |
|   |   | $C1 = 0$ ; $C0 = 1$   | 210  | 280  | 350    | μA     |
|   |   | $C1 = 1$ ; $C0 = 0$   | 450  | 600  | 750    | μA     |
|   |   | $C1 = 1$ ; $C0 = 1$   | 920  | 1230 | 1540   | μA     |
| $I_{cpl}$                               | charge pump leakage current                           |   | -10  | 0    | +10    | nA     |

## 2.7 GHz I<sup>2</sup>C-bus controlled low phase noise frequency synthesizer

TSA5059

| SYMBOL  | PARAMETER                              | CONDITIONS   | MIN. | TYP. | MAX. | UNIT          |
|---|--|--|------|------|------|---------------|
| <b>Tuning voltage output (pin VT)</b>                         |  |  |      |      |      |               |
| $I_{IO(off)}$   | leakage current when switched off      | $XCE = 0; XCS = 1; T2 = 1; V_{VT} = 33 \text{ V}$  | –    | –    | –10  | $\mu\text{A}$ |
| $V_O$   | output voltage                         | when the loop is locked; normal mode; $V_{VT} = 33 \text{ V}$ ; pull-up resistor of $27 \text{ k}\Omega$ | 0.25 | –    | 32.7 | V             |
| <b>XT/COMP output (pin XT/COMP)</b>                           |  |  |      |      |      |               |
| $V_{O(p-p)}$  | AC output voltage (peak-to-peak value) | $XCE = 1$  | –    | 400  | –    | mV            |
| <b>Input/output and output ports (pins P0, P1, P2 and P3)</b> |  |  |      |      |      |               |
| $I_{IO}$  | port leakage current                   | port off; $V_O = V_{CC}$   | –    | –    | 10   | $\mu\text{A}$ |
| $V_{O(sat)}$  | output port saturation voltage         | port on; $I_{sink} = 10 \text{ mA}$  | –    | 0.2  | 0.4  | V             |
| $V_{IL}$  | LOW-level input voltage                |  | –    | –    | 1.5  | V             |
| $V_{IH}$  | HIGH-level input voltage               |  | 3.0  | –    | –    | V             |
| <b>ADC input (pin ADC)</b>                                    |  |  |      |      |      |               |
| $I_{LIH}$   | HIGH-level input leakage current       | $V_{ADC} = V_{CC}$   | –    | –    | 10   | $\mu\text{A}$ |
| $I_{LIL}$   | LOW-level input leakage current        | $V_{ADC} = 0 \text{ V}$  | –10  | –    | –    | $\mu\text{A}$ |
| <b>Address selection (pin AS)</b>                             |  |  |      |      |      |               |
| $I_{LIH}$   | HIGH-level input leakage current       | $V_{AS} = V_{CC}$  | –    | –    | 1    | mA            |
| $I_{LIL}$   | LOW-level input leakage current        | $V_{AS} = 0 \text{ V}$   | –0.5 | –    | –    | mA            |
| <b>SCL and SDA inputs (pins SCL and SDA)</b>                  |  |  |      |      |      |               |
| $V_{IL}$  | LOW-level input voltage                |  | –    | –    | 1.5  | V             |
| $V_{IH}$  | HIGH-level input voltage               |  | 2.3  | –    | –    | V             |
| $I_{LIH}$   | HIGH-level input leakage current       | $V_{IH} = 5.5 \text{ V}$<br>$V_{CC} = 5.5 \text{ V}$<br>$V_{CC} = 0 \text{ V}$                           | –    | –    | 10   | $\mu\text{A}$ |
| $I_{LIL}$   | LOW-level input leakage current        | $V_{IL} = 0 \text{ V}; V_{CC} = 5.5 \text{ V}$   | –10  | –    | –    | $\mu\text{A}$ |
| $f_{SCL}$   | SCL clock frequency                    |  | –    | –    | 400  | kHz           |
| <b>SDA output (pin SDA)</b>                                   |  |  |      |      |      |               |
| $V_{O(ack)}$  | output voltage during acknowledge      | $I_{sink} = 3 \text{ mA}$  | –    | –    | 0.4  | V             |
|   |  | $I_{sink} = 6 \text{ mA}$  | –    | –    | 0.6  | V             |

**Notes**

1. Asymmetrical drive on pin RFA or RFB; see Fig.3.
2. The drive level is expected with the crystal at series resonance with a series resistance of  $50 \Omega$ . The value will be different with another crystal.
3. To drive pin XTAL from the pin XT/COMP of another TSA5059, couple the signal through a capacitor of  $1 \text{ nF}$  (to remove the DC level), in series with an  $1.2 \text{ k}\Omega$  resistor, see Fig.5.

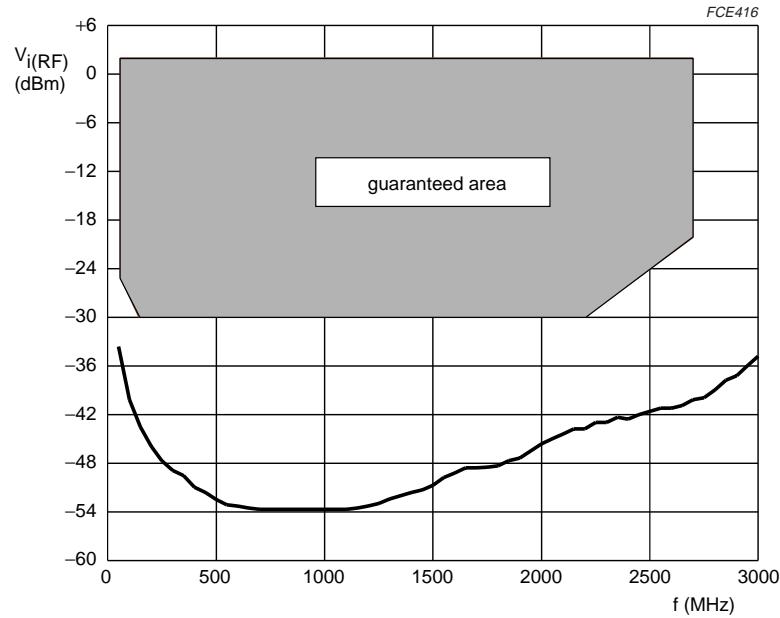
**2.7 GHz I<sup>2</sup>C-bus controlled low phase noise frequency synthesizer****TSA5059**

Fig.3 Sensitivity curve.

## 2.7 GHz I<sup>2</sup>C-bus controlled low phase noise frequency synthesizer

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### APPLICATION INFORMATION

An example of a typical application is given in Fig.4. In this application the VCO centre frequency is 1.5 GHz, with a slope of 100 MHz/V; the expected loop bandwidth is 10 kHz with a charge pump current of 555  $\mu$ A and  $f_{comp}$  of 250 kHz. Filter components need to be adapted to each application depending on the VCO characteristics and the required performance of the loop.

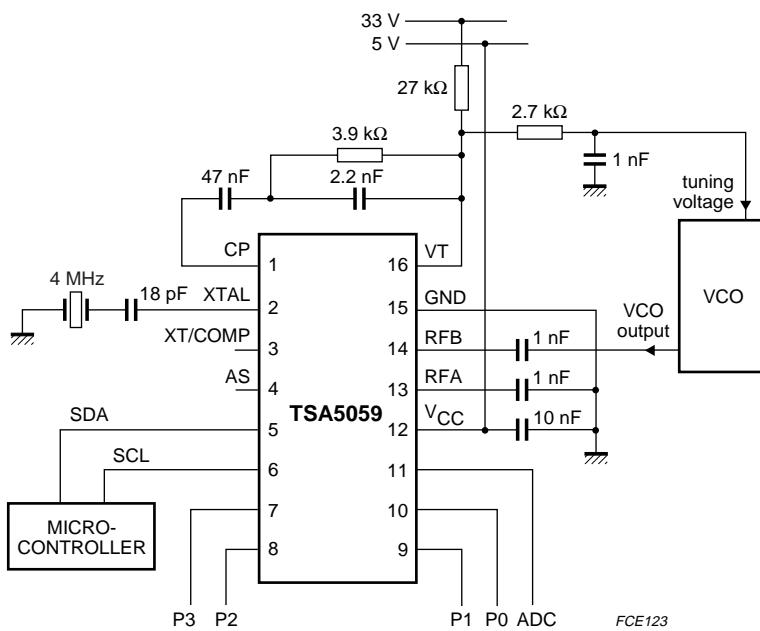


Fig.4 Typical application.

### Loop bandwidth

Most of the applications the TSA5059 are dedicated for require a large loop bandwidth, in the order of a few kHz to a few tens of kHz. The calculation of the loop filter elements has to be done for each application, while it depends on the VCO slope and phase noise, as well as the reference frequency and charge pump current.

A simulation of the loop can easily be done by using the SIMPATA software from Philips.

### Reference source

The TSA5059 is well suited to be used with a 4 MHz crystal connected to pin XTAL. Philips crystal ordering code 4322 143 04093 is recommended in this case.

It is however possible to use a crystal with an higher frequency (up to 16 MHz) to improve the noise performance. When choosing a crystal, one should take notice to select a crystal able to withstand the drive level of the TSA5059 without suffering from accelerated ageing.

It is also possible to feed pin XTAL with an external signal between 2 and 20 MHz, coming from an external oscillator or from the pin XT/COMP of another TSA5059, when more than one synthesizer is present in the same application. Then the application given in Fig.5 should be used.

If the signal at pin XT/COMP is not used in an application, the output should be switched off (XCE = 0, XCS = 0). This pin should then be open.

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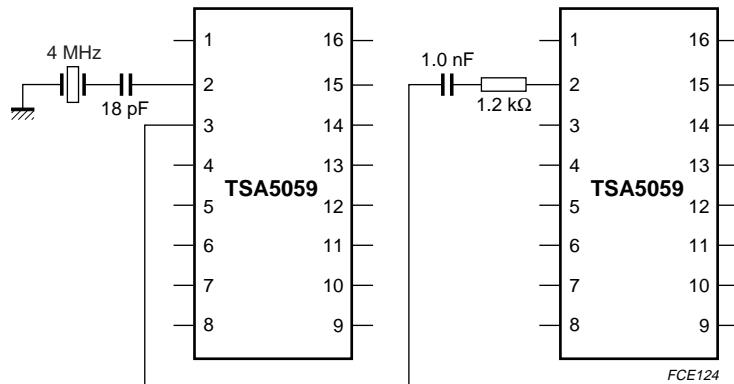


Fig.5 Application for using one crystal with two TSA5059s.

### I<sup>2</sup>C-bus crosstalk and loop amplifier

The TSA5059 includes a loop amplifier between pin CP and pin VT. While this amplifier shares the same ground pin as the I<sup>2</sup>C-bus, there may be some I<sup>2</sup>C-bus crosstalk.

The best way to avoid any I<sup>2</sup>C-bus crosstalk, both in the PLL IC and in the application (i.e. parasitic coupling between the I<sup>2</sup>C-bus lines and the VCO coil), is to avoid the I<sup>2</sup>C-bus signal to come in the RF part by using an I<sup>2</sup>C-bus gate that allows only the messages for the PLL to go to the PLL, and to avoid unnecessary repeated sending. Such a gate is integrated in most of the Philips digital demodulators.

If I<sup>2</sup>C-bus crosstalk is still a problem, it is possible not to use the internal amplifier, and to replace it with a NMOS transistor in the application as given in Fig.6. In this case the pin VT is left open, and it is possible to implement on the PCB the foot print for a jumper between the tuning voltage line and pin VT to be able to choose either the internal amplifier (mounting the jumper and not the NMOS transistor) or the external amplifier (mounting the NMOS transistor and not the jumper). It is recommended to use a BSH111 or BSH121 N-channel MOS transistor. The threshold voltage of the transistor has to be lower than 2.0 V.

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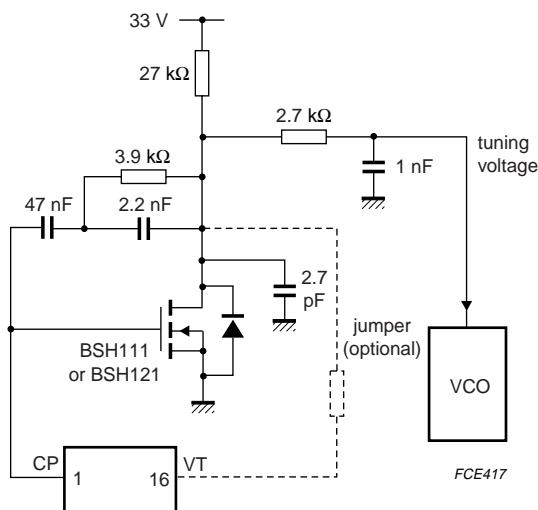


Fig.6 Application for using an external loop amplifier.

### RF input impedance

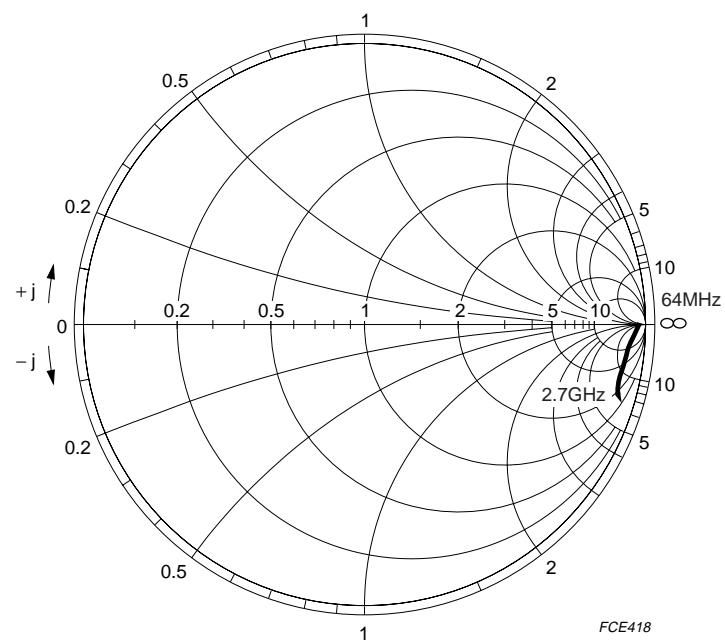


Fig.7 RF input impedance.

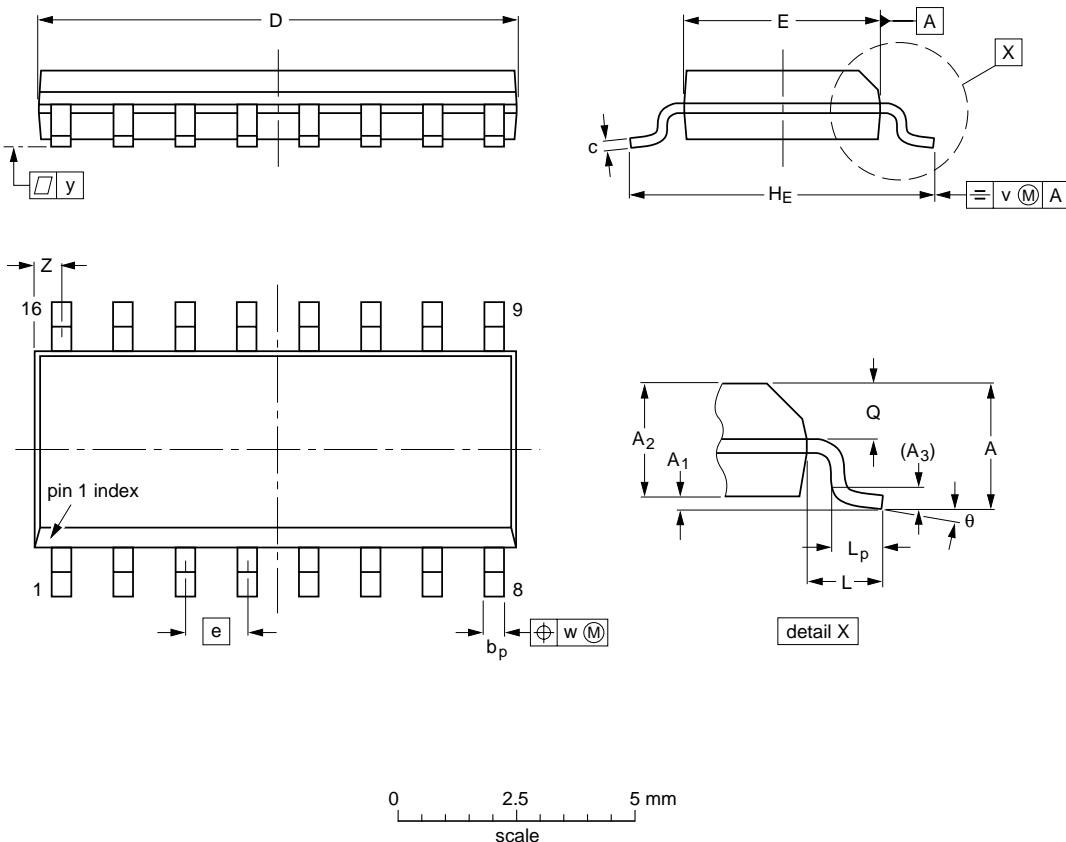
## 2.7 GHz I<sup>2</sup>C-bus controlled low phase noise frequency synthesizer

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### PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c                | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | z <sup>(1)</sup> | θ        |
|--------|-----------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75      | 0.25<br>0.10   | 1.45<br>1.25   | 0.25           | 0.49<br>0.36   | 0.25<br>0.19     | 10.0<br>9.8      | 4.0<br>3.8       | 1.27  | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069     | 0.010<br>0.004 | 0.057<br>0.049 | 0.01           | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38     | 0.16<br>0.15     | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

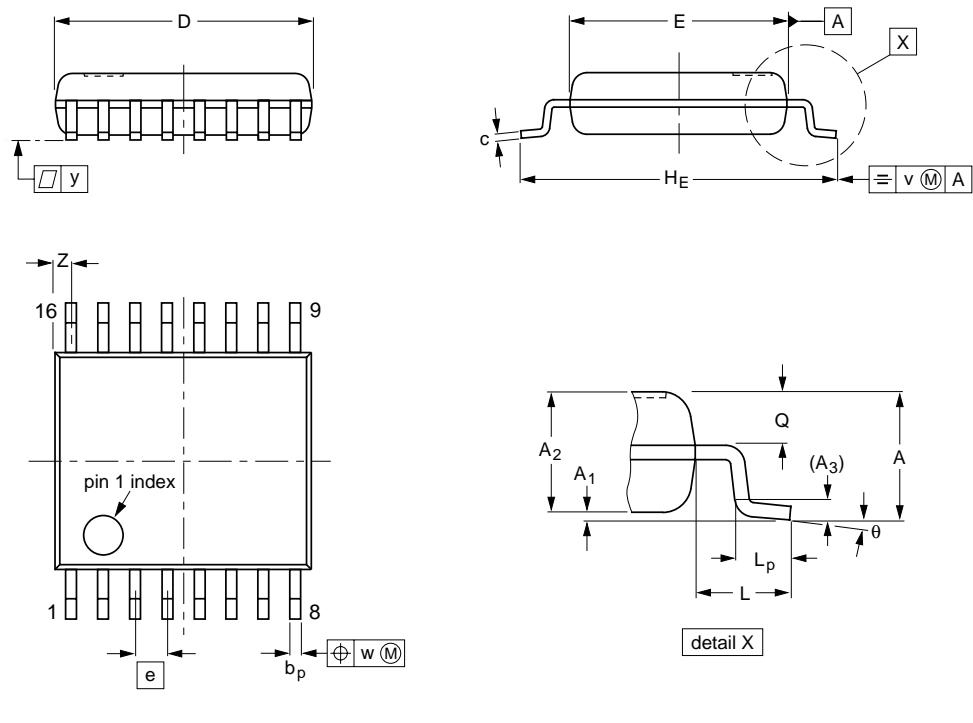
| OUTLINE<br>VERSION | REFERENCES |          |      |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|----------|------|--|------------------------|----------------------|
|                    | IEC        | JEDEC    | EIAJ |  |                        |                      |
| SOT109-1           | 076E07S    | MS-012AC |      |  |                        | 95-01-23<br>97-05-22 |

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SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm

SOT369-1



## DIMENSIONS (mm are the original dimensions)

| UNIT | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q            | v   | w    | y   | z <sup>(1)</sup> | θ         |
|------|-----------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|-----|----------------|--------------|-----|------|-----|------------------|-----------|
| mm   | 1.5       | 0.15<br>0.00   | 1.4<br>1.2     | 0.25           | 0.32<br>0.20   | 0.25<br>0.13 | 5.30<br>5.10     | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.45   | 0.65<br>0.45 | 0.2 | 0.13 | 0.1 | 0.48<br>0.18     | 10°<br>0° |

## Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |       |      |  | EUROPEAN<br>PROJECTION | ISSUE DATE            |
|--------------------|------------|-------|------|--|------------------------|-----------------------|
|                    | IEC        | JEDEC | EIAJ |  |                        |                       |
| SOT369-1           |            |       |      |  |                        | -94-04-20<br>95-02-04 |

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                         | SOLDERING METHOD                  |                       |
|---------------------------------|-----------------------------------|-----------------------|
|                                 | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                       | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ   | suitable                          | suitable              |
| LQFP, QFP, TQFP                 | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                | not recommended <sup>(5)</sup>    | suitable              |

### Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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### DEFINITIONS

| <b>Data sheet status</b>  |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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