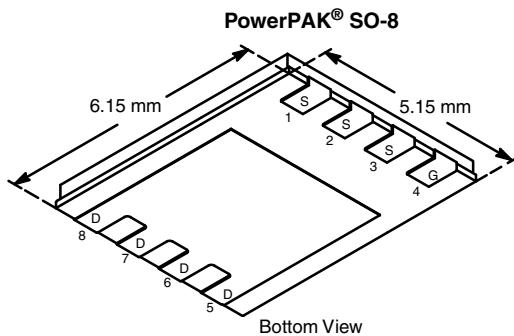


N-Channel 30 V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
30	0.0034 at V _{GS} = 10 V	60	23 nC
	0.0042 at V _{GS} = 4.5 V	60	



Ordering Information:
Si7794DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

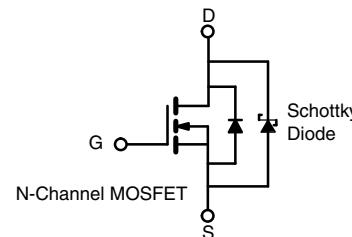
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- SkyFET® Monolithic TrenchFET® Gen III Power MOSFET and Schottky Diode
- 100 % R_g Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Low Side in V_{core}, System and Memory - Notebook PCs



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	60 ^a	A
	T _C = 70 °C	60 ^a	
	T _A = 25 °C	28.6 ^{b, c}	
	T _A = 70 °C	22.8 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	80	
Continuous Source-Drain Diode Current	T _C = 25 °C	60 ^a	
	T _A = 25 °C	5.6 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	40	
Single Pulse Avalanche Energy	E _{AS}	80	mJ
Maximum Power Dissipation	T _C = 25 °C	48	W
	T _C = 70 °C	31	
	T _A = 25 °C	5.0 ^{b, c}	
	T _A = 70 °C	3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	20	25
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.1	2.6

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?273257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

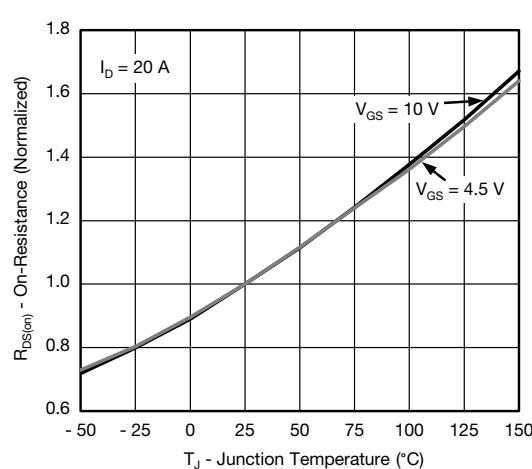
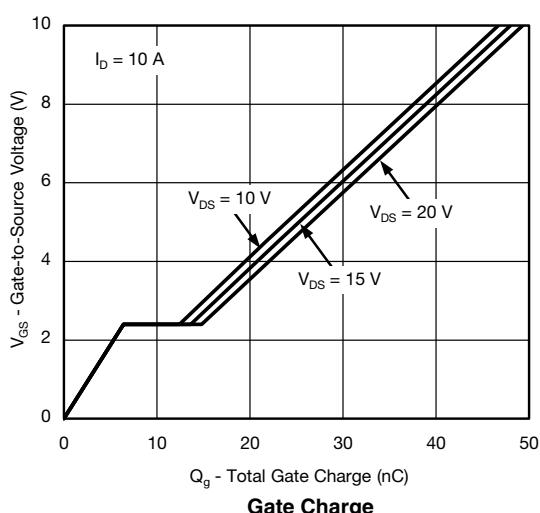
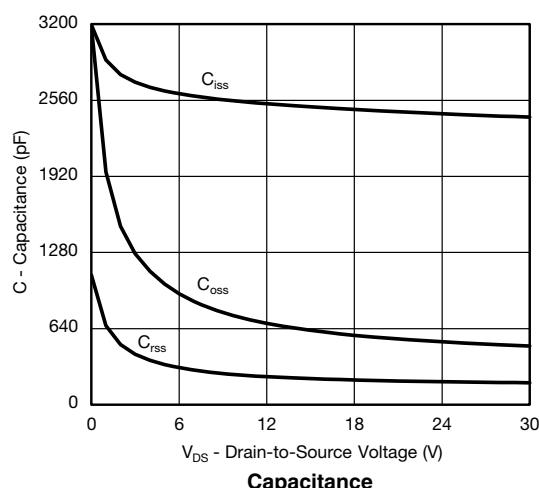
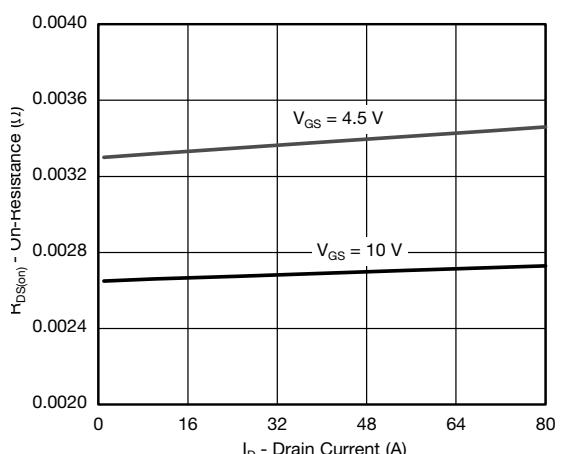
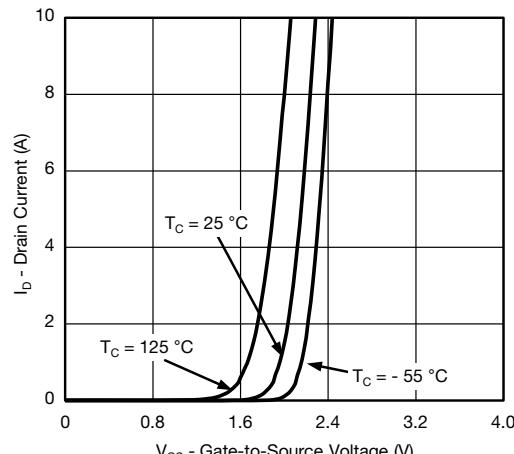
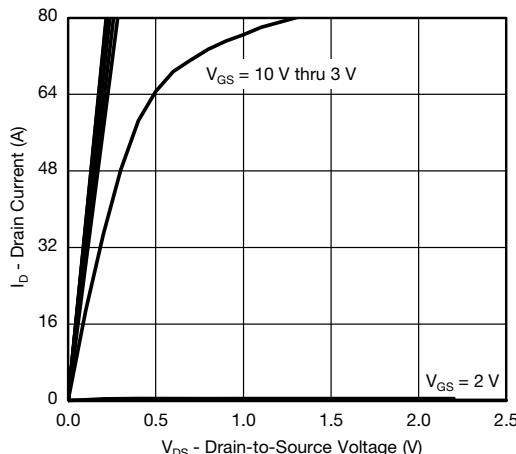
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$	30			V
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1		2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$		0.035	0.2	mA
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 100^\circ\text{C}$		3	30	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$		0.0027	0.0034	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$		0.0033	0.0042	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 20 \text{ A}$		85		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		2520		pF
Output Capacitance	C_{oss}			630		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$		48	72	nC
				23	35	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 10 \text{ A}$		6.4		
Gate-Drain Charge	Q_{gd}			7.2		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.3	1.1	2.2	Ω
Turn-On Delay Time	$t_{d(\text{on})}$		22	40	ns	
Rise Time	t_r	$V_{DD} = 15 \text{ V}$, $R_L = 1.5 \Omega$ $I_D \equiv 10 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$		16		30
Turn-Off Delay Time	$t_{d(\text{off})}$			30		55
Fall Time	t_f			10		20
Turn-On Delay Time	$t_{d(\text{on})}$			11		22
Rise Time	t_r	$V_{DD} = 15 \text{ V}$, $R_L = 1.5 \Omega$ $I_D \equiv 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		10		20
Turn-Off Delay Time	$t_{d(\text{off})}$			30		55
Fall Time	t_f			10		20
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 3 \text{ A}$		0.39	0.5	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		28	55	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	34	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			14		

Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

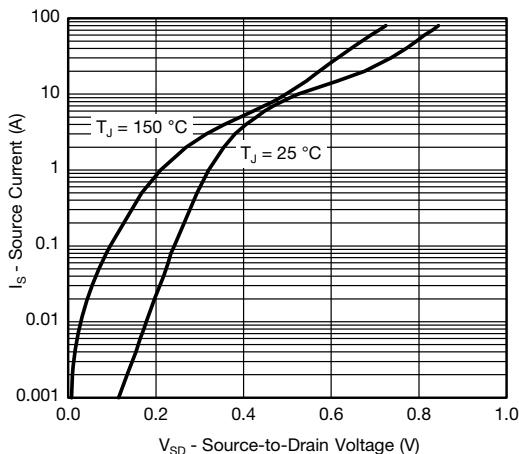
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Si7794DP

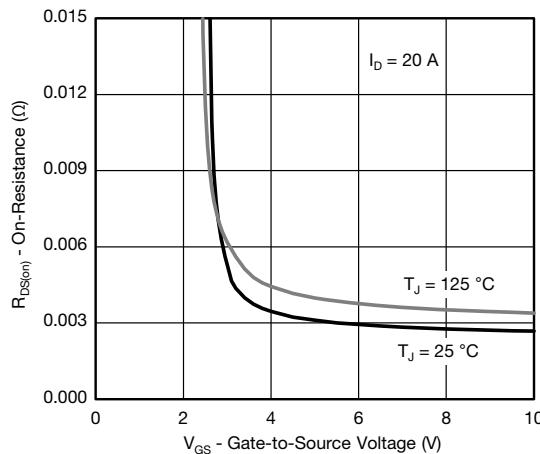
Vishay Siliconix



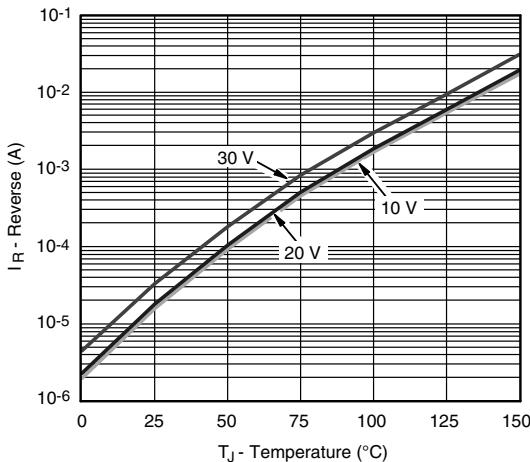
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



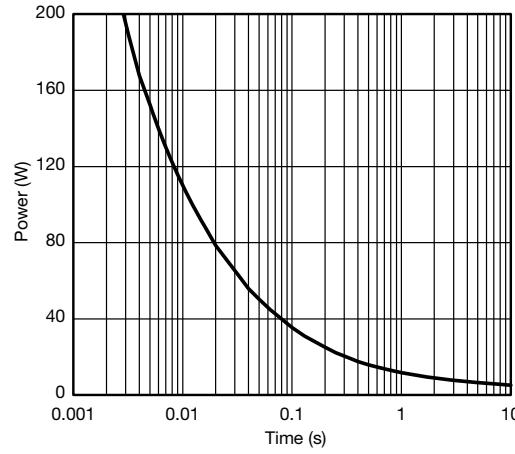
Source-Drain Diode Forward Voltage



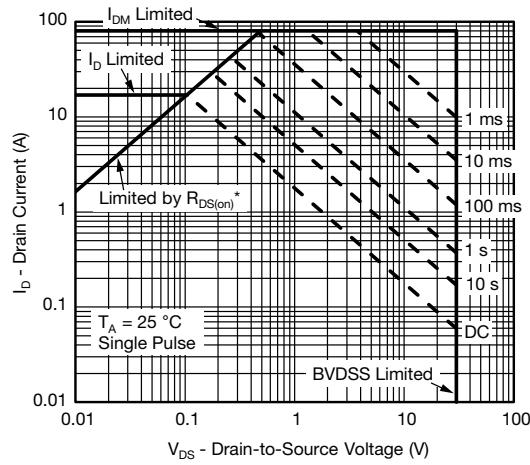
On-Resistance vs. Gate-to-Source Voltage

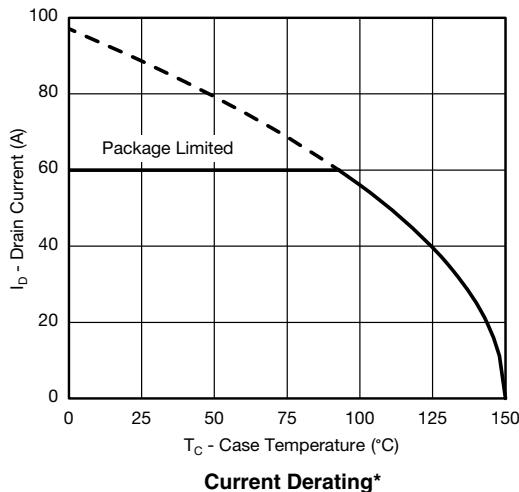


Reverse Current (Schottky)

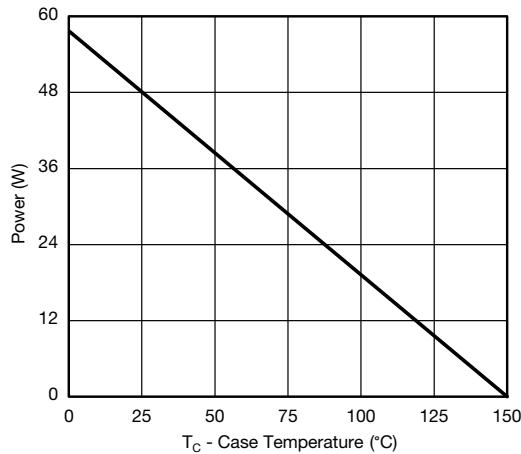


Single Pulse Power, Junction-to-Ambient

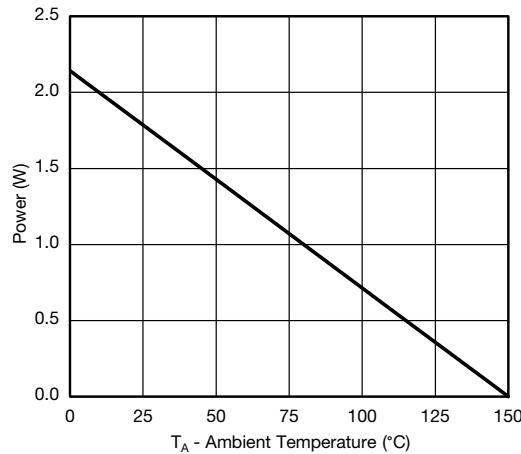
Safe Operating Area, Junction-to-Ambient
* V_GS > minimum V_GS at which R_DS(on) is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

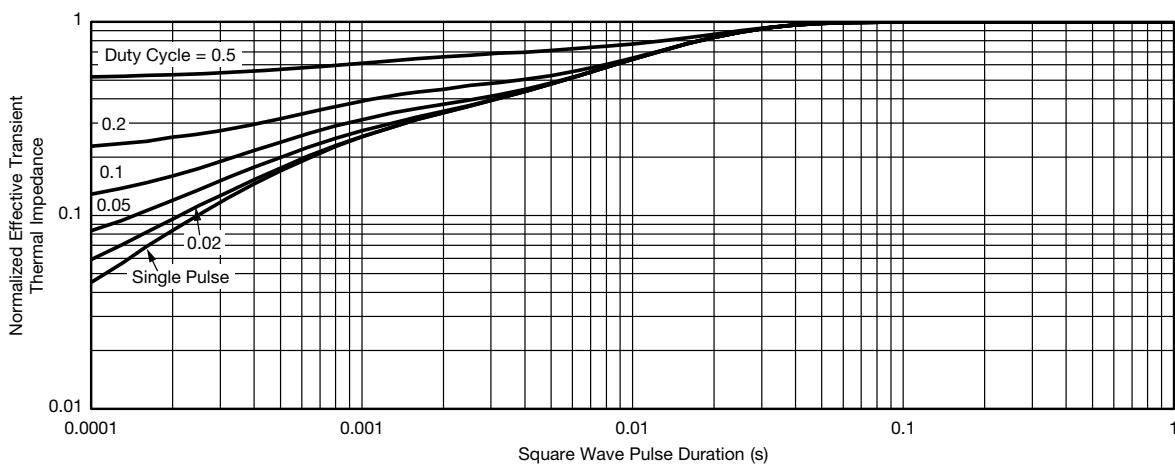
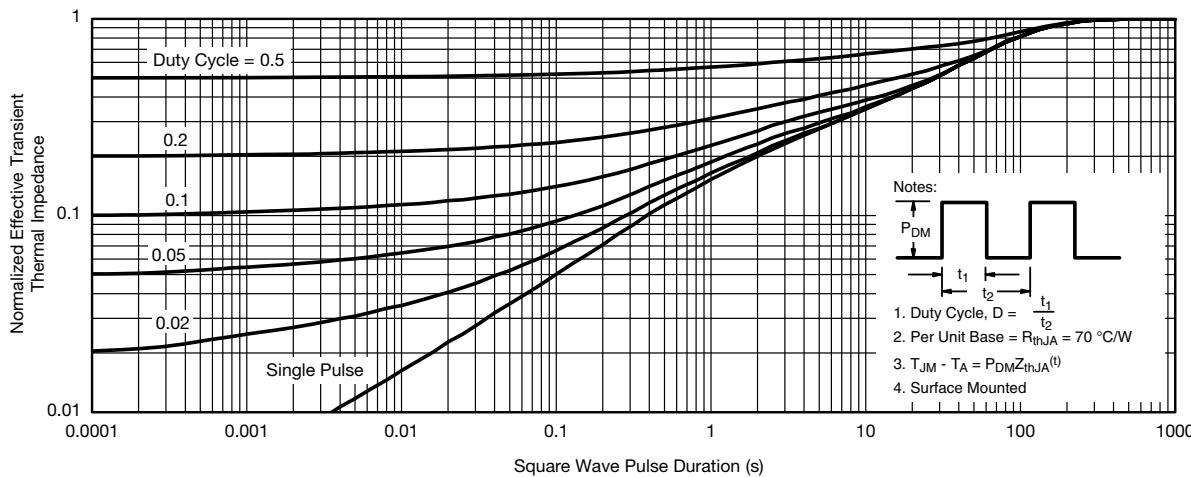
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7794DP

Vishay Siliconix

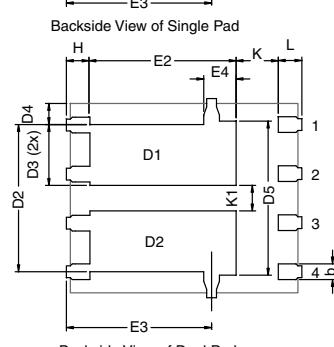
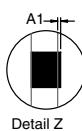
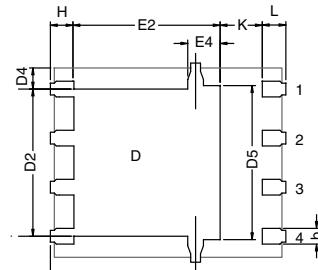
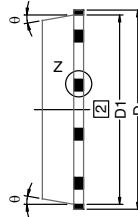
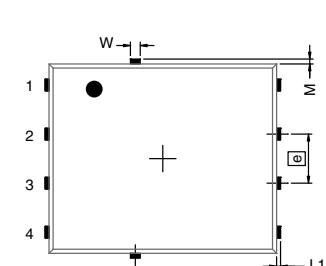


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67692.

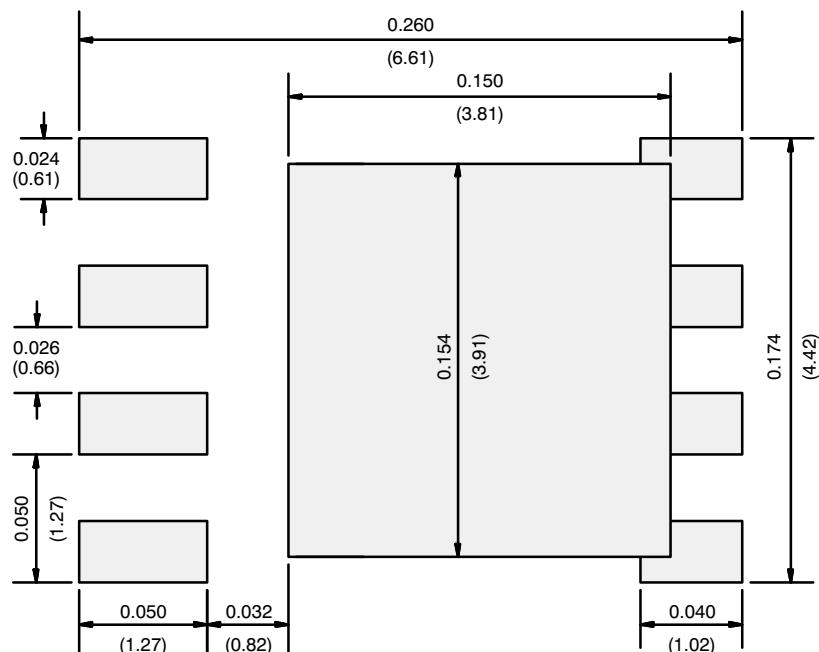
PowerPAK® SO-8, (Single/Dual)


Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
c	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4	0.57 typ.			0.0225 typ.			
D5	3.98 typ.			0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)	0.58 typ.			0.023 typ.			
E4 (for other product)	0.75 typ.			0.030 typ.			
e	1.27 BSC			0.050 BSC			
K (for AL product)	1.45 typ.			0.057 typ.			
K (for other product)	1.27 typ.			0.050 typ.			
K1	0.56	-	-	0.022	-	-	
H	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
M	0.125 typ.			0.005 typ.			

ECN: C13-0702-Rev. K, 20-May-13
DWG: 5881

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single

Recommended Minimum Pads
Dimensions in Inches/(mm)

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