

## N-Channel and P-Channel Enhancement-Mode Dual MOSFET

### Features

- Low Threshold
- Low On-resistance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage
- Independent, Electrically Isolated N-channel and P-channel

### Applications

- Medical Ultrasound Transmitters
- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interface

### General Description

The TC2320 consists of a high-voltage, low-threshold N-channel and P-channel MOSFET in an 8-Lead SOIC package. This Enhancement-mode (normally-off) transistor uses an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

### Package Type



See [Table 2-1](#) for pin information.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

|                                                     |                   |
|-----------------------------------------------------|-------------------|
| Drain-to-source Voltage.....                        | BV <sub>DSS</sub> |
| Drain-to-gate Voltage .....                         | BV <sub>DGS</sub> |
| Gate-to-source Voltage .....                        | ±20V              |
| Operating Ambient Temperature, T <sub>A</sub> ..... | –55°C to +150°C   |
| Storage Temperature, T <sub>S</sub> .....           | –55°C to +150°C   |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### N-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, T<sub>A</sub> = T<sub>J</sub> = +25°C.

| Parameter                                      | Sym.                 | Min. | Typ. | Max. | Unit  | Conditions                                                                                        |
|------------------------------------------------|----------------------|------|------|------|-------|---------------------------------------------------------------------------------------------------|
| DC PARAMETER (Note 1)                          |                      |      |      |      |       |                                                                                                   |
| Drain-to-source Breakdown Voltage              | BV <sub>DSS</sub>    | 200  | —    | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 100 μA                                                     |
| Gate Threshold Voltage                         | V <sub>GS(th)</sub>  | 0.6  | —    | 2    | V     | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1 mA                                         |
| Change in V <sub>GS(th)</sub> with Temperature | ΔV <sub>GS(th)</sub> | —    | —    | −4.5 | mV/°C | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1 mA (Note 2)                                |
| Gate Body Leakage Current                      | I <sub>GSS</sub>     | —    | —    | 100  | nA    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V                                                      |
| Zero-gate Voltage Drain Current                | I <sub>DSS</sub>     | —    | —    | 1    | μA    | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 100V                                                      |
|                                                |                      | —    | —    | 10   | μA    | V <sub>GS</sub> = 0V, V <sub>DS</sub> = Maximum rating                                            |
|                                                |                      | —    | —    | 1    | mA    | V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C,<br>V <sub>DS</sub> = 0.8 Maximum rating<br>(Note 2) |
| On-state Drain Current                         | I <sub>D(ON)</sub>   | 0.6  | —    | —    | A     | V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 25V                                                     |
|                                                |                      | 1.2  | —    | —    |       | V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V                                                      |
| Static Drain-to-Source On-state Resistance     | R <sub>DS(ON)</sub>  | —    | —    | 8    | Ω     | V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 150 mA                                                   |
|                                                |                      | —    | —    | 7    |       | V <sub>GS</sub> = 10V, I <sub>D</sub> = 1A                                                        |
| Change in R <sub>DS(ON)</sub> with Temperature | ΔR <sub>DS(ON)</sub> | —    | —    | 1    | %/°C  | V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 150 mA (Note 2)                                          |
| AC PARAMETER (Note 2)                          |                      |      |      |      |       |                                                                                                   |
| Forward Transconductance                       | G <sub>FS</sub>      | 150  | —    | —    | mmho  | V <sub>DS</sub> = 25V, I <sub>D</sub> = 200 mA                                                    |
| Input Capacitance                              | C <sub>ISS</sub>     | —    | —    | 110  | pF    | V <sub>GS</sub> = 0V,<br>V <sub>DS</sub> = 25V,<br>f = 1 MHz                                      |
| Common Source Output Capacitance               | C <sub>OSS</sub>     | —    | —    | 60   |       |                                                                                                   |
| Reverse Transfer Capacitance                   | C <sub>RSS</sub>     | —    | —    | 23   |       |                                                                                                   |
| Turn-on Delay Time                             | t <sub>d(ON)</sub>   | —    | —    | 20   | ns    | V <sub>DD</sub> = 25V,<br>I <sub>D</sub> = 150 mA,<br>R <sub>GEN</sub> = 25Ω                      |
| Rise Time                                      | t <sub>r</sub>       | —    | —    | 15   |       |                                                                                                   |
| Turn-off Delay Time                            | t <sub>d(OFF)</sub>  | —    | —    | 25   |       |                                                                                                   |
| Fall Time                                      | t <sub>f</sub>       | —    | —    | 25   |       |                                                                                                   |
| DIODE PARAMETER                                |                      |      |      |      |       |                                                                                                   |
| Diode Forward Voltage Drop                     | V <sub>SD</sub>      | —    | —    | 1.8  | V     | V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200 mA (Note 1)                                           |
| Reverse Recovery Time                          | t <sub>rr</sub>      | —    | 300  | —    | ns    | V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200 mA (Note 2)                                           |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at +25°C.

Pulse test: 300 µs pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

## P-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

| Electrical Specifications: Unless otherwise noted, T <sub>A</sub> = T <sub>J</sub> = +25°C. |                      |       |      |      |       |                                                                                                   |
|---------------------------------------------------------------------------------------------|----------------------|-------|------|------|-------|---------------------------------------------------------------------------------------------------|
| Parameter                                                                                   | Sym.                 | Min.  | Typ. | Max. | Unit  | Conditions                                                                                        |
| DC PARAMETER (Note 1)                                                                       |                      |       |      |      |       |                                                                                                   |
| Drain-to-source Breakdown Voltage                                                           | BV <sub>DSS</sub>    | −200  | —    | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = −2 mA                                                      |
| Gate Threshold Voltage                                                                      | V <sub>GS(th)</sub>  | −1    | —    | −2.4 | V     | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = −1 mA                                        |
| Change in V <sub>GS(th)</sub> with Temperature                                              | ΔV <sub>GS(th)</sub> | —     | —    | 4.5  | mV/°C | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = −1 mA (Note 2)                               |
| Gate Body Leakage                                                                           | I <sub>GSS</sub>     | —     | —    | −100 | nA    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V                                                      |
| Zero-gate Voltage Drain Current                                                             | I <sub>DSS</sub>     | —     | —    | −10  | μA    | V <sub>GS</sub> = 0V,<br>V <sub>DS</sub> = Maximum rating                                         |
|                                                                                             |                      | —     | —    | −1   | mA    | V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C,<br>V <sub>DS</sub> = 0.8 Maximum rating<br>(Note 2) |
| On-state Drain Current                                                                      | I <sub>D(ON)</sub>   | −0.25 | −0.7 | —    | A     | V <sub>GS</sub> = −4.5V, V <sub>DS</sub> = −25V                                                   |
|                                                                                             |                      | −0.75 | −2.1 | —    |       | V <sub>GS</sub> = −10V, V <sub>DS</sub> = −5V                                                     |
| Static Drain-to-Source On-state Resistance                                                  | R <sub>DS(ON)</sub>  | —     | 10   | 15   | Ω     | V <sub>GS</sub> = −4.5V, I <sub>D</sub> = −100 mA                                                 |
|                                                                                             |                      | —     | 8    | 12   |       | V <sub>GS</sub> = −10V, I <sub>D</sub> = −200 mA                                                  |
| Change in R <sub>DS(ON)</sub> with Temperature                                              | ΔR <sub>DS(ON)</sub> | —     | —    | 1.7  | %/°C  | V <sub>GS</sub> = −10V, I <sub>D</sub> = −200 mA<br>(Note 2)                                      |
| AC PARAMETER (Note 2)                                                                       |                      |       |      |      |       |                                                                                                   |
| Forward Transconductance                                                                    | G <sub>FS</sub>      | 100   | 250  | —    | mmho  | V <sub>DS</sub> = −25V, I <sub>D</sub> = −200 mA                                                  |
| Input Capacitance                                                                           | C <sub>ISS</sub>     | —     | 75   | 125  | pF    | V <sub>GS</sub> = 0V,<br>V <sub>DS</sub> = −25V,<br>f = 1 MHz                                     |
| Common Source Output Capacitance                                                            | C <sub>OSS</sub>     | —     | 20   | 85   |       |                                                                                                   |
| Reverse Transfer Capacitance                                                                | C <sub>RSS</sub>     | —     | 10   | 35   | ns    | V <sub>DD</sub> = −25V,<br>I <sub>D</sub> = −0.75A,<br>R <sub>GEN</sub> = 25Ω                     |
| Turn-on Delay Time                                                                          | t <sub>d(ON)</sub>   | —     | —    | 10   |       |                                                                                                   |
| Rise Time                                                                                   | t <sub>r</sub>       | —     | —    | 15   |       |                                                                                                   |
| Turn-on Delay Time                                                                          | t <sub>d(OFF)</sub>  | —     | —    | 20   |       |                                                                                                   |
| Fall Time                                                                                   | t <sub>f</sub>       | —     | —    | 15   |       |                                                                                                   |
| DIODE PARAMETER                                                                             |                      |       |      |      |       |                                                                                                   |
| Diode Forward Voltage Drop                                                                  | V <sub>SD</sub>      | —     | —    | −1.8 | V     | V <sub>GS</sub> = 0V, I <sub>SD</sub> = −0.5A (Note 1)                                            |
| Reverse Recovery Time                                                                       | t <sub>rr</sub>      | —     | 300  | —    | ns    | V <sub>GS</sub> = 0V, I <sub>SD</sub> = −0.5A (Note 2)                                            |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at  $+25^{\circ}\text{C}$ . Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

## TEMPERATURE SPECIFICATIONS

| Parameter                         | Sym.          | Min. | Typ. | Max. | Unit                 | Conditions |
|-----------------------------------|---------------|------|------|------|----------------------|------------|
| <b>TEMPERATURE RANGE</b>          |               |      |      |      |                      |            |
| Operating Ambient Temperature     | $T_A$         | -55  | —    | +150 | $^{\circ}\text{C}$   |            |
| Storage Temperature               | $T_S$         | -55  | —    | +150 | $^{\circ}\text{C}$   |            |
| <b>PACKAGE THERMAL RESISTANCE</b> |               |      |      |      |                      |            |
| 8-lead SOIC                       | $\theta_{JA}$ | —    | 101  | —    | $^{\circ}\text{C/W}$ | Note 1     |

**Note 1:** 1 oz., four-layer, 3" x 4" PCB

# TC2320

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## 2.0 PIN DESCRIPTION

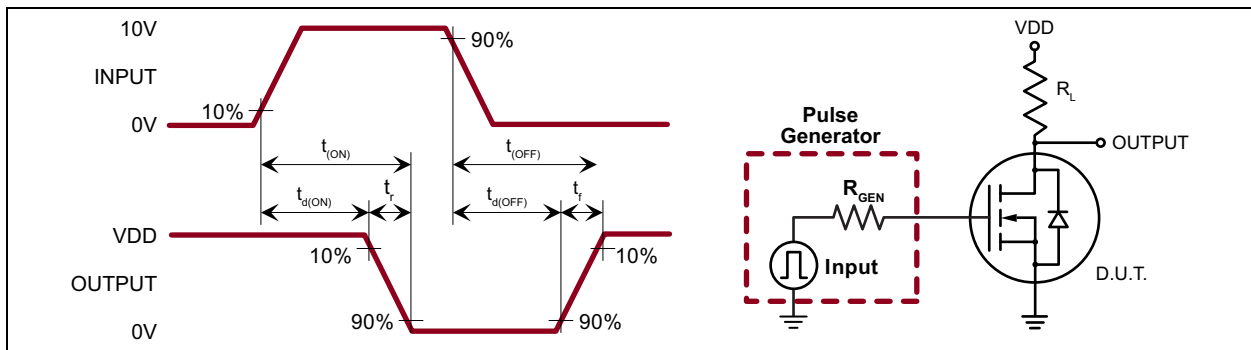
Table 2-1 shows the description of pins in TC2320.  
Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

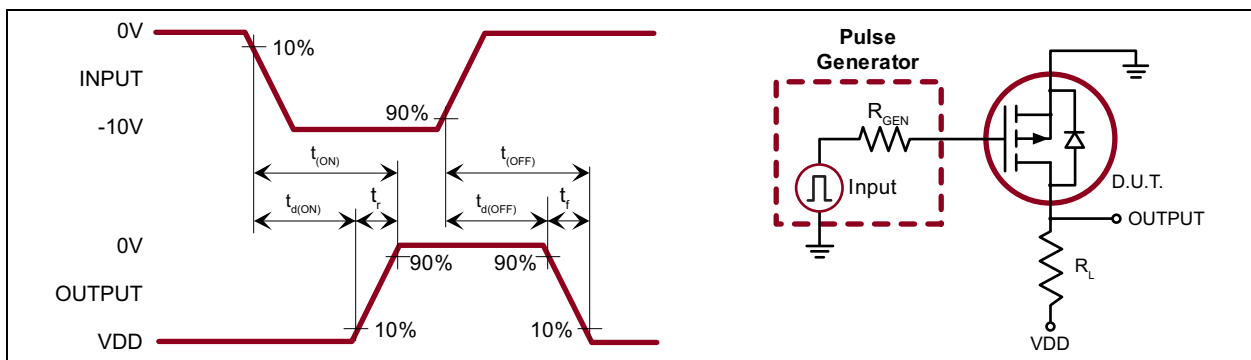
| Pin Number | Pin Name | Description      |
|------------|----------|------------------|
| 1          | SN       | Source N-channel |
| 2          | GN       | Gate N-channel   |
| 3          | SP       | Source P-channel |
| 4          | GP       | Gate P-channel   |
| 5          | DP       | Drain P-channel  |
| 6          | DP       | Drain P-channel  |
| 7          | DN       | Drain N-channel  |
| 8          | DN       | Drain N-channel  |

## 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC2320.



**FIGURE 3-1:** N-channel Switching Waveforms and Test Circuit.



**FIGURE 3-2:** P-channel Switching Waveforms and Test Circuit.

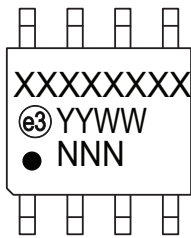
**TABLE 3-1: PRODUCT SUMMARY**

| $BV_{DSS}/BV_{DGS}$<br>(V) |           | $R_{DS(ON)}$<br>(Maximum)<br>( $\Omega$ ) |           |
|----------------------------|-----------|-------------------------------------------|-----------|
| N-Channel                  | P-Channel | N-Channel                                 | P-Channel |
| 200                        | -200      | 7                                         | 12        |

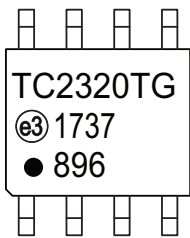
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

8-lead SOIC

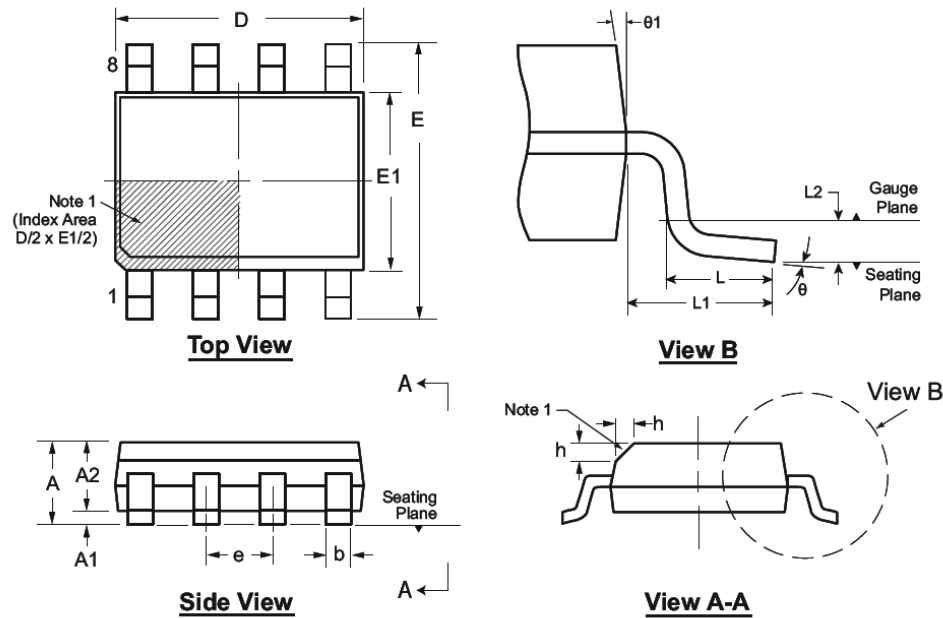


Example



|                |                                                                                                                                                                                                                                                                        |                                                                                                                  |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X                                                                                                                                                                                                                                                                 | Product Code or Customer-specific information                                                                    |
|                | Y                                                                                                                                                                                                                                                                      | Year code (last digit of calendar year)                                                                          |
|                | YY                                                                                                                                                                                                                                                                     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW                                                                                                                                                                                                                                                                     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN                                                                                                                                                                                                                                                                    | Alphanumeric traceability code                                                                                   |
|                | (e3)                                                                                                                                                                                                                                                                   | Pb-free JEDEC® designator for Matte Tin (Sn)                                                                     |
|                | *                                                                                                                                                                                                                                                                      | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo. |                                                                                                                  |

## 8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

### Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol            |     | A     | A1   | A2    | b    | D     | E     | E1    | e           | h    | L    | L1          | L2          | θ  | θ1 |
|-------------------|-----|-------|------|-------|------|-------|-------|-------|-------------|------|------|-------------|-------------|----|----|
| Dimension<br>(mm) | MIN | 1.35* | 0.10 | 1.25  | 0.31 | 4.80* | 5.80* | 3.80* | 1.27<br>BSC | 0.25 | 0.40 | 1.04<br>REF | 0.25<br>BSC | 0° | 5° |
|                   | NOM | -     | -    | -     | -    | 4.90  | 6.00  | 3.90  |             | -    | -    |             |             | -  | -  |
|                   | MAX | 1.75  | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* |             | 0.50 | 1.27 |             |             | -  | 8° |

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (June 2017)

- Converted Supertex Doc# DSFP-TC2320 to Microchip DS20005708A
- Changed packaging format
- Changed the packaging quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel
- Made minor text changes throughout the document



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