



PRELIMINARY

CY7C1001
CY7C1002

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
— $t_{AA} = 12$ ns
- **Transparent write (7C1001)**
- **CMOS for optimum speed/power**
- **Low active power**
— 910 mW
- **Low standby power**
— 275 mW
- **2.0V data retention (optional)**
— 100 μ W
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1001 and CY7C1002 are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

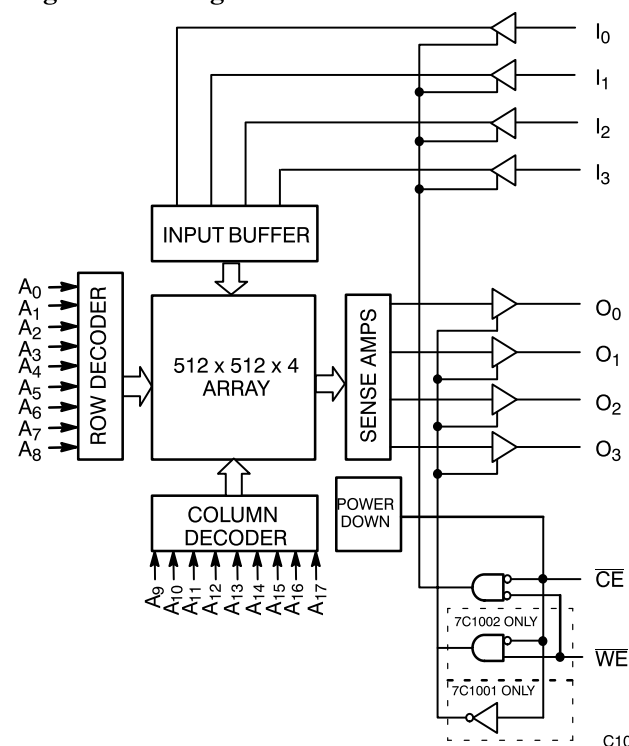
Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write en-

able ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

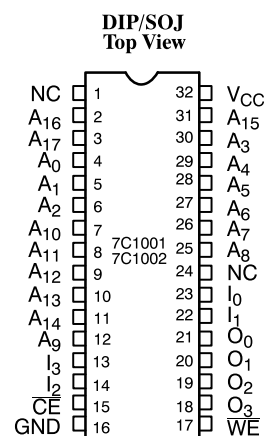
The data output pins on the CY7C1001 and the CY7C1002 are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C1002's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C1001, the output pins will carry the same data as the inputs after a specified delay.

The CY7C1001 and CY7C1002 are available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



C1001-2

C1001-1

Selection Guide

		7C1001-12 7C1002-12	7C1001-15 7C1002-15	7C1001-20 7C1002-20	7C1001-25 7C1002-25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current	Commercial	165	155	140	130
	Military		165	150	140
Maximum Standby Current (mA)	Commercial	50	40	30	30
	Military		40	30	30



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -55°C to $+125^{\circ}\text{C}$
 Supply Voltage on V_{CC} Relative to GND^[1] . -0.5V to $+7.0\text{V}$
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1001-12 7C1002-12		7C1001-15 7C1002-15		7C1001-20 7C1002-20		7C1001-25 7C1002-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_I \leq V_{CC},$ Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[4]	$V_{CC} = \text{Max.},$ $V_{OUT} = \text{GND}$		-300		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0\text{ mA},$ $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Com'l	165		155		140		130	mA
			Mil			165		150		140	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC},$ $\overline{\text{CE}} \geq V_{IH},$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL},$ $f = f_{\text{MAX}}$	Com'l	50		40		30		30	mA
			Mil			40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC},$ $\overline{\text{CE}} \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}, f=0$	Com'l	2		2		2		2	mA
			Mil			2		2		2	

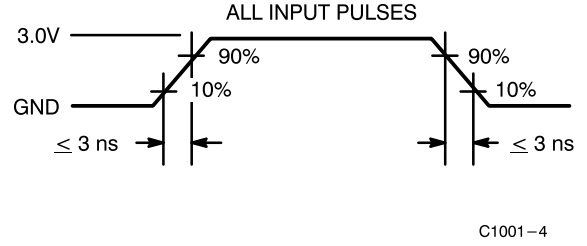
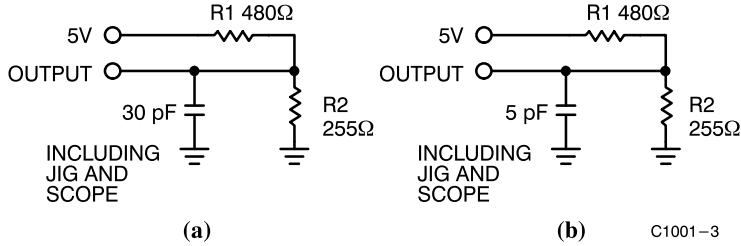
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN} : Addresses	Input Capacitance	$T_A = 25^{\circ}\text{C}, f = 1\text{ MHz},$ $V_{CC} = 5.0\text{V}$	7	pF
C_{IN} : Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

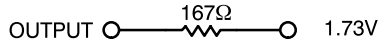
Notes:

- $V_{IL}(\text{min.}) = -2.0\text{V}$ for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[3, 6]

Parameter	Description	7C1001-12 7C1002-12		7C1001-15 7C1002-15		7C1001-20 7C1002-20		7C1001-25 7C1002-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	12		15		20		25		ns
t _{AA}	Address to Data Valid		12		15		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7]	3		3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[7, 8]		6		7		8		10	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25	ns
WRITE CYCLE ^[9]										
t _{WC}	Write Cycle Time	12		15		20		25		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[7]	3		3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7, 8]		6		7		8		10	ns
t _{DWE}	$\overline{WE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t _{DCE}	$\overline{CE}$ LOW to Data Valid (7C1001)		12		15		20		25	ns
t _{ADV}	Data Valid to Output Valid (7C1001)		12		15		20		25	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

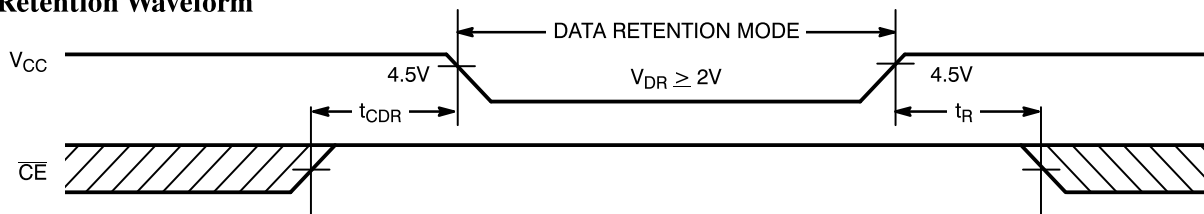
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Conditions ^[10]	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Retention Data		2.0		2.0		V
I _{CCDR}	Data Retention Current	V _{CC} = V _{DR} = 2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		50		70	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time		0		0		ns
t _R ^[5]	Operation Recovery Time		t _{RC}		t _{RC}		ns

Note:

10. No input may exceed V_{CC} + 0.5V.

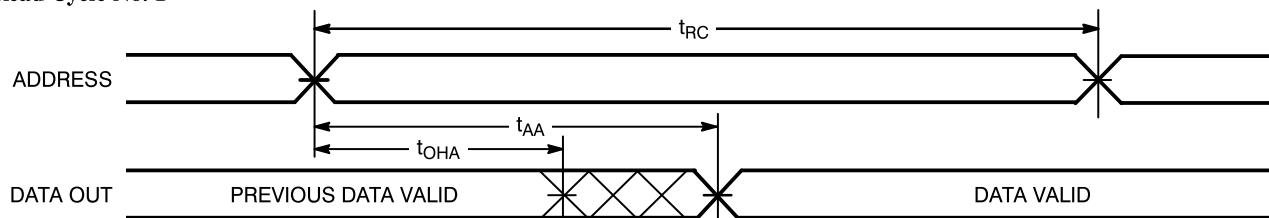
Data Retention Waveform



C1001-5

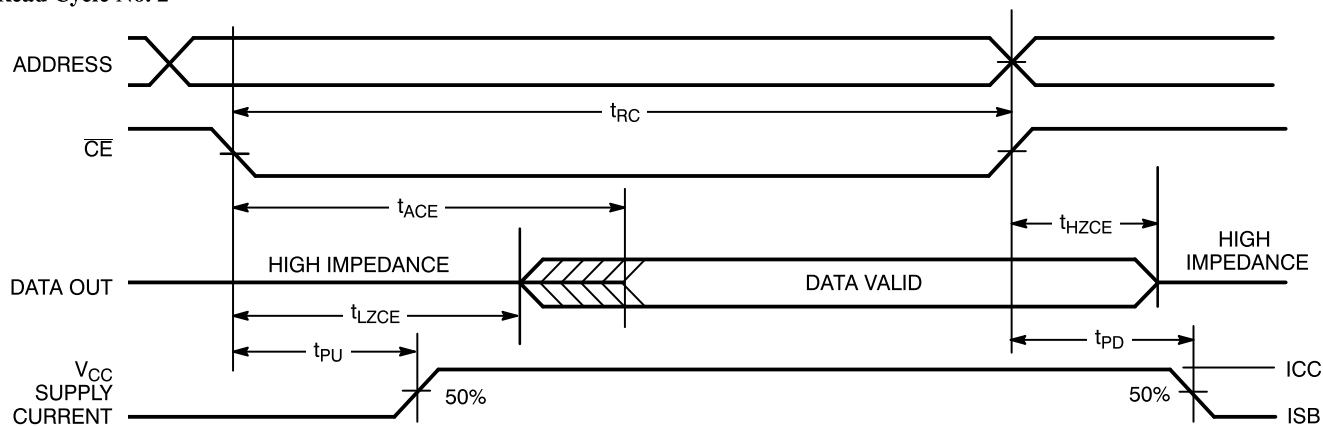
Switching Waveforms

Read Cycle No. 1^[11, 12]



C1001-6

Read Cycle No. 2^[12, 13]



C1001-7

Notes:

11. Device is continuously selected, $\overline{CE} = V_{IL}$.

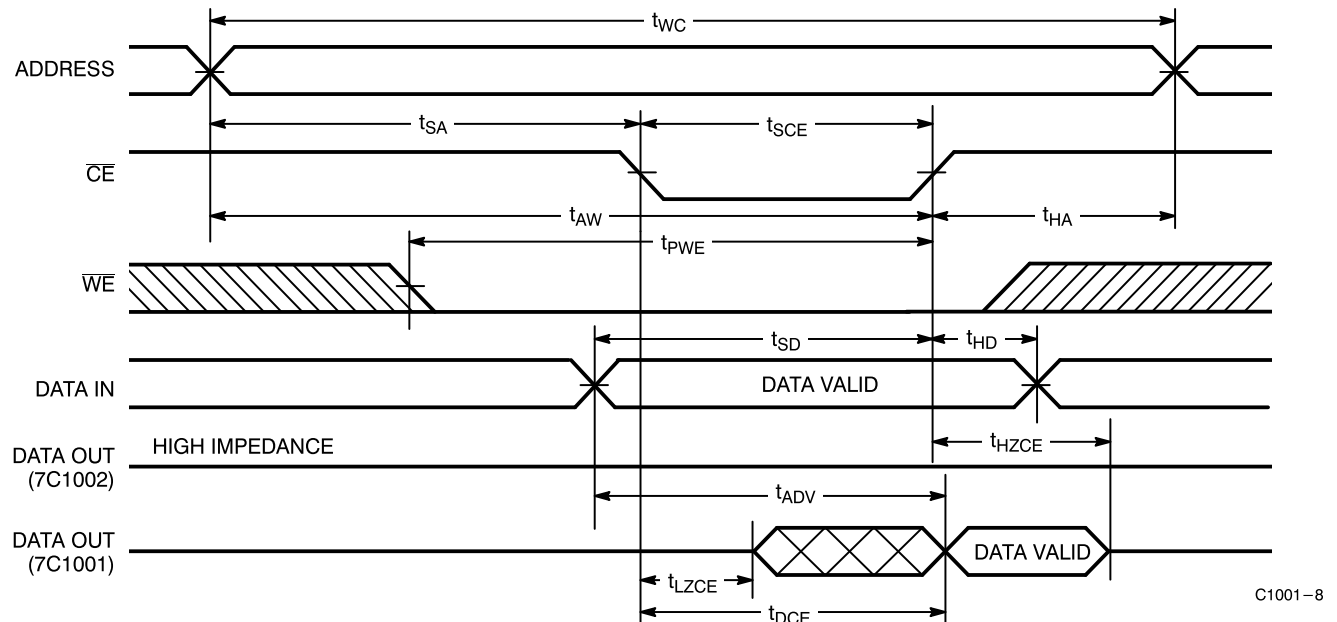
12. $\overline{WE}$ is HIGH for read cycle.

13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

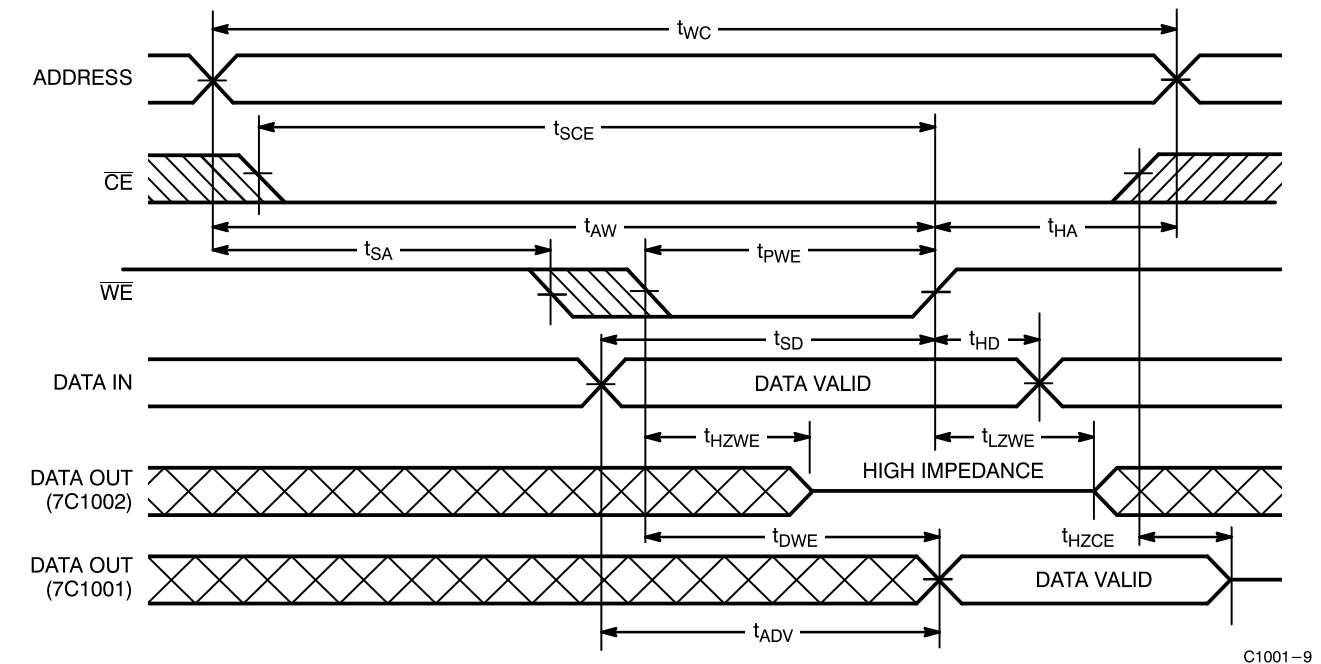


Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)^[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)^[9]



Note:

14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C1002 only).



Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C1002: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C1001: Transparent Write ^[15]	Active (I_{CC})

Note:

15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1001-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1001-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1001-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1001-25DC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1001-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1001-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1002-12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1002-15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-15DMB	D32	32-Lead (300-Mil) CerDIP	Military
20	CY7C1002-20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-20DMB	D32	32-Lead (300-Mil) CerDIP	Military
25	CY7C1002-25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1002-25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1002-25DMB	D32	32-Lead (300-Mil) CerDIP	Military

Contact factory for "L" version availability.



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{DWE} ^[16]	7, 8, 9, 10, 11
t _{ADV} ^[16]	7, 8, 9, 10, 11

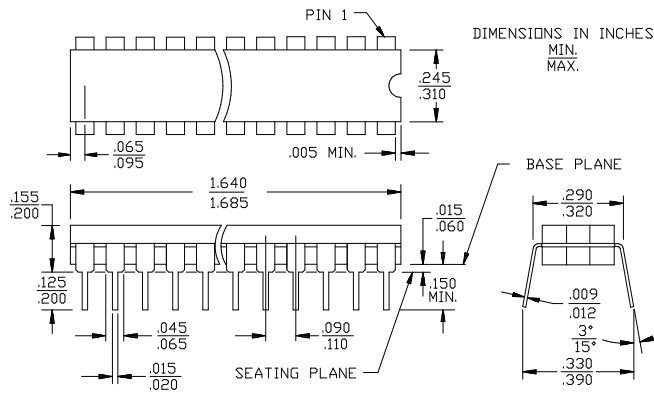
Note:

16. 7C1001 only.

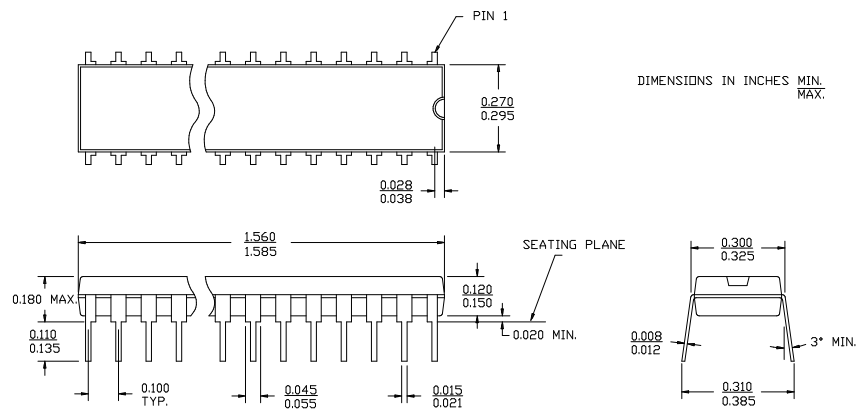
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Package Diagrams

32-Lead (300-Mil) CerDIP D32



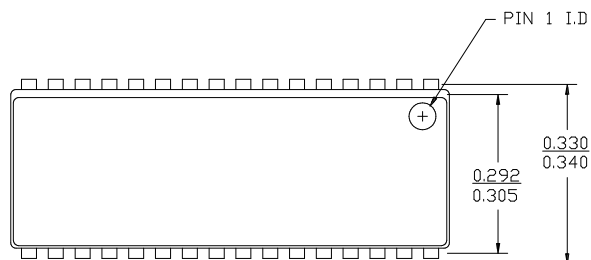
32-Lead (300-Mil) Molded DIP P31





Package Diagrams (continued)

32-Lead (300-Mil) Molded SOJ V32



DIMENSIONS IN INCHES MIN.
MAX.

