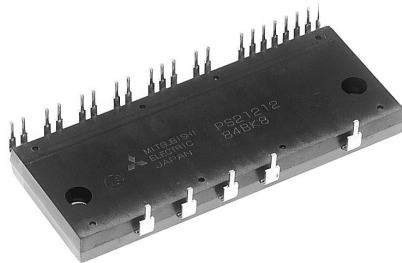


PS21212

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21212



INTEGRATED POWER FUNCTIONS

600V/5A low-loss 3rd generation IGBT inverter bridge for 3 phase DC-to-AC power conversion (Fig. 2)

Application Motor Ratings : Power : 0.2kW, sinusoidal, PWM
Frequency=15kHz
100% load current : 1.5A (rms)*
150% load current : 2.25A (rms)*,
1 minute.

*(Note) : The motor current is assumed to be sinusoidal and the peak current value is defined as : $I_o \times \sqrt{2}$

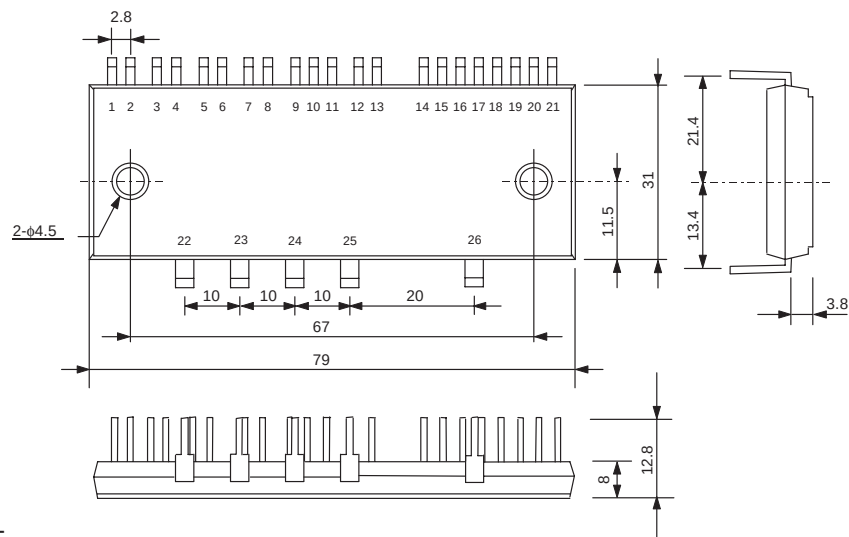
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.
Note : Bootstrap supply scheme can be applied (Fig. 2).
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC). (Fig. 3)
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side supply).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

APPLICATION

AC100V~200V three-phase inverter drive for small power (0.2 kW) motor control.

Fig. 1 PACKAGE OUTLINES



TERMINALS CODE

1. UP	4. VUFS	7. VVFB	10. VP1	13. VWFS	16. CIN	19. UN	22. P	25. W
2. VP1	5. VP	8. VVFS	11. VPC	14. VN1	17. CFO	20. VN	23. U	26. N
3. VUFB	6. VP1	9. WP	12. VWFB	15. VNC	18. Fo	21. WN	24. V	

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

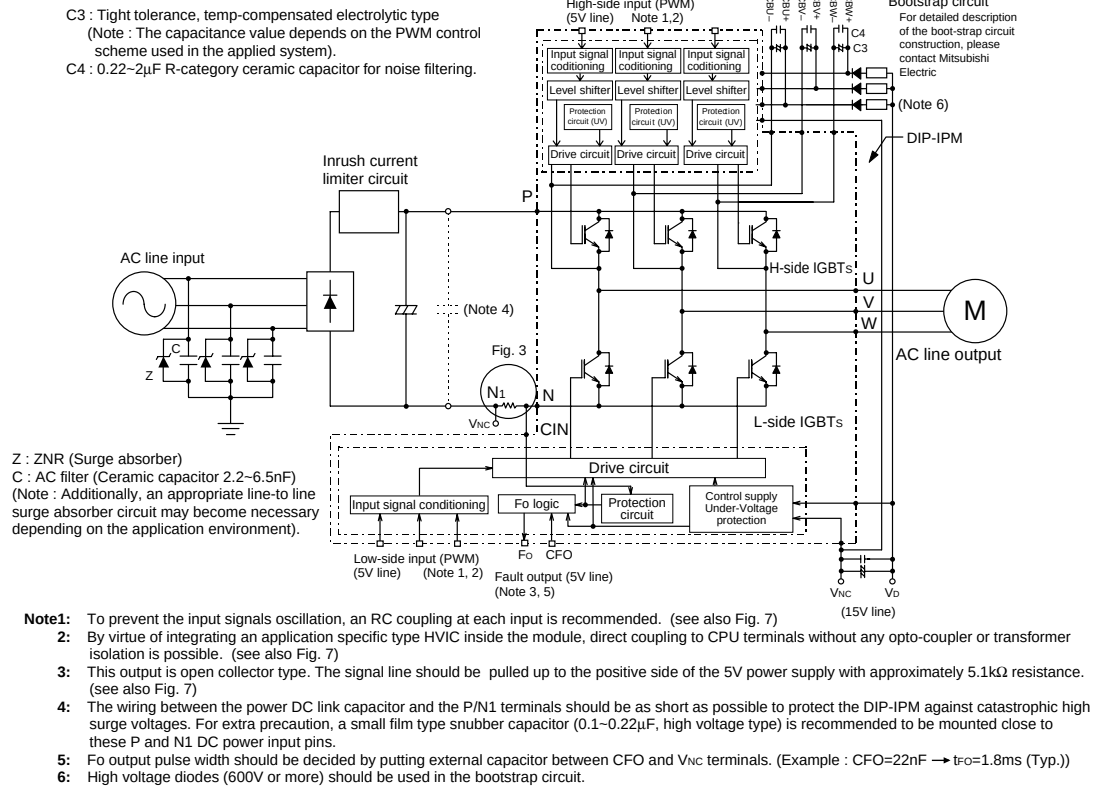
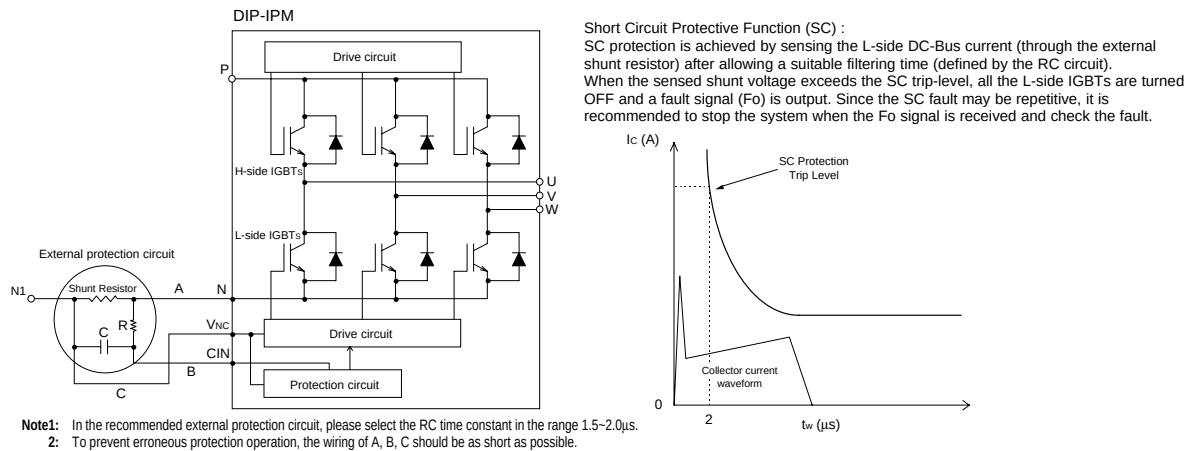


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



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MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	T _c = 25°C	5	A
±I _{CP}	Each IGBT collector current (peak)	T _c = 25°C, instantaneous value (pulse)	10	A
P _C	Collector dissipation	T _c = 25°C, per 1 chip	31	W
T _j	Junction temperature	(Note 1)	-20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ T_c ≤ 100°C) however, to insure safe operation of the DIP-IPM, the average junction temperature should be limited to T_{j(ave)} ≤ 125°C (@ T_c ≤ 100°C).

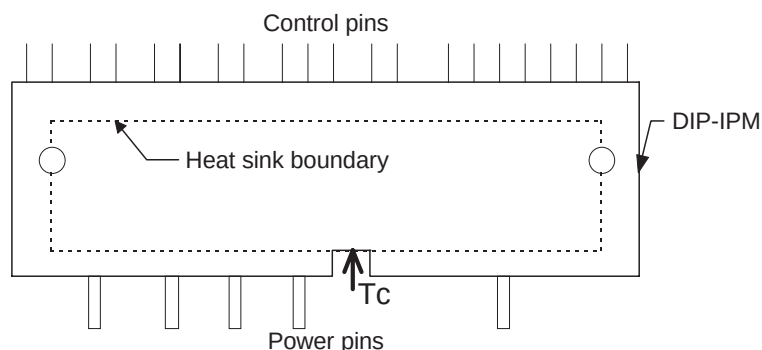
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{CIN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~+5.5	V
V _{FO}	Fault output supply voltage	Applied between Fo-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at Fo terminal	15	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Self protection supply voltage limit (short circuit protection capability)	V _D = V _{DB} = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2 μs	400	V
T _C	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V _{rms}

Note 2 : T_C MEASUREMENT POINT



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case thermal resistance	Inverter IGBT part (per 1/6 module)	—	—	4.0	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/6 module)	—	—	6.1	
R _{th(c-f)}	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.067	

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V V _{CIN} = 0V I _C = 5A, T _j = 25°C I _C = 5A, T _j = 125°C	—	2.1	—	V
V _{EC}	FWDi forward voltage	T _j = 25°C, -I _C = 5A, V _{CIN} = 5V	—	1.7	—	V
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 5A, T _j = 125°C, V _{CIN} = 5V → 0V Inductive load (upper-lower arm) Note: t _{on} , t _{off} include delay time of the internal control circuit	—	0.6	—	μs
t _{tr}			—	0.1	—	
t _{c(on)}			—	0.2	—	
t _{off}			—	1.1	—	
t _{c(off)}			—	0.35	—	
I _{CES}	Collector-emitter cut-off current	V _{CE} = V _{CES} T _j = 25°C T _j = 125°C	—	—	1.0 10	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _D	Control supply voltage	Applied between V _{P1} -V _{PC} , V _{N1} -V _{NC}		13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}		13.5	15.0	16.5	V
I _D	Circuit current	V _D = V _{DB} = 15V, input = OFF	V _{P1} -V _{PC} , V _{N1} -V _{NC}	—	4.25	8.50	mA
			V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	—	0.50	1.00	mA
		V _D = V _{DB} = 15V, input = ON	V _{P1} -V _{PC} , V _{N1} -V _{NC}	—	4.95	9.70	mA
			V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	—	0.50	1.00	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O circuit : 10kΩ to 5V pull-up		4.9	—	—	V
V _{FOL}		V _{SC} = 1V, F _O circuit : 10kΩ to 5V pull-up		—	1.0	2.0	V
V _{FOsat}		V _{SC} = 1V, I _{FO} = 15mA		0.8	1.2	1.8	V
f _{PWM}	PWM input frequency	T _C ≤ 100°C, T _j ≤ 125°C		—	15	—	kHz
t _{dead}	Allowable deadtime	Relates to corresponding input signal for blocking arm shoot-through. –20°C ≤ T _C ≤ 100°C		3.0	—	—	μs
V _{SC(ref)}	Short circuit trip level	T _j = 25°C, V _D = 15°C (Note 2)		0.45	0.5	0.55	V
UV _{DBt}	Supply circuit under-voltage protection	T _j ≤ 125°C	Trip level	10.0	—	12.0	V
UV _{DBr}			Reset level	10.5	—	12.5	V
UV _{Dt}			Trip level	10.3	—	12.5	V
UV _{Dr}			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width (Note 3)	C _{FO} = 22nF (connected between C _{FO} –V _{NC})		1.0	1.8	—	ms
V _{th(on)}	ON threshold voltage	H-side	Applied between:	0.8	1.4	2.0	V
V _{th(off)}	OFF threshold voltage		U _P , V _P , W _P -V _{PC}	2.5	3.0	4.0	
V _{th(on)}	ON threshold voltage	L-side	Applied between:	0.8	1.4	2.0	V
V _{th(off)}	OFF threshold voltage		U _N , V _N , W _N -V _{NC}	2.5	3.0	4.0	

Note 2 : Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 8.5 A.

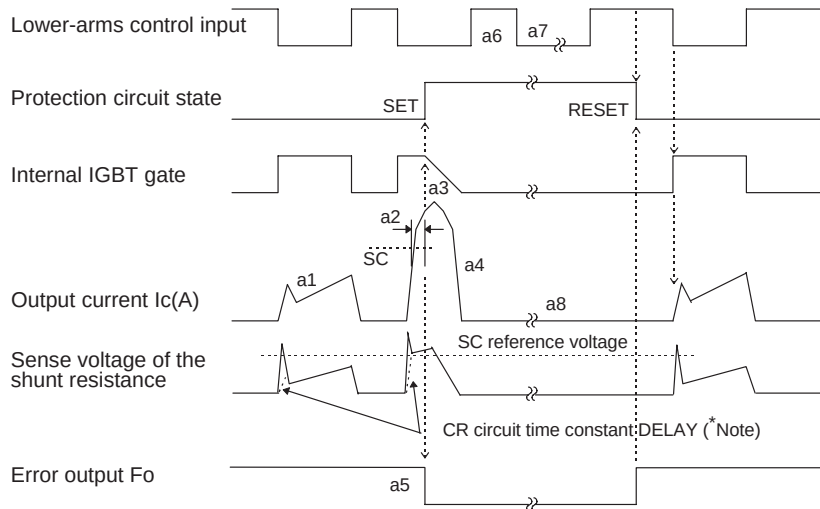
3 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : C_{FO} = 12.2 × 10⁻⁶ × t_{FO} [F].

Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

[A] Short-Circuit Protection (Lower-arms only)

(For the external shunt resistance and CR connection, please refer to Fig. 3.)

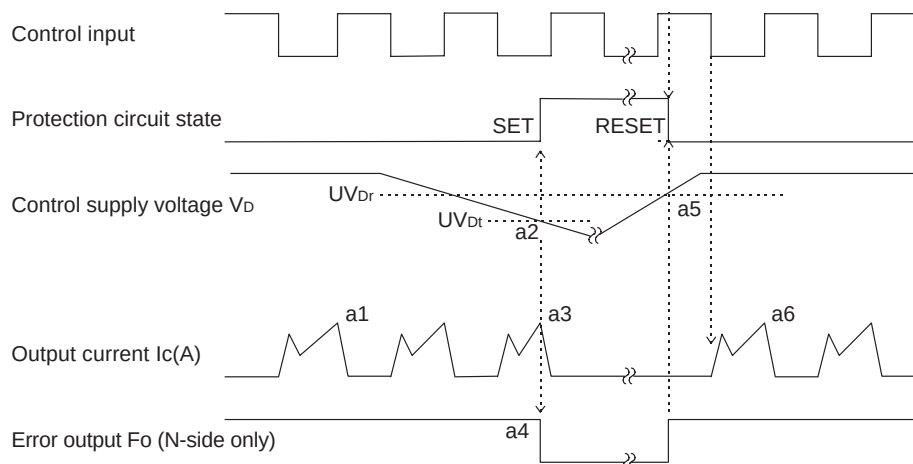
- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. Hard IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "H" : IGBT OFF state.
- a7. Input "L" : IGBT ON state, but during the Fo active signal the IGBT doesn't turn ON.
- a8. IGBT OFF state.



Note : The CR time constant safe guards against erroneous SC fault signals resulting from di/dt generated voltages when the IGBT turns ON.
The optimum setting for the CR circuit time constant is 1.5~2.0 μ s.

[B] Under-Voltage Protection (N-side, UV_D)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Under voltage trip (UV_{Dt}).
- a3. IGBT OFF inspite of control input condition.
- a4. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a5. Under voltage reset (UV_{Dr}).
- a6. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (P-side, UV_{DB})

- a1. Control supply voltage rises : After the voltage level reaches UV_{DBr} , the circuits start to operate when the next input is applied.
- a2. Normal operation : IGBT ON and carrying current.
- a3. Under voltage trip (UV_{DBt}).
- a4. IGBT OFF inspite of control input condition, but there is no Fo signal output.
- a5. Under-voltage reset (UV_{DBr}).
- a6. Normal operation : IGBT ON and carrying current.

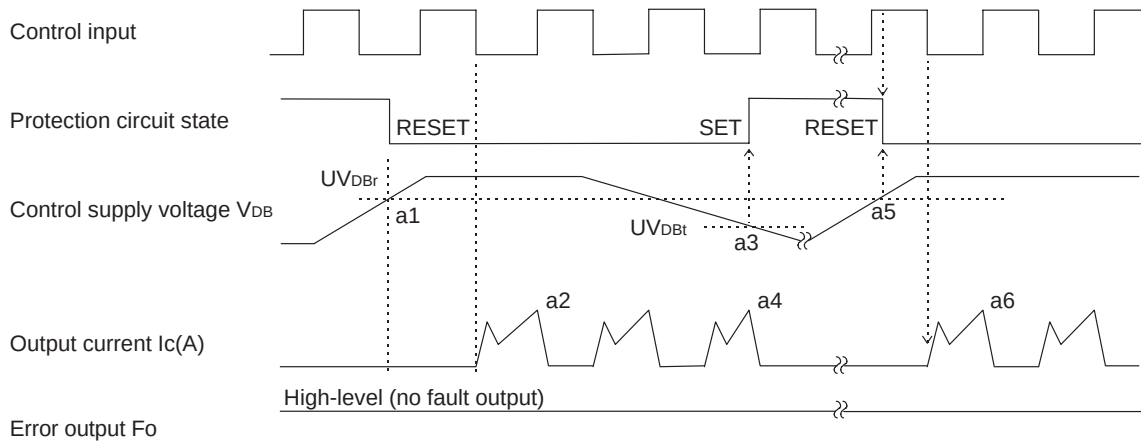
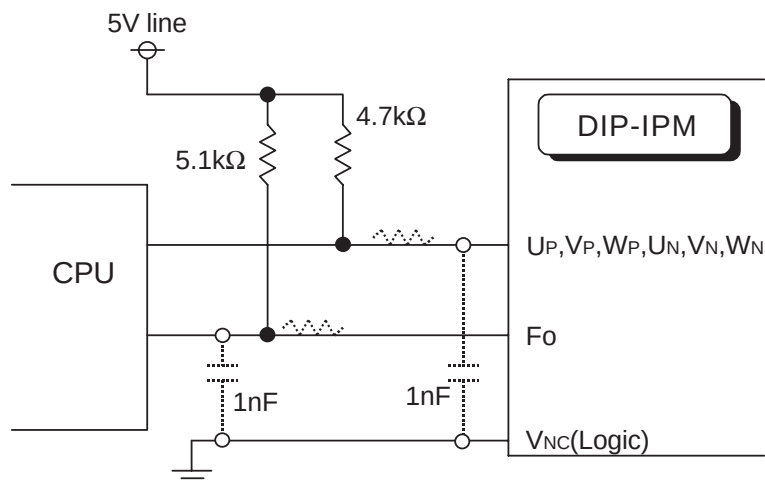
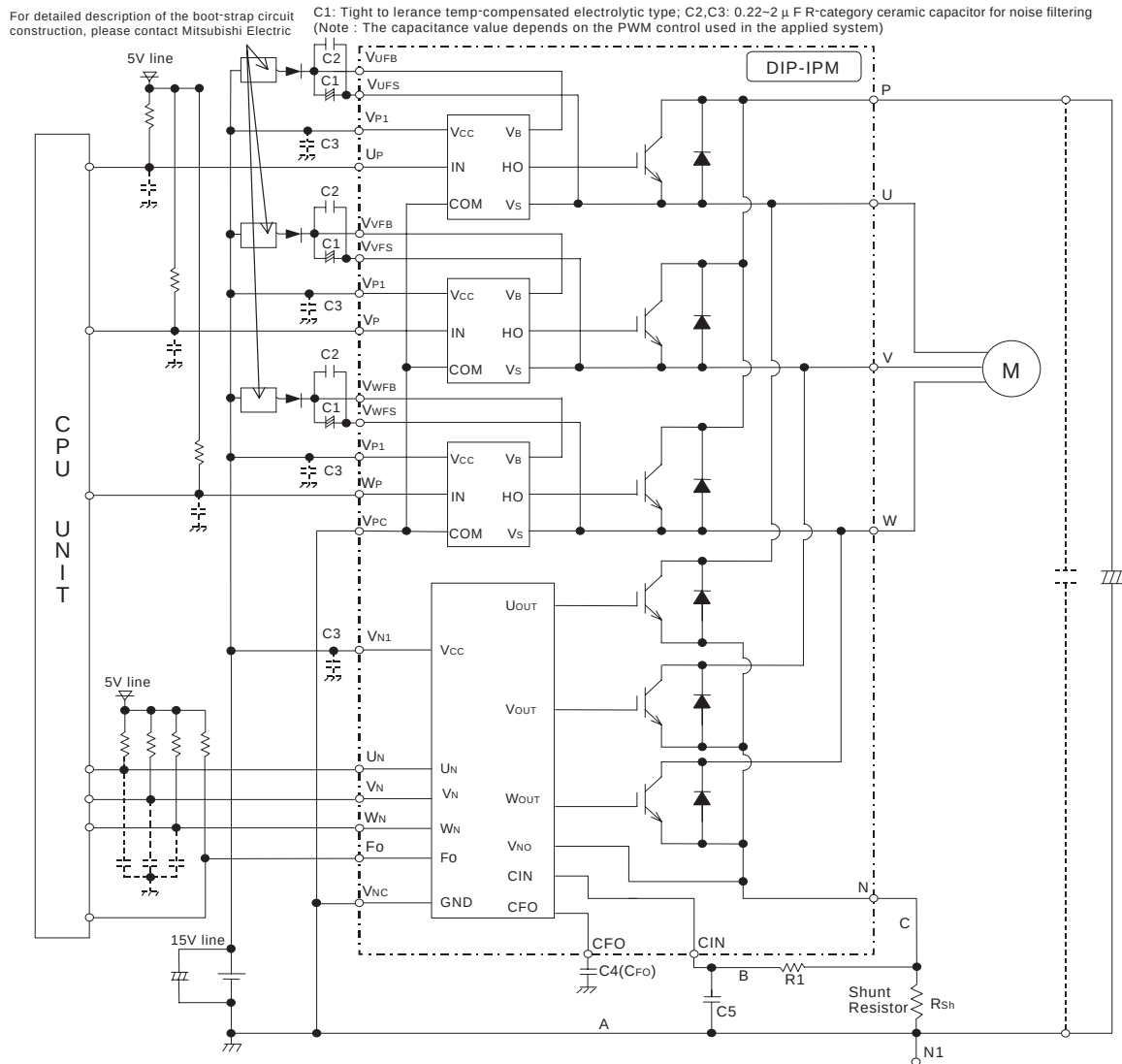


Fig. 7 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedances of the application's printed circuit board.

Fig. 8 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



- Note 1:** To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible. (Less than 2cm)
- 2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
- 3:** Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1k Ω resistance.
- 4:** Fo output pulse width should be decided by connecting an external capacitor between CFO and Vnc terminals (Cfo). (Example: Cfo = 22 nF $\rightarrow$ tfo = 1.8 ms (typ.))
- 5:** Each input signal line should be pulled up to the 5V power supply with approximately 4.7k Ω resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2 μ F by-pass capacitor should be used across each power supply connection terminals.
- 6:** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.
- 7:** In the recommended protection circuit, please select the R1C5 time constant in the range 1.5~2 μ s.
- 8:** Each capacitor should be put as nearby the pins of the DIP-IPM as possible.
- 9:** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22 μ F snubber capacitor between the P&N1 pins is recommended.