LM8335 General Purpose Output Expander with MIPI® RFFE Host Interface

Check for Samples: LM8335

FEATURES

- **MIPI RFFE Interface Version 1.10 Compliant**
- **Supports Output Expansion**
- **Host Interface Address Select Pin:**
  - **ADR=GND, USID[3:0]=0001**
  - **ADR=VDD, USID[3:0]=1001**
- **Pin-Configurable Initial State: VIO**
  - **CFG=GND, GPO High-z, with Weak Internal Pull-Down Resistor Enabled; GPO_OUT_DATA is Unmasked**
  - **CFG=VDD, GPO High-z, with Weak Internal Pull-Down Resistor Enabled; GPO_OUT_DATA is Masked**
- **Three Sources for Chip Reset:**
  - **VIO Input Pin**
  - **POR**
  - **Software-Commanded Reset**

APPLICATIONS:

- **Smart Handheld Devices**
- **RF Transceiver Applications**

KEY SPECIFICATIONS

- **1.8 ± 0.15V MIPI RFFE Operation (VIO)**
- **1.8 ± 0.15V Core Supply (V_{DD})**
- **1.65 to 3.6V GPO Supply (V_{DDIO})**
- **Low Standby and Active Current**
- **On-Chip Power-On Reset (POR)**
- **−30 to +85°C Ambient Temperature Range**
- **16-Bump DSBGA Package**
  - **1.965 mm x 1.965 mm x 0.6 mm, 0.5 mm Pitch (Nominal)**

DESCRIPTION

The LM8335 General Purpose Output Expander is a dedicated device to provide flexible and general purpose, host programmable output expansion functions. This device communicates with a host processor through a MIPI® RFFE Interface (Mobile Industry Processor Interface RF Front-End).

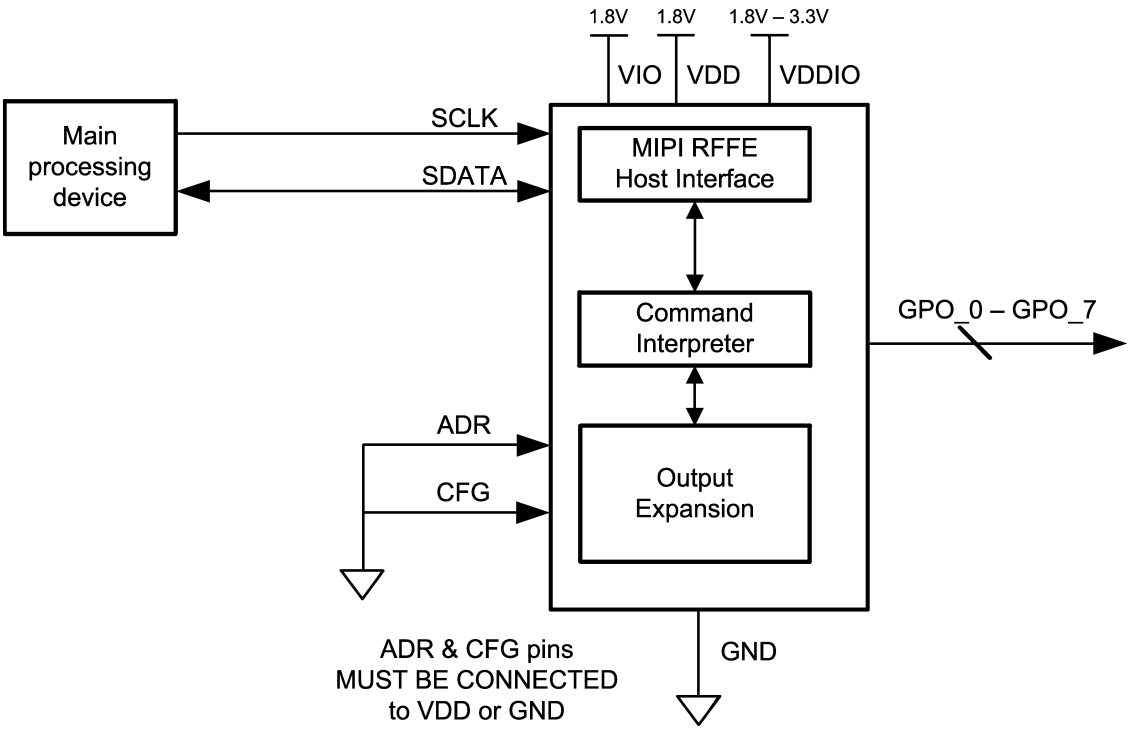
Eight general purpose outputs (GPO) can be configured by the host controller as drive high/low/high-z. Weak pull-ups (PU) or weak pull-downs (PD) can be enabled.

Upon power-on, the LM8335 default configuration is for all GPO to be set based on the state of the CFG pin.

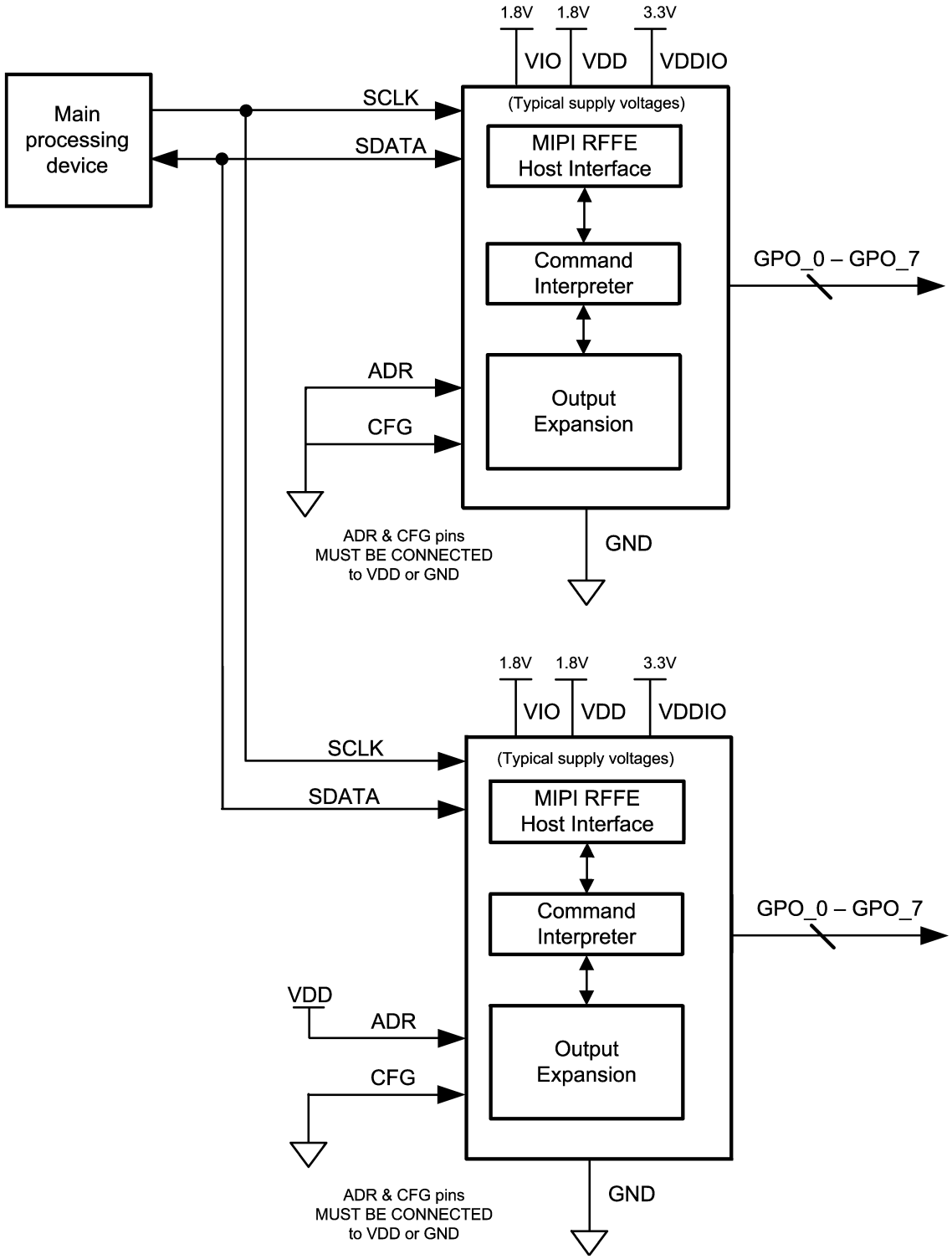
After startup, any changes to the default configuration must be sent from the host via the MIPI RFFE host interface..

The LM8335 is available in a 16-bump lead-free DSBGA package of size 1.965 mm x 1.965 mm x 0.6 mm (0.5 mm pitch).

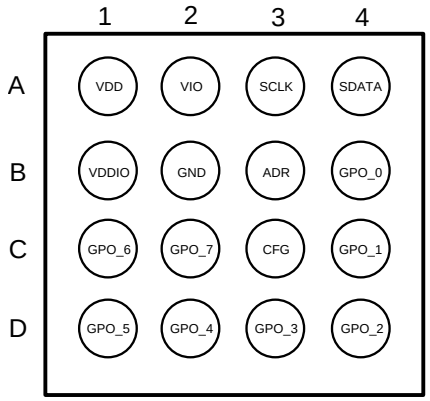
Single RFFE Slave Application Block Diagram



Dual RFFE Slave Application Block Diagram



Connection Diagram and Package Mark Information



Top View

Figure 1. 16-Bump DSBGA Pinout
1.965mm x 1.965mm x 0.6mm (nom), 0.5mm pitch
See Package Number YZR0016

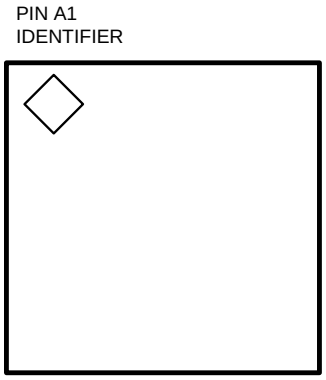


Figure 2. A1 Pin Identifier

PIN DESCRIPTIONS

Pin Number	Name	Description
8	GPO_0 through GPO_7	General purpose outputs
1	SCLK	RFFE clock input
1	SDATA	RFFE data input
1	ADR	RFFE chip address input
		ADR = VDD: USID[3:0] = b1001
		ADR = GND: USID[3:0] = b0001
1	CFG	Initial configuration select
		CFG = VDD: GPO high-z with weak internal pull-down resistor enabled, GPO_OUT_DATA masked
		CFG = GND: GPO high-z, with weak internal pull-down resistor enabled, GPO_OUT_DATA unmasked
1	VIO	MIPI RFFE VIO (1.8V ± 0.15V)
1	VDD	Core supply VDD (1.8V ± 0.15V)
1	VDDIO	GPO supply VDDIO (1.65V to 3.6V)
1	GND	Ground

ADR INPUT PIN

The state of the ADR pin determines the MIPI RFFE USID as described in the table above. This enables two devices to be used on the same RFFE bus thereby doubling the number of GPOs available in the system (see Dual RFFE Slave Application Block Diagram).

DEFAULT GPO_x PIN CONFIGURATION

Upon power-on all GPOs will default based on the state of the CFG pin.

CFG INPUT PIN = GND

The CFG0 mode is an automatic initialization mode. It allows the host to not have to first configure any registers before writing the GPO_OUT_DATA register to set the GPOs high or low. In this mode, the GPOs will default as high-z with weak pull-down resistors enabled and the GPO_OUT_DATA will be unmasked. When the host writes the GPO_OUT_DATA register, the weak pull-down resistor will be disabled. The output driver will immediately be enabled and will drive high or low based on the value written to the GPO_OUT_DATA register. In configuration mode CFG0 the GPO data mask function is available but the GPO pull resistor, and high-z functions cannot be changed. Writing to the GPO_PULL_DIR, GPO_PULL_ENABLE, and GPO_OUT_HIGH_CFG registers will have no effect. If control of the GPO pull resistor or output configuration is required then the CFG1 mode must be used.

CFG INPUT PIN = VDD

The CFG1 mode is a more general purpose mode where the outputs must be configured during initialization prior to use. In this mode, the GPOs will default as high-z with internal pull-down resistors enabled and GPO_OUT_DATA will be masked. During initialization, the host must first write to the GPO_OUT_DATA register (Note: this will transition all of the GPOs from high-z with internal pull-down to Full-Buffer driven low with internal pull-down regardless of the value written to the GPO_OUT_DATA register). The host must then write to the GPO_PULL_DIR, GPO_PULL_ENABLE, & GPO_OUT_HIGH_CFG registers to configure each GPO into the desired output configuration. Once that is complete, the host then writes the GPO_DATA_MASK and GPO_OUT_DATA registers to set the GPO outputs in the desired state. Refer to Figure 8.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

RFFE Supply Voltage (VIO)	−0.3V to 2.2V
Core Supply Voltage (VDD)	−0.3V to 2.2V
GPO Supply Voltage (VDDIO)	−0.3V to 4.0V
DC Input Voltage for SCLK & SDATA pins	−0.3V to (VIO+0.3V)
DC Input Voltage for ADR & CFG pins	−0.3V to (V_{DD}+0.3V)
DC Output Voltage for GPO pins	−0.3V to (V_{DDIO}+0.3V)
Storage Temperature Range	−40°C to +125° C
Operating Ambient Temperature (TA)	−0°C to +85°C
Lead Temperature (TL) (Soldering, 10 sec.)	260°C
ESD Rating (CZAP=120 pF, RZAP=1500Ω)	
Human Body Model (3)	1000V
Charge Device Model:	250V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

OPERATING RATINGS

	Min	Max	Unit
RFFE Supply Voltage (VIO)	1.65	1.95	V
RFFE Supply Noise (VIO)		25	mVpp
Core Supply Voltage (V_{DD})	1.65	1.95	V
Core Supply Noise (V_{DD})		25	mVpp
GPO Supply Voltage (V_{DDIO})	1.65	3.60	V
GPO Supply Noise (V_{DDIO})		50	mVpp

DC ELECTRICAL CHARACTERISTICS: GENERAL (ADR, CFG)(1)(2)

T_A: −30°C to +85°C, VIO = 1.8V ± 0.15V, V_{DD} = 1.8V ± 0.15V, V_{DDIO} = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Minimim high-level input voltage (ADR, CFG)		0.7 * V_{DD}		V_{DD}+ 0.2	V
V_{IL}	Maximum low-level input voltage (ADR, CFG)		−0.2		0.3 * V_{DD}	
I_{IH}	Logic high-level input current (ADR, CFG)	V_{IN} = V_{DD}			2	µA
I_{IL}	Logic low-level input current (ADR, CFG)	V_{IN} = GND	−2			

(1) All voltages are with respect to the GND pin.
(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V_{DD} = 1.8V, V_{DDIO} = 3.3V, VIO = 1.8V, T_A = +25°C.

DC ELECTRICAL CHARACTERISTICS: GPO (GPO_X, VDD, VDDIO)[1][2]

T_A: −30°C to +85°C, VIO = 1.8V ± 0.15V, V_{DD} = 1.8V ± 0.15V; V_{DDIO} = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Minimum high-level output voltage	I_{OH} = −12 mA (V_{DDIO} = 3.3V ± 0.3V)	0.7 * V_{DDIO}			V
		I_{OH} = −4 mA (V_{DDIO} = 1.8V ± 0.15V)				
		I_{OH} = −10 µA	V_{DDIO} − 0.2			
V_{OL}	Maximum low-level output voltage	I_{OL} = 12 mA (V_{DDIO} = 3.3V ± 0.3V)			0.4	V
		I_{OL} = 4 mA (V_{DDIO} = 1.8V ± 0.15V)			0.4	
		I_{OL} = 10 µA			0.2	
I_{OH}	Logic high-level output current	(V_{DDIO} = 3.3V ± 0.3V)	−12			mA
		(V_{DDIO} = 1.8V ± 0.15V)	−4			
I_{OL}	Logic low-level output current	(V_{DDIO} = 3.3V ± 0.3V)			12	mA
		(V_{DDIO} = 1.8V ± 0.15V)			4	
I_{OZ}	High-Z leakage current	0 < V_{PIN} < V_{DDIO}	−2		2	µA
I_{PU}	Pull-Up current	(V_{DDIO} = 3.3V ± 0.3V)	−60		−200	µA
		(V_{DDIO} = 1.8V ± 0.15V)	−9		-60	
I_{PD}	Pull-Down current	(V_{DDIO} = 3.3V ± 0.3V)	60		200	µA
		(V_{DDIO} = 1.8V ± 0.15V)	9		60	
I_{STBY}	V_{DD} supply standby current	T_A = 25°C, VIO = 1.8V, V_{DD} = 1.8V, V_{DDIO} = 3.3V, GPO_X = high-z, PU & PD disabled SCLK = Low			2.5	µA
I_{STBYIO}	V_{DDIO} supply standby current				2.5	
I_{VDD}	V_{DD} supply current	T_A = 25°C, V_{DD} = 1.8V		225	400	µA
I_{VDDIO}	V_{DDIO} supply current	T_A = 25°C V_{DDIO} = 3.3V		200	450	

(1) All voltages are with respect to the GND pin.
(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V_{DD} = 1.8V, V_{DDIO} = 3.3V, VIO = 1.8V, T_A = +25°C.

DC ELECTRICAL CHARACTERISTICS: RFFE (SCLK, SDATA, VIO)[1][2]

T_A: −30°C to +85°C, VIO = 1.8V ± 0.15V, V_{DD} = 1.8V ± 0.15V; V_{DDIO} = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input pin capacitance (SCLK, SDATA)[2]				2.5	pF
V_{TP}	Positive edge threshold voltage (SCLK, SDATA)		0.4 * VIO		0.7 * VIO	V
V_{TN}	Negative edge threshold voltage (SCLK, SDATA)		0.3 * VIO		0.6 * VIO	
V_{HYST}	Input hysteresis voltage (SDATA)		0.1 * VIO		0.4 * VIO	
V_{IORST}	RFFE I/O voltage reset voltage level	VIO toggled low			0.2	
I_{INVIO}	Input current (VIO)	0 < VIO < 0.2V	−1		1	µA
I_{IN}	Input current (SCLK, SDATA)	VIO = Max, 0.2 * VIO < V_{IN} < 0.8 * VIO	−1		1	
I_{VIO}	VIO supply input current	VIO = 1.8, RFFE write only mode			100	

(1) All voltages are with respect to the GND pin.
(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V_{DD} = 1.8V, V_{DDIO} = 3.3V, VIO = 1.8V, T_A = +25°C.

AC ELECTRICAL CHARACTERISTICS: INTERNAL POR, VIO, GPO_X, SCLK(1)(2)

T_A: −30°C to +85°C, VIO = 1.8V ± 0.15V, V_{DD} = 1.8V ± 0.15V; V_{DDIO} = 3.3V ± 0.3V (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PORC1}	VDD POR reset complete	V_{DD} ramp rate = 100 µS			1	mS
t_{PORC2}	VDDIO POR reset complete	V_{DDIO} ramp rate = 100 µS			1	
t_{READY}	VIO input signal reset delay time	VIO = 1.65V, SCLK, SDATA = Low, t_{PORC1}, t_{PORC2} = complete			120	nS
f_{SCLK}	SCLK frequency		0.032		26	MHz
t_D	GPO_x output delay time	V_{DDIO} = 1.8V ± 0.15V, C_{LOAD} = 10 pf			25	nS

(1) All voltages are with respect to the GND pin.
(2) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not specified, but do represent the most likely norm. Unless otherwise specified conditions for typical specifications are: V_{DD} = 1.8V, V_{DDIO} = 3.3V, VIO = 1.8V, T_A = +25°C.

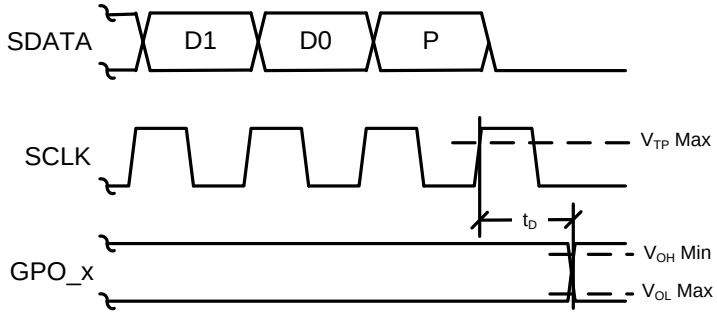


Figure 3. GPO Delay Timing

MIPI RFFE INTERFACE

The LM8335 provides RFFE compatible slave access to the device specific and RFFE defined registers on a single master bidirectional serial bus interface. The LM8335 uses the three interface signals SCLK, SDATA, and VIO as defined in MIPI RFFE Version 1.10 – 26 July 2011. The VIO voltage supply provides power to the LM8335 RFFE Interface and doubles as an asynchronous enable and reset. Whenever VIO is low the SCLK and SDATA lines must be held low. When the VIO voltage is applied, the LM8335 enables the slave interface and resets the user defined slave registers to the default settings. The LM8335 enters the power down mode via the asynchronous VIO signal. The LM8335 does not support read access.

The LM8335 contains fewer than 28 user defined registers but supports the Extended Register Write Command to allow a burst write of configuration registers during initialization. Any write outside of the range from 0x00 to 0x1F will have no effect on device operation.

The LM8335 recognizes the broadcast Slave Identifier (SID) of 0000b and is configured internally with a Unique Slave Identifier (USID) and a Group Slave Identifier (GSID). The USID is set based on the state of the ADR pin and the GSID is set to 0000b. The USID may be reprogrammed via the RFFE Interface by performing the Register Write USID Command Sequence.

The LM8335 supports only the 1.8V VIO supply levels. The LM8335 utilizes a power-detect reset circuit that resets the RFFE interface and internal registers when VIO is removed.

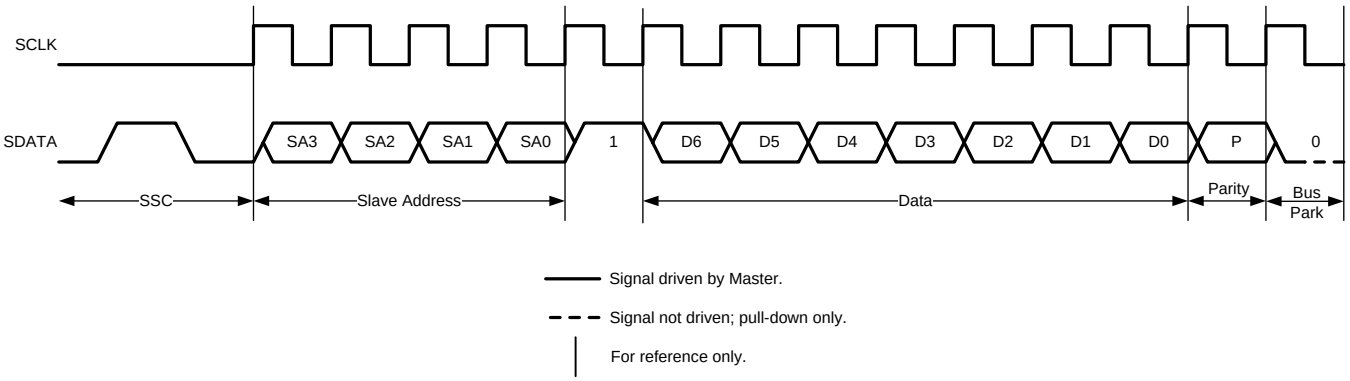


Figure 4. Register 0 Write Command Sequence

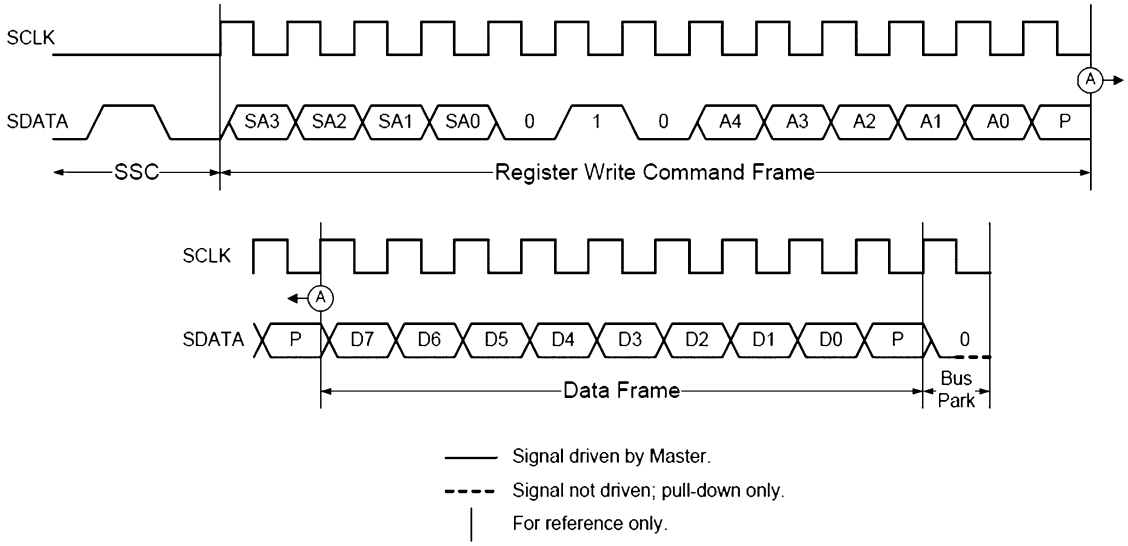


Figure 5. Register Write Command Sequence

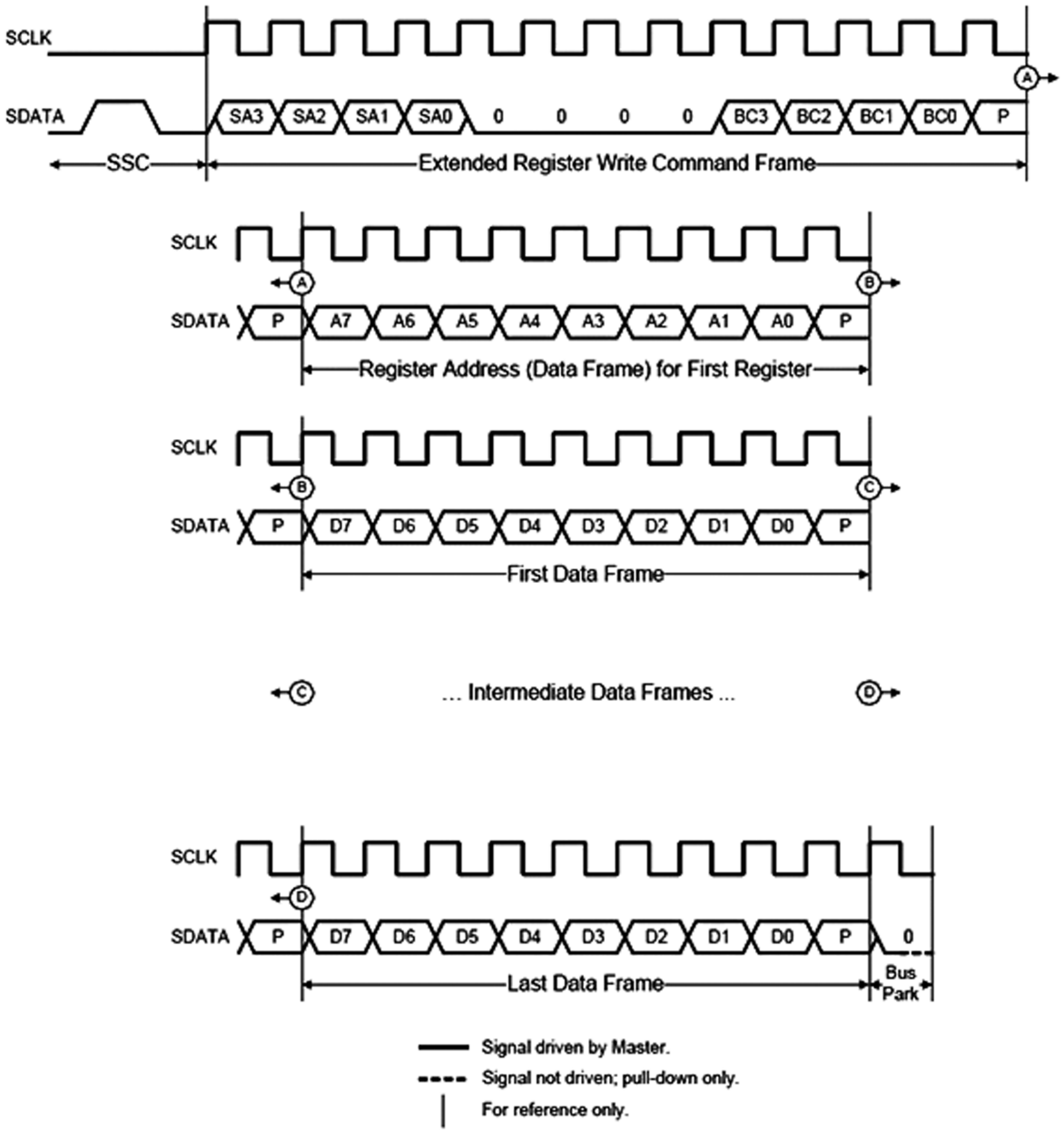


Figure 6. Extended Register Write Command Sequence

INTERNAL POR OPERATION

There are two internal POR circuits: one on the VDD supply and one on the VDDIO supply that initialize the LM8335 when power is applied. The duration of the reset is an RC delay which is based on the ramp rate and not a threshold voltage of the VDD/VDDIO supply. VIO can be activated as soon as VDD and VDDIO have reached their minimum respective voltage levels however the LM8335 may still be in reset due to the internal POR timing. When VIO is asserted after VDD and VDDIO t_{PORC} Max, the device reset will be released based on the VIO t_{READY} timing.

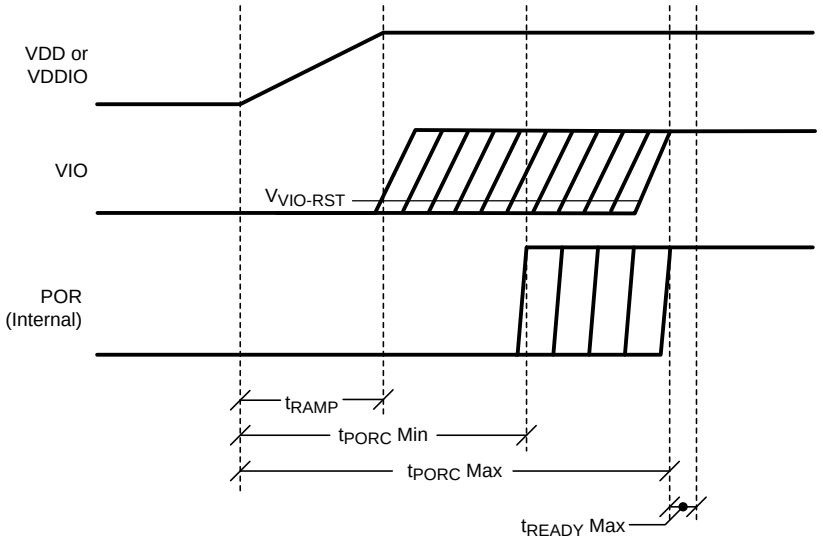


Figure 7. Internal VDD or VDDIO POR Timing

Register Information

Table 1. Register Listing

Register Name	Addr	Bit	Default	Description
CNTL_REG	0x00	7:0	0x00	Software reset register Bit 0 = 0, no effect Bit 0 = 1, reset registers to default values (self-clearing)
GPO_PULL_DIR	0x01	7:0	0x00	GPO pin pull resistor direction 0 = pull-down 1 = pull-up Note: When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled after the first write to the GPO_OUT_DATA register.
GPO_PULL_ENABLE	0x02	0xFF	0xFF	GPO pin internal pull resistor enable 0 = disabled 1 = enabled Note: GPO_PULL_DIR register selects if the resistor is a pull-up or a pull-down. When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled after the first write to the GPO_OUT_DATA register.
GPO_OUT_HIGH_CFG	0x03	7:0	0xFF	GPO output high state (full buffer or high-z). 0 = full buffer 1 = high-z (open-drain behavior) Note: When CFG = GND, writing to this register has no effect. The pull-down resistor will be disabled, and all GPO outputs will be in the actively driven state (not high-z) after the first write to the GPO_OUT_DATA register.

Table 1. Register Listing (continued)

Register Name	Addr	Bit	Default	Description
GPO_OUT_MASK	0x04	7:0	0xFF (CFG=0) or 0x00 (CFG=1)	GPO output data mask 0 = GPO_OUT_DATA masked 1 = GPO_OUT_DATA unmasked Note: Only the GPO_OUT_DATA register write is affected by the GPO_OUT_MASK register. When the GPO_OUT_MASK bit is set low (masked), writing to GPO_OUT_DATA register will leave the pin state unchanged. When the GPO_OUT_MASK bit is set high (unmasked), the GPO output will be updated when the GPO_OUT_DATA is written (only GPOs that are unmasked will be changed).
GPO_OUT_DATA	0x05	7:0	0x00	GPO output data 0 = pin set low 1 = pin set high Note: GPO_OUT_HIGH_CFG register selects if the pin is driven or high-z. The pin state will follow GPO_OUT_DATA only if the corresponding bit is unmasked in the GPO_OUT_MASK register.
PM_TRIG	0x1C	7:0	0x00	MIPI RFFE power mode and trigger register Bits 7:6 = PWR_MODE Bits 5:0 = TRIG_REG
PROD_ID	0x1D	7:0	0xC4	This is a MIPI RFFE reserved read only register and can not be read since readback is not supported on this device. Bits 7:0 = PRODUCT_ID [7:0] The product ID is provided as information only to support the RFFE USID programming feature.
MAN_ID	0x1E	7:0	0x02	This is a MIPI RFFE reserved read-only register and can not be read since readback is not supported on this device. Bits 7:0 = MANUFACTURER_ID [7:0] The manufacturer ID is provided as information only to support the RFFE USID programming feature.
USID_REG	0x1F	7:0	0x11 (ADR=0) or 0x19 (ADR=1)	This MIPI RFFE reserved register Bits 7:6 = SPARE Bits 5:4 = MANUFACTURER_ID [9:8] = 1 Bits 3:0 = Programmable Unique Slave Identifier — ADR=Low, USID[3:0]=0001 — ADR=High, USID[3:0]=1001 Note: The USID is initially set based on the state of the ADR pin (default value when ADR=Low shown). This register can not be read since readback is not supported on this device. USID_REG[5:4] are provided as information only to support the RFFE USID programming feature.

Table 2. General Bit Field Layout for GPO_x Registers

7	6	5	4	3	2	1	0
GPO_7	GPO_6	GPO_5	GPO_4	GPO_3	GPO_2	GPO_1	GPO_0

Table 3. CNTL_REG Register Bit Fields

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	SW_RESET

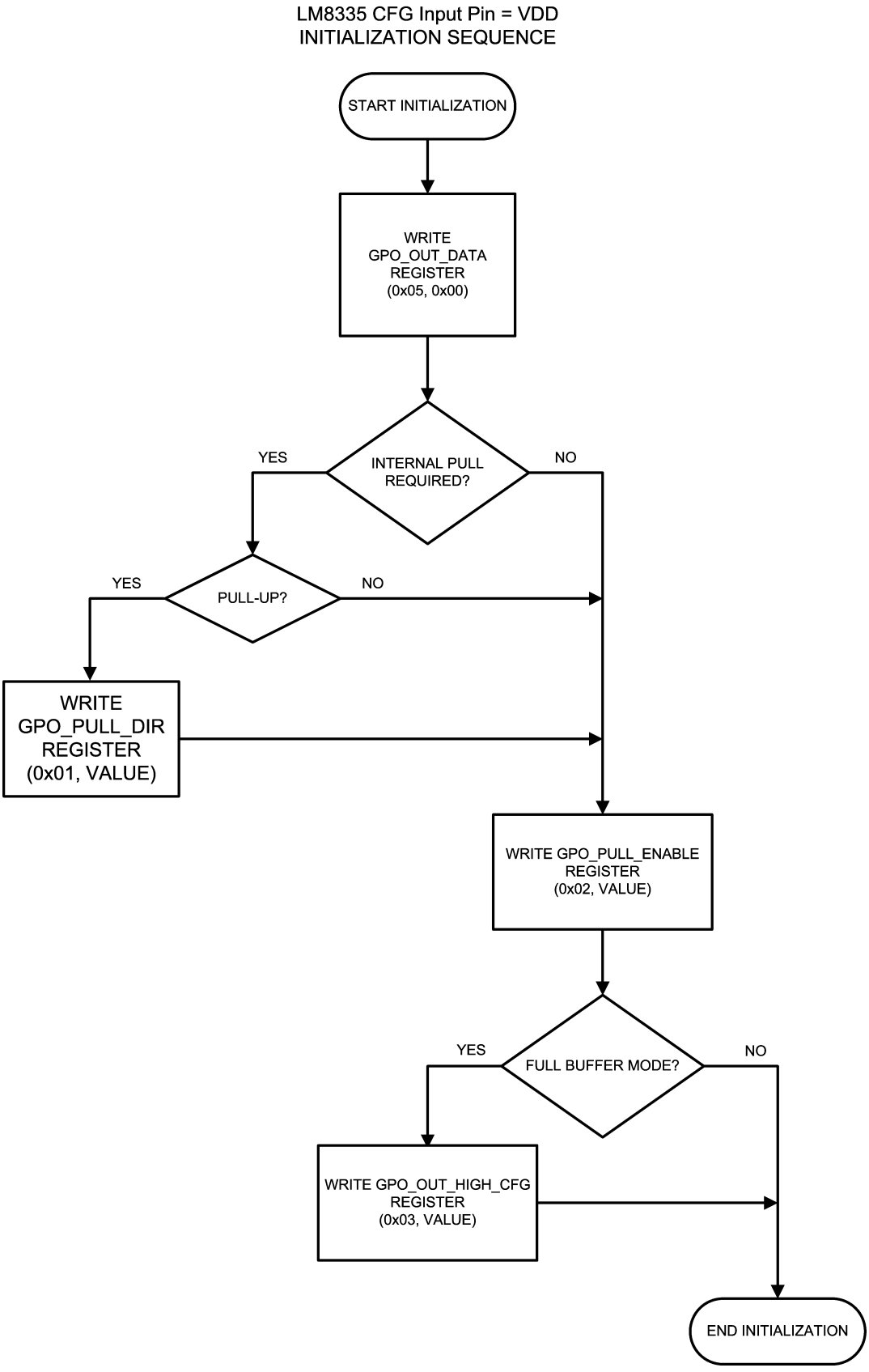


Figure 8. CFG1 MODE Recommended Initialization Sequence

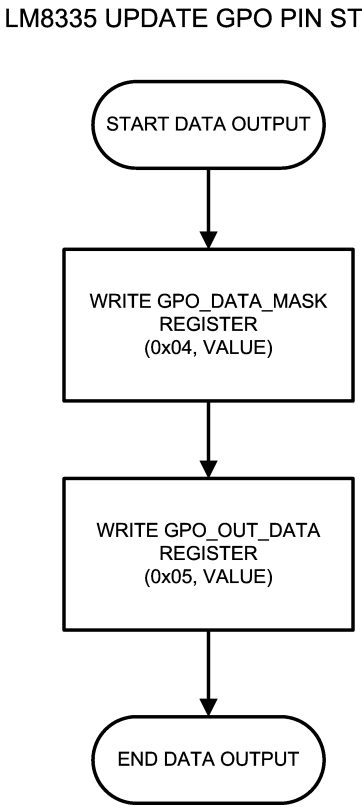


Figure 9. Update GPO Pin State Sequence

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format 14

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM8335TLE/NOPB	Active	Production	DSBGA (YZR) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335
LM8335TLE/NOPB.A	Active	Production	DSBGA (YZR) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335
LM8335TLX/NOPB	Active	Production	DSBGA (YZR) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335
LM8335TLX/NOPB.A	Active	Production	DSBGA (YZR) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8335

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

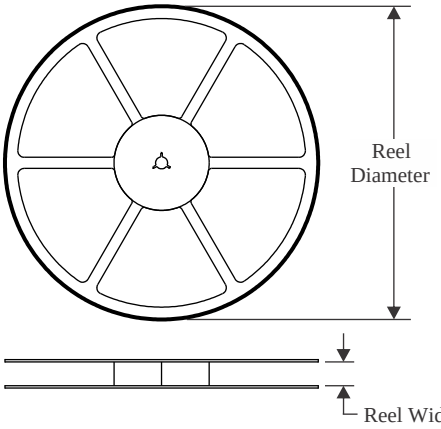
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

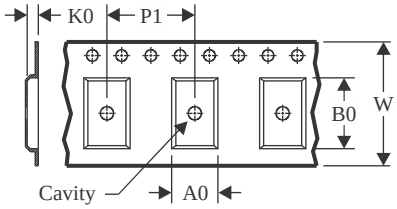
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

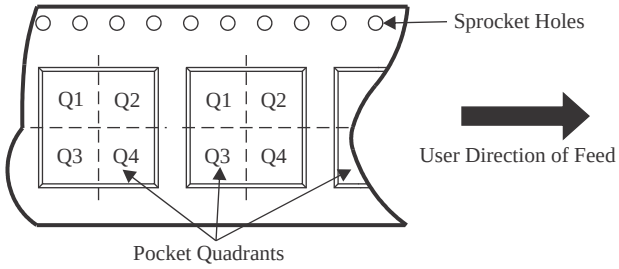


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

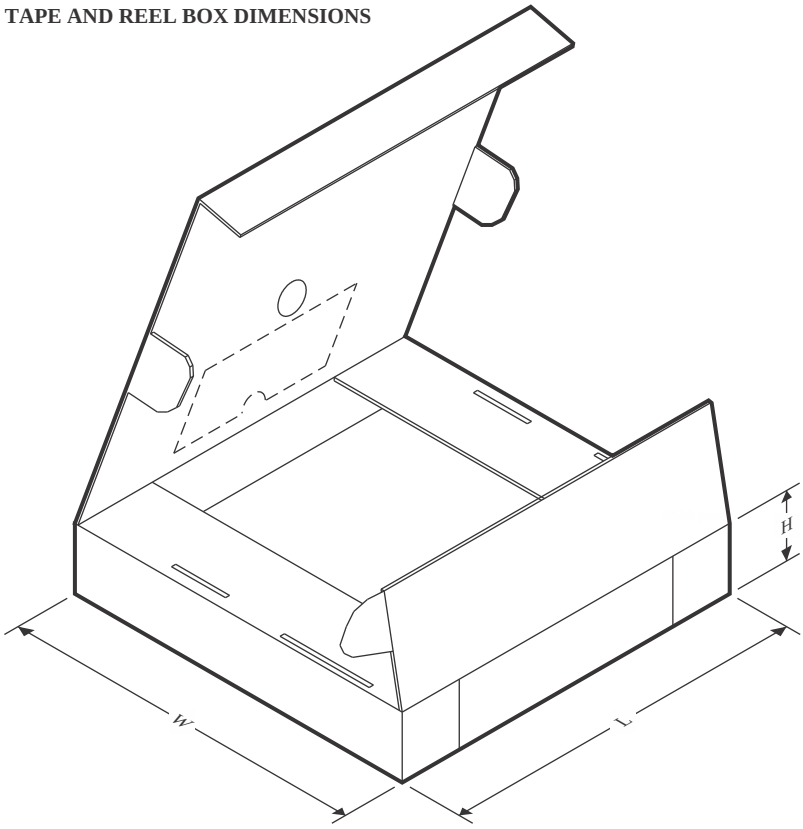
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8335TLE/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM8335TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

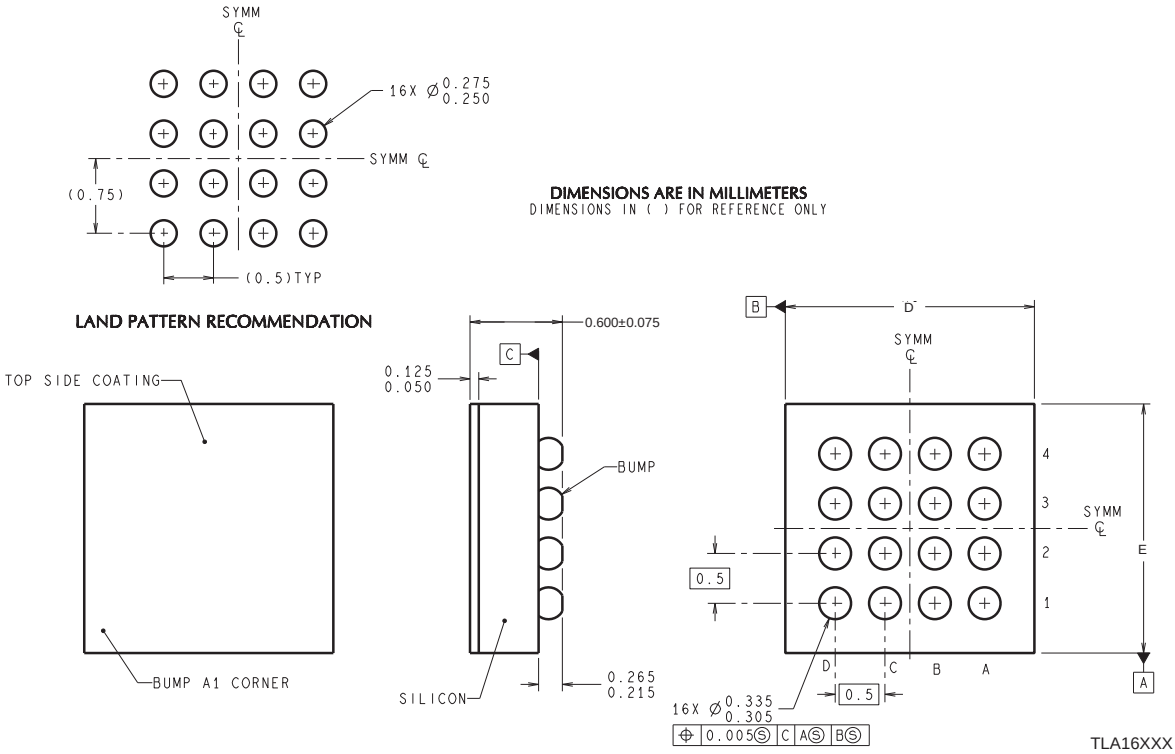
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8335TLE/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM8335TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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