TC1025

Linear Building Block – Dual Low Power Comparator

Features

- Rail-to-Rail Inputs and Outputs
- Optimized for Single Supply Operation
- Small Packages: 8-Pin MSOP, 8-Pin SOIC or 8-Pin PDIP
- Ultra Low Input Bias Current: Less than 100pA
- Low Quiescent Current: 8µA (Typ.)
- Operates Down to V_{DD} = 1.8V

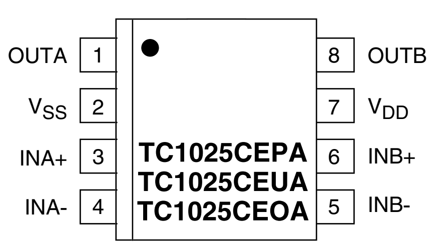
Applications

- Power Management Circuits
- Battery Operated Equipment
- Consumer Products

Device Selection Table

Part Number	Package	Temperature Range
TC1025CEPA	8-Pin PDIP	-40°C to +85°C
TC1025CEUA	8-Pin MSOP	-40°C to +85°C
TC1025CEOA	8-Pin SOIC	-40°C to +85°C

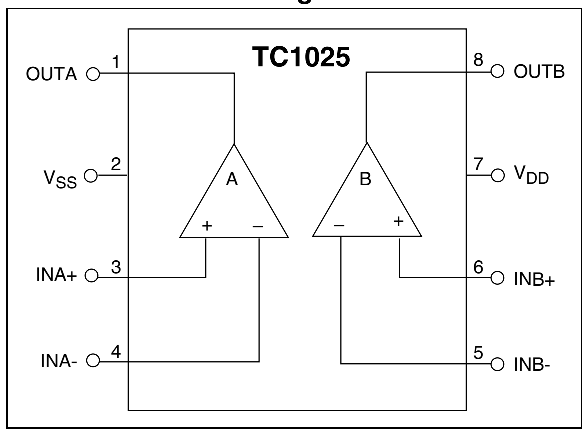
Package Types



General Description

The TC1025 is a dual low-power comparator with a typical supply current of 8µA and operation ensured to V_{DD} = 1.8V. Input and output signal swing is rail-to-rail. Available in a space-saving 8-pin MSOP package, the TC1025 consumes half the board area required by a standard 8-Pin SOIC package. It is also available in 8-Pin SOIC and PDIP packages. It is ideal for applications requiring high integration, small-size and low power.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 6.0V
Voltage on Any Pin ....(V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Junction Temperature......................................+150°C
Operating Temperature Range.............-40°C to +85°C
Storage Temperature Range ....-55°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC1025 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Typical values apply at 25°C and V_{DD} = 3.0V. Minimum and maximum values apply for T_A = -40° to +85°C, and V_{DD} = 1.8V to 5.5V, unless otherwise specified.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
V_{DD}	Supply Voltage	1.8	—	5.5	V	
I_Q	Supply Current	—	8	12	µA	
Comparator						
V_{ICMR}	Common Mode Input Range	V_{SS} – 0.2	—	V_{DD} + 0.2	V	
V_{OS}	Input Offset Voltage	-5 -5	—	+5 +5	mV mV	V_{DD} = 3V, V_{CM} = 1.5V, T_A = 25°C
I_B	Input Bias Current	-100	—	100	pA	T_A = 25°C, IN+,IN- = V_{DD} to V_{SS}
V_{OH}	Output High Voltage	V_{DD} – 0.3	—	—	V	R_L = 10kΩ to V_{SS}
V_{OL}	Output Low Voltage	—	—	0.3	V	R_L = 10kΩ to V_{DD}
CMRR	Common Mode Rejection Ratio	66	—	—	dB	T_A = 25°C, V_{DD} = 5V V_{CM} = V_{DD} to V_{SS}
PSRR	Power Supply Rejection Ratio	60	—	—	dB	T_A = 25°C, V_{CM} = 1.2V V_{DD} = 1.8V to 5V
I_{SRC}	Output Source Current	1	—	—	mA	IN+ = V_{DD}, IN- = V_{SS}, Output Shorted to V_{SS} V_{DD} = 1.8V
I_{SINK}	Output Sink Current	2	—	—	mA	IN+ = V_{SS}, IN- = V_{DD}, Output Shorted to V_{DD} V_{DD} = 1.8V
t_{PD1}	Response Time	—	4	—	µsec	100mV Overdrive, C_L = 100pF
t_{PD2}	Response Time	—	6	—	µsec	10mV Overdrive, C_L = 100pF

2.0 PIN DESCRIPTION

The description of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP) (8-Pin MSOP) (8-Pin SOIC)	Symbol	Description
1	OUTA	Comparator output.
2	V_{SS}	Negative power supply.
3	INA+	Non inverting input.
4	INA-	Inverting input.
5	INB-	Inverting input.
6	INB+	Non inverting input.
7	V_{DD}	Positive power supply.
8	OUTB	Comparator input.

3.0 DETAILED DESCRIPTION

The TC1025 is one of a series of very low-power, linear building block products targeted at low-voltage, single-supply applications. The TC1025 minimum operating voltage is 1.8V, and typical supply current is only 8µA. It combines two comparators in a single package.

3.1 Comparators

The TC1025 contains two comparators. The comparator's input range extends beyond both supply voltages by 200mV and the outputs will swing to within several millivolts of the supplies depending on the load current being driven.

The comparators exhibit propagation delay and supply current which are largely independent of supply voltage. The low input bias current and offset voltage make them suitable for high impedance precision applications.

4.0 TYPICAL APPLICATIONS

The TC1025 lends itself to a wide variety of applications, particularly in battery-powered systems. Typically, it finds application in power management, processor supervisory, and interface circuitry.

4.1 External Hysteresis (Comparator)

Hysteresis can be set externally with two resistors using positive feedback techniques (see Figure 4-1). The design procedure for setting external comparator hysteresis is as follows:

1. Choose the feedback resistor R_C. Since the input bias current of the comparator is at most 100pA, the current through R_C can be set to 100nA (i.e., 1000 times the input bias current) and retain excellent accuracy. The current through R_C at the comparator's trip point is V_R/R_C where V_R is a stable reference voltage.
2. Determine the hysteresis voltage (V_{HY}) between the upper and lower thresholds.
3. Calculate R_A as follows:

EQUATION 4-1:

$$R_A = R_C\left(\frac{V_{HY}}{V_{DD}}\right)$$

4. Choose the rising threshold voltage for V_{SRC} (V_{THR}).
5. Calculate R_B as follows:

EQUATION 4-2:

$$R_B = \frac{1}{\left[\left(\frac{V_{THR}}{V_R \times R_A}\right) - \frac{1}{R_A} - \frac{1}{R_C}\right]}$$

6. Verify the threshold voltages with these formulas:

   V_{SRC} rising:

EQUATION 4-3:

$$V_{THR} = (V_R)(R_A)\left[\left(\frac{1}{R_A}\right) + \left(\frac{1}{R_B}\right) + \left(\frac{1}{R_C}\right)\right]$$

   V_{SRC} falling:

EQUATION 4-4:

$$V_{THF} = V_{THR} - \left[\left(\frac{R_A \times V_{DD}}{R_C}\right)\right]$$

4.2 32.768 kHz "Time of Day Clock" Crystal Controlled Oscillator

A very stable oscillator driver can be designed by using a crystal resonator as the feedback element. Figure 4-2 shows a typical application circuit using this technique to develop clock driver for a Time Of Day (TOD) clock chip. The value of R_A and R_B determine the DC voltage level at which the comparator trips – in this case one-half of V_{DD}. The RC time constant of R_C and C_A should be set several times greater than the crystal oscillator's period, which will ensure a 50% duty cycle by maintaining a DC voltage at the inverting comparator input equal to the absolute average age of the output signal.

4.3 Non-Retriggerable One Shot Multivibrator

Using two comparators, a non-retriggerable one shot multivibrator can be designed using the circuit configuration of Figure 4-3. A key feature of this design is that the pulse width is independent of the magnitude of the supply voltage because the charging voltage and the intercept voltage are a fixed percentage of V_{DD}. In addition, this one shot is capable of pulse width with as much as a 99% duty cycle and exhibits input lockout to ensure that the circuit will not retrigger before the output pulse has completely timed out. The trigger level is the voltage required at the input to raise the voltage at node A higher than the voltage at node B, and is set by the resistive divider R4 and R10 and the impedance network composed of R1, R2 and R3. When the one shot has been triggered, the output of CMPTR2 is high, causing the reference voltage at the non-inverting input of CMPTR1 to go to V_{DD}. This prevents any additional input pulses from disturbing the circuit until the output pulse has timed out.

The value of the timing capacitor C1 must be small enough to allow CMPTR1 to discharge C1 to a diode voltage before the feedback signal from CMPTR2 (through R10) switches CMPTR1 to its high state and allows C1 to start an exponential charge through R5. Proper circuit action depends upon rapidly discharging C1 through the voltage set by R6, R9 and D2 to a final voltage of a small diode drop. Two propagation delays after the voltage on C1 drops below the level on the non-inverting input of CMPTR2, the output of CMPTR1 switches to the positive rail and begins to charge C1 through R5. The time delay which sets the output pulse width results from C1 charging to the reference voltage set by R6, R9 and D2, plus four comparator propagation delays. When the voltage across C1 charges beyond the reference, the output pulse returns to ground and the input is again ready to accept a trigger signal.

4.4 Oscillators and Pulse Width Modulators

Microchip's linear building block comparators adapt well to oscillator applications for low frequencies (less than 100kHz). Figure 4-4 shows a symmetrical square wave generator using a minimum number of components. The output is set by the RC time constant of R4 and C1, and the total hysteresis of the loop is set by R1, R2 and R3. The maximum frequency of the oscillator is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which degrades the slew rate. To analyze this circuit, assume that the output is initially high. For this to occur, the voltage at the inverting input must be less than the voltage at the non-inverting input. Therefore, capacitor C1 is discharged. The voltage at the non-inverting input (V_H) is:

EQUATION 4-5:

$$V_H = \frac{R2(V_{DD})}{[R2 + (R1 \parallel R3)]}$$

where, if R1 = R2 = R3, then:

EQUATION 4-6:

$$V_H = \frac{2(V_{DD})}{3}$$

Capacitor C1 will charge up through R4. When the voltage at the comparator's inverting input is equal to V_H, the comparator output will switch. With the output at ground potential, the value at the non-inverting input terminal (V_L) is reduced by the hysteresis network to a value given by:

EQUATION 4-7:

$$V_L = \frac{V_{DD}}{3}$$

Using the same resistors as before, capacitor C1 must now discharge through R4 toward ground. The output will return to a high state when the voltage across the capacitor has discharged to a value equal to V_L. The period of oscillation will be twice the time it takes for the RC circuit to charge up to one half its final value. The period can be calculated from:

EQUATION 4-8:

$$\frac{1}{FREQ} = 2(0.694)(R4)(C1)$$

The frequency stability of this circuit should only be a function of the external component tolerances.

Figure 4-5 shows the circuit for a pulse width modulator circuit. It is essentially the same as in Figure 4-4, but with the addition of an input control voltage. When the input control voltage is equal to one-half V_{DD}, operation is basically the same as described for the free-running oscillator. If the input control voltage is moved above or below one-half V_{DD}, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. The equations for these trip points are shown in Figure 4-5 (see V_H and V_L). Pulse width sensitivity to the input voltage variations can be increased by reducing the value of R6 from 10kΩ and conversely, sensitivity will be reduced by increasing the value of R6. The values of R1 and C1 can be varied to produce the desired center frequency.

FIGURE 4-1: COMPARATOR EXTERNAL HYSTERESIS CONFIGURATION

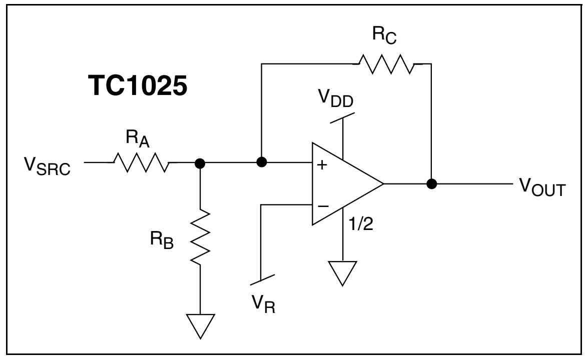


FIGURE 4-2: 32.768 kHz "TIME OF DAY" CLOCK OSCILLATOR

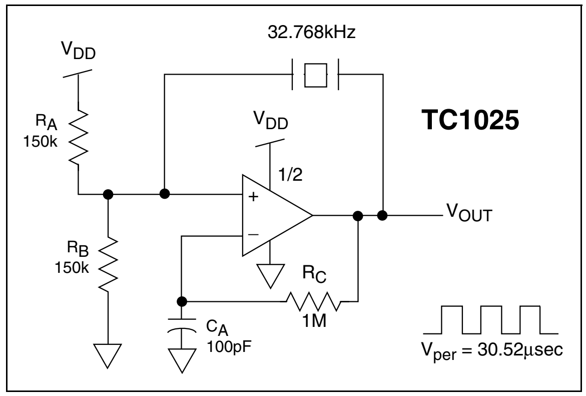


FIGURE 4-3: NON-RETRIGGERABLE MULTIVIBRATOR

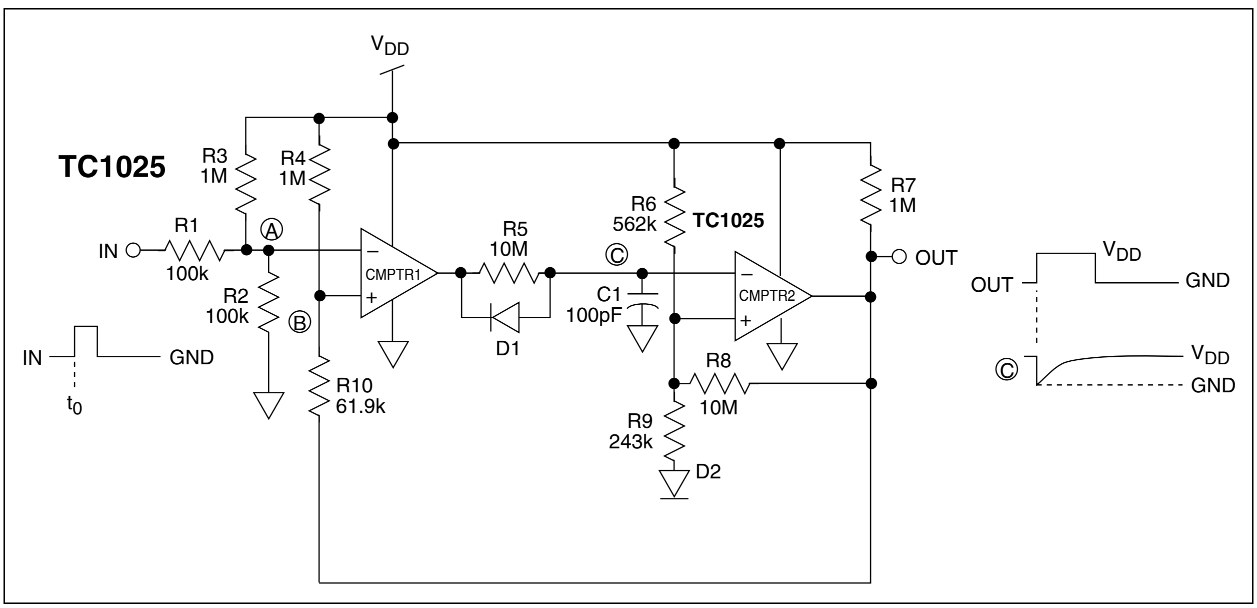
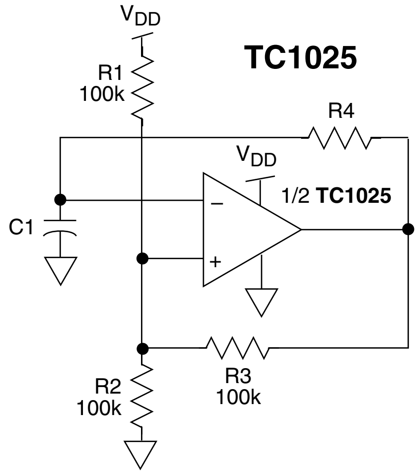


FIGURE 4-4: SQUARE WAVE GENERATOR

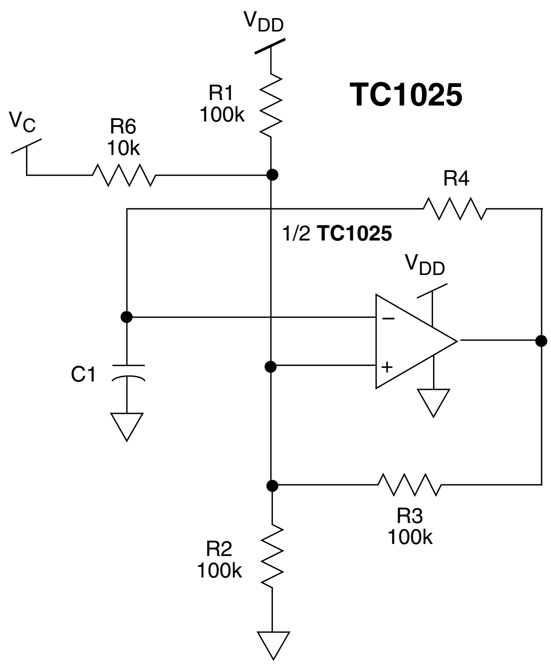


$$V_H = \frac{R2\ (V_{DD})}{R2 + (R1||R3)}$$

$$V_L = \frac{(V_{DD})\ (R2||R3)}{R1 + (R2||R3)}$$

$$FREQ = \frac{1}{2(0.694)(R4)(C1)}$$

FIGURE 4-5: PULSE WIDTH MODULATOR



$$V_H = \frac{V_{DD}\ (R_1R_2R_6 + R_2R_3R_6) + V_C\ (R_1R_2R_3)}{R_1R_2R_6 + R_1R_3R_6 + R_2R_3R_6 + R_1R_2R_3}$$

$$V_L = \frac{V_{DD}\ (R_2R_3R_6) + V_C\ (R_1R_2R_3)}{R_1R_2R_6 + R_1R_3R_6 + R_2R_3R_6 + R_1R_2R_3}$$

$$FREQ = \frac{1}{2\ (0.694)\ (R4)\ (C1)}$$

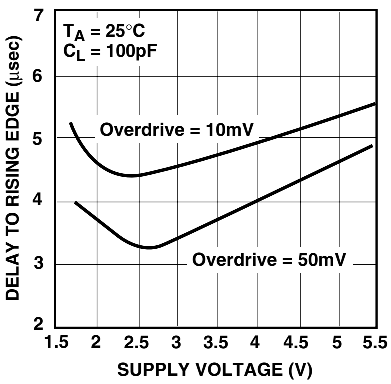
For Square Wave Generation
Select R1 = R2 = R3

$$V_C = \frac{V_{DD}}{2}$$

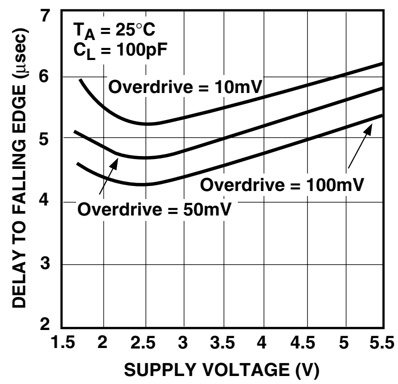
5.0 TYPICAL CHARACTERISTICS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

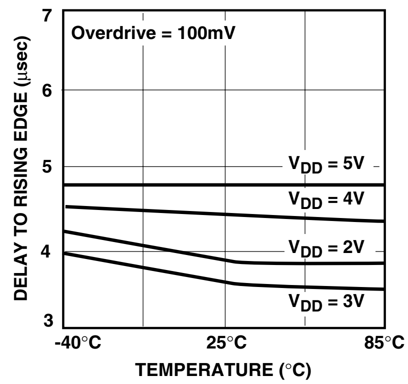
Comparator Propagation Delay vs. Supply Voltage



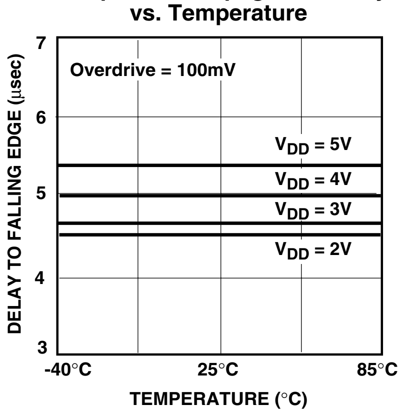
Comparator Propagation Delay vs. Supply Voltage



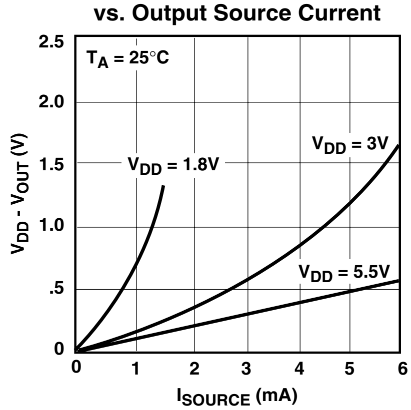
Comparator Propagation Delay vs. Temperature



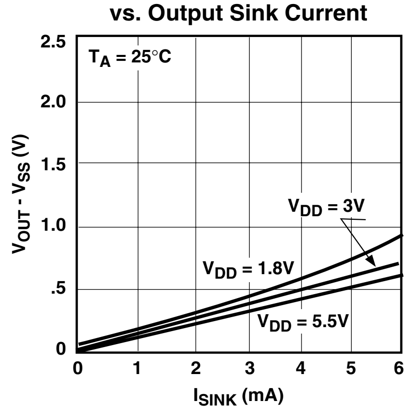
Comparator Propagation Delay vs. Temperature



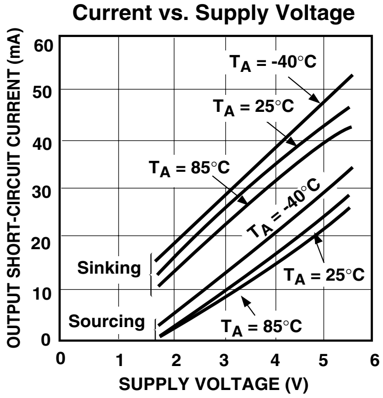
Comparator Output Swing vs. Output Source Current



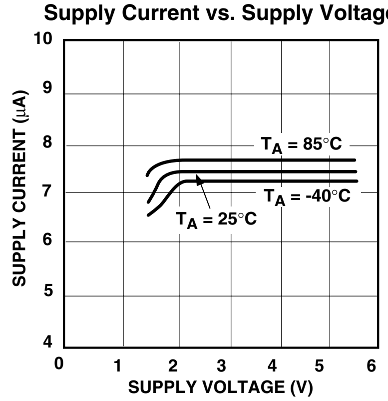
Comparator Output Swing vs. Output Sink Current



Comparator Output Short-Circuit Current vs. Supply Voltage



Supply Current vs. Supply Voltage



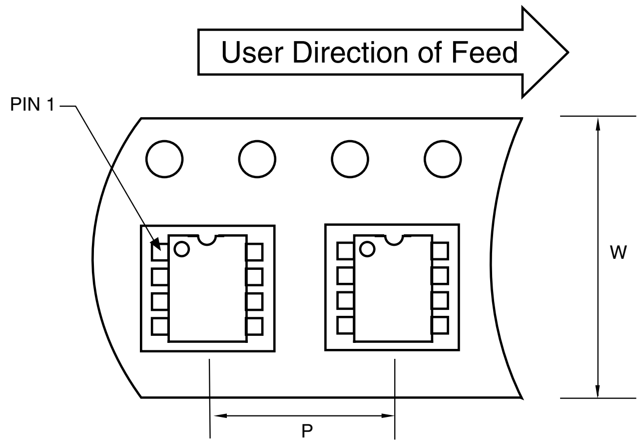
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking data not available at this time.

6.2 Taping Form

Component Taping Orientation for 8-Pin MSOP Devices

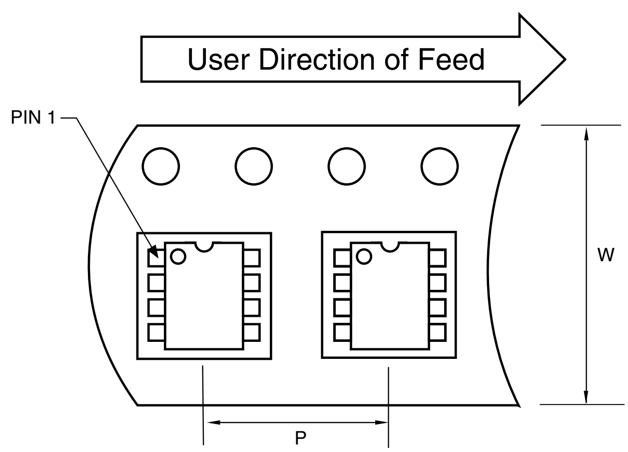


Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



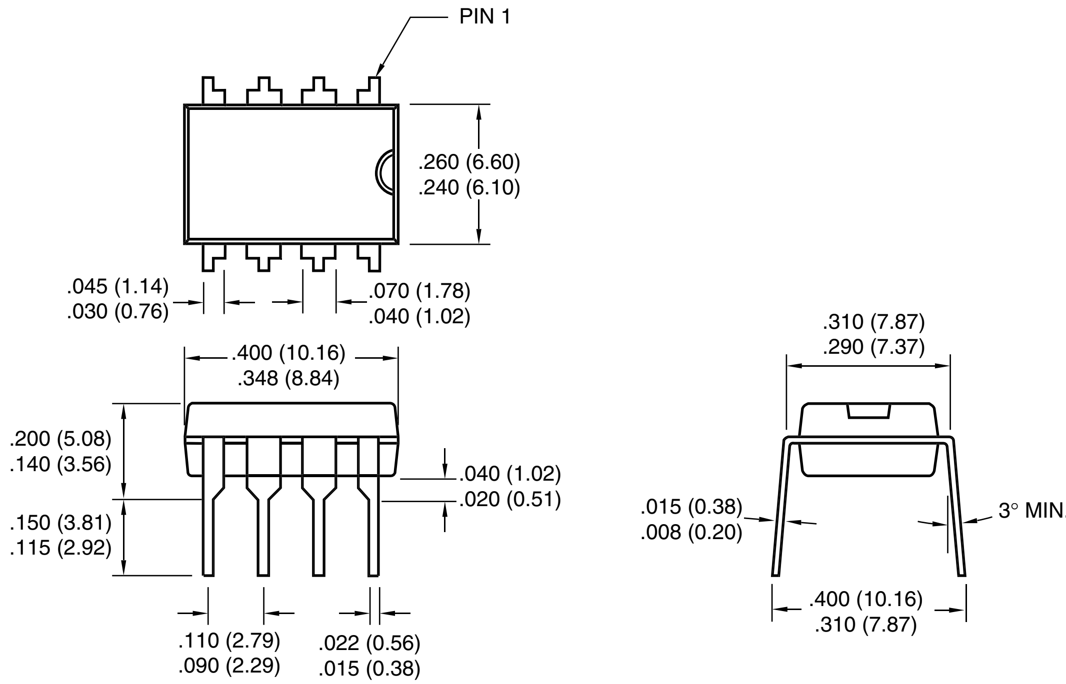
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

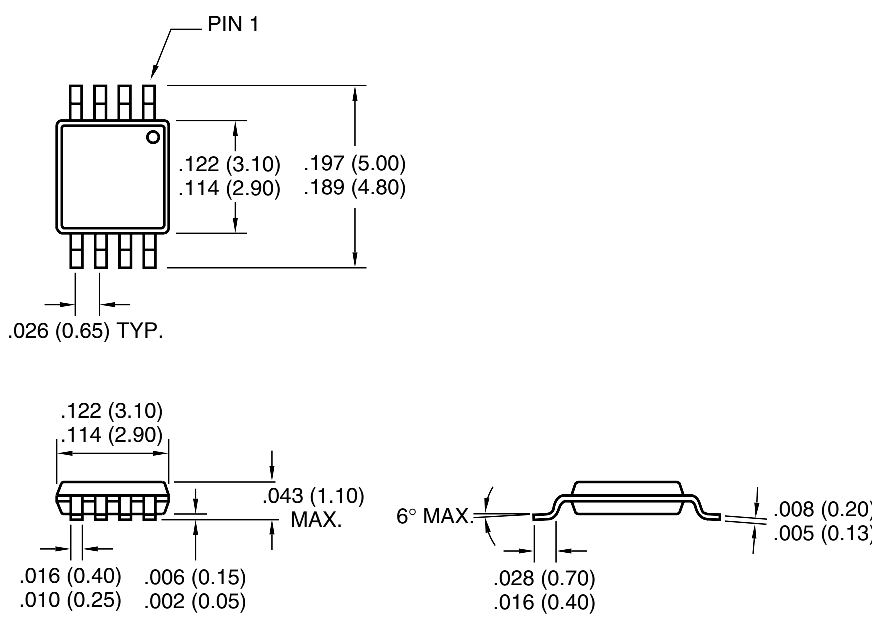
6.3 Package Dimensions

8-Pin Plastic DIP



Dimensions: inches (mm)

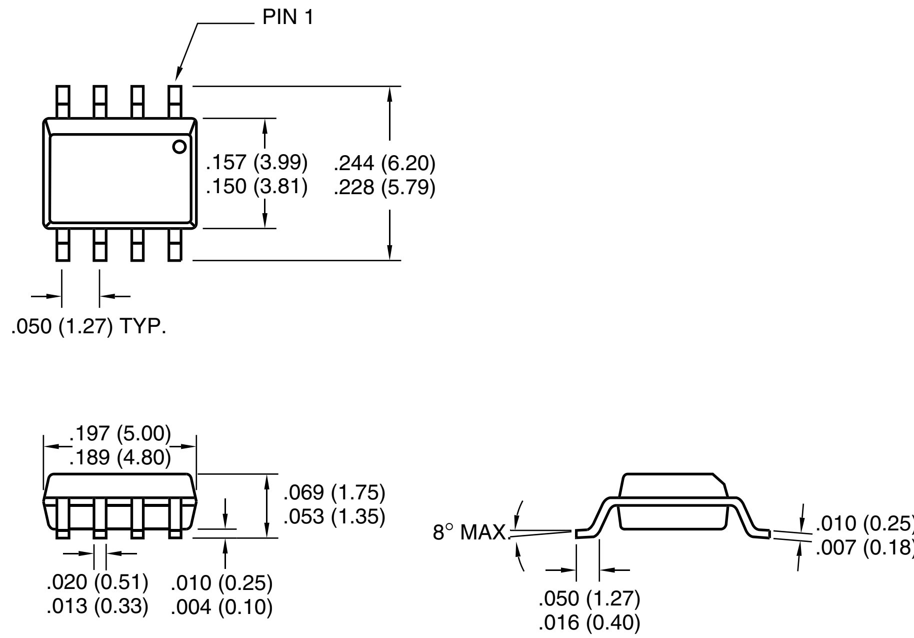
8-Pin MSOP



Dimensions: inches (mm)

6.3 Package Dimensions (Continued)

8-Pin SOIC



Dimensions: inches (mm)

NOTES:

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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