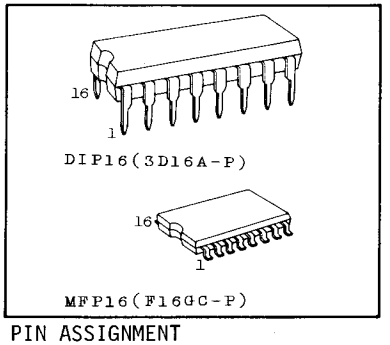
TC4029BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4029BP/TC4029BF PRESETTABLE UP/DOWN COUNTER

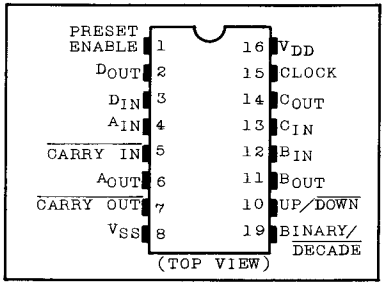
TC4029BP/BF is up/down counter having the capabilities of preset operation, parallel carry connection and decimal/binary switching. Switching of decimal counter and binary counter is controlled by BINARY/$\overline{\text{DECADE}}$ input("H"-Binary and "L"-Decimal), and switching of UP/$\overline{\text{DOWN}}$ is controlled by UP/$\overline{\text{DOWN}}$ input ("H"-Count up and "L"-Count down). As PRESET ENABLE input at "H" level causes input information at A_{IN} through D_{IN} to be directly input to the flip-flops, any arbitrary count can be set. The counter advances its counting state by rising edge of CLOCK input.



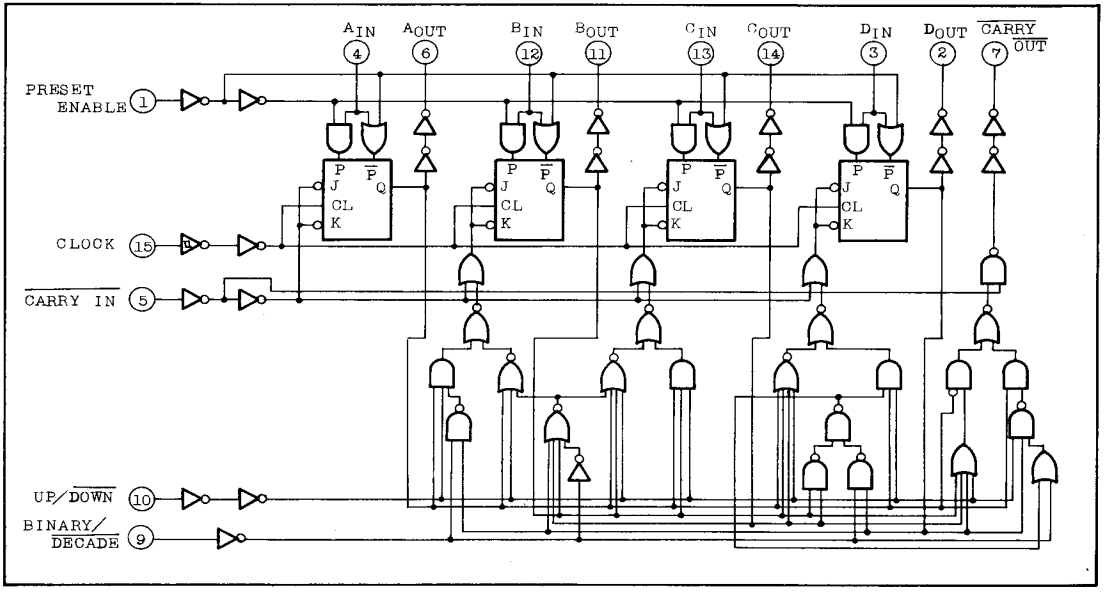
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM

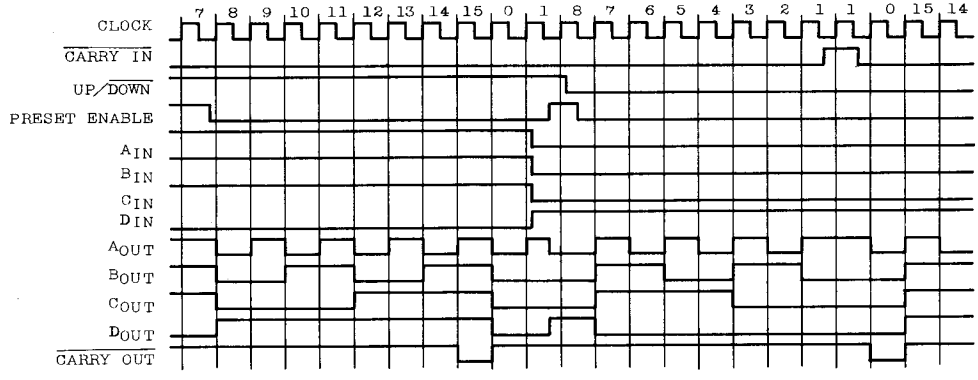


TRUTH TABLE

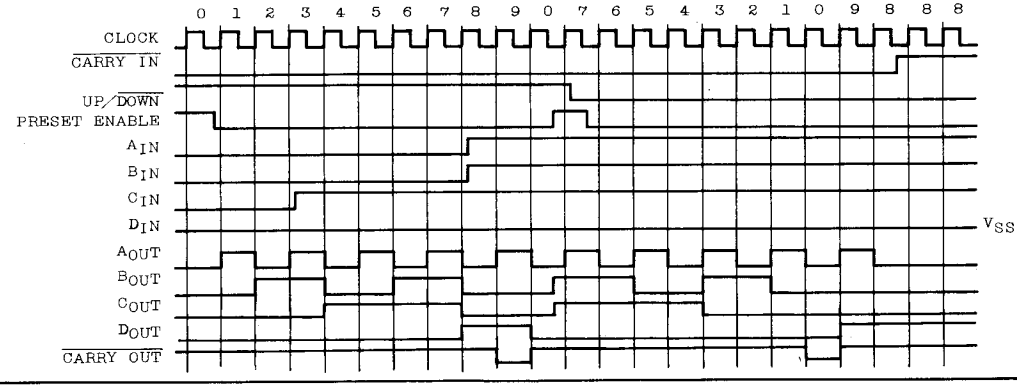
$\overline{\text{CARRY IN}}$	PRESET ENABLE	UP/$\overline{\text{DOWN}}$	BINARY/$\overline{\text{DECADE}}$	OPERATION	
L	L	H	*	UP CONUT	
L	L	L	*	DOWN COUNT	
*	H	*	*	PRESET	* Don't care
H	L	*	*	NO COUNT	
L	L	*	H	BINARY COUNT	
L	L	*	L	DECADE COUNT	

TIMING DIAGRAM

BINARY MODE (B/$\overline{\text{D}}$: "H")



CECADE MODE (B/$\overline{\text{D}}$: "L")



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.2	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.2	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	12.0	-	2.8	-	
		$V_{IN}=V_{SS}$, V_{DD}									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{ID}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

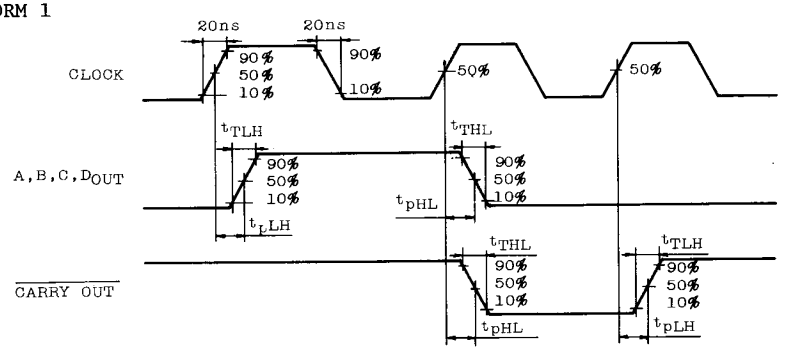
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	70	200	ns
			10	-	35	100	
			15	-	30	80	
Output Transition Time (High to Low)	t_{THL}		5	-	70	200	
			10	-	35	100	
			15	-	30	80	
Propagation Delay Time (CLOCK - A, B, C, D_{OUT})	t_{pLH} t_{pHL}		5	-	180	470	
			10	-	85	200	
			15	-	65	160	
Propagation Delay Time (CLOCK - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	220	500	
			10	-	100	260	
			15	-	75	190	
Propagation Delay Time (PRESET ENABLE - A, B, C, D_{OUT})	t_{pLH} t_{pHL}		5	-	180	470	
			10	-	85	200	
			15	-	65	160	
Propagation Delay Time (PRESET ENABLE - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	240	640	
			10	-	110	290	
			15	-	80	210	
Propagation Delay Time ($\overline{\text{CARRY IN}}$ - $\overline{\text{CARRY OUT}}$)	t_{pLH} t_{pHL}		5	-	85	340	
			10	-	45	100	
			15	-	35	80	
Min. Clock Pulse Width	t_w		5	-	40	130	
			10	-	20	70	
			15	-	15	50	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

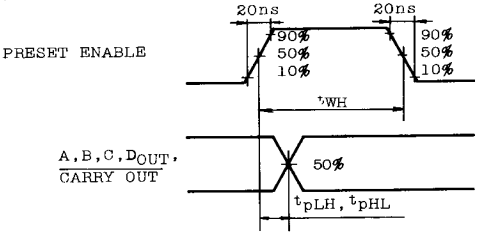
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Pulse Width (PRESET ENABLE)	t_{WH}		5	-	55	130	ns
			10	-	25	70	
			15	-	20	50	
Max. Clock Frequency	f_{CL}		5	2	5	-	MHz
			10	4	10	-	
			15	5.5	14	-	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t_{rCL} t_{fCL}		5 10 15	No Limit			μs
Min. Set-up Time ($\overline{\text{CARRY IN}}$ - CLOCK)	t_{SU}		5	-	75	140	ns
			10	-	35	60	
			15	-	25	30	
Min. Set-up Time (B/$\overline{D}$, U/$\overline{D}$ - CLOCK)	t_{SU}		5	-	120	320	
			10	-	55	130	
			15	-	40	90	
Min. Set-up Time (A,B,C,D - PRESET ENABLE)	t_{SU}		5	-	35	70	
			10	-	15	30	
			15	-	10	20	
Min. Hold Time ($\overline{\text{CARRY IN}}$ - CLOCK)	t_H		5	-	-	50	
			10	-	-	30	
			15	-	-	25	
Min. Hold Time (B/$\overline{D}$, U/$\overline{D}$ - CLOCK)	t_H		5	-	-	30	
			10	-	-	30	
			15	-	-	30	
Min. Hold Time (A,B,C,D - PRESET ENABLE)	t_H		5	-	15	70	
			10	-	10	40	
			15	-	5	40	
Min. Removal Time (PRESET ENABLE - CLOCK)	t_{rem}		5	-	40	150	
			10	-	20	80	
			15	-	15	60	
Input Capacitance	C_{IN}			-	5	7.5	pF

SWITCHING TIME TEST WAVEFORMS

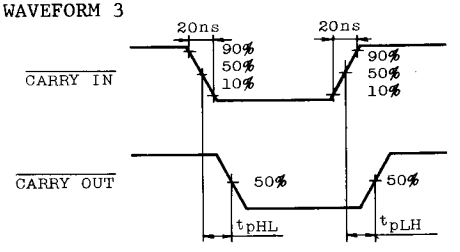
WAVEFORM 1



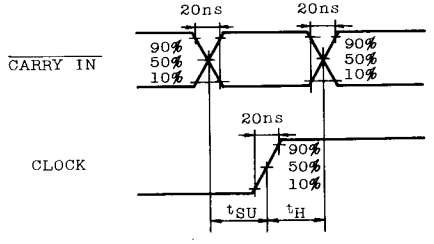
WAVEFORM 2



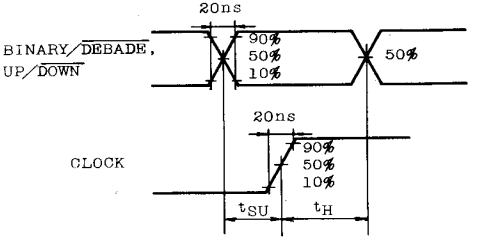
WAVEFORM 3



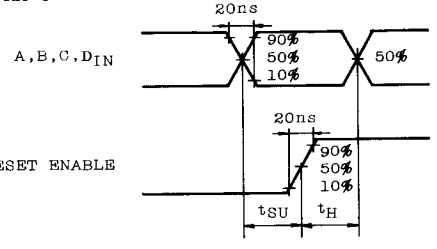
WAVEFORM 4



WAVEFROM 5



WAVEWORM 6



WAVEFORM 7