

## 4A Processor Supply with I<sup>2</sup>C Compatible Interface and Remote Sense

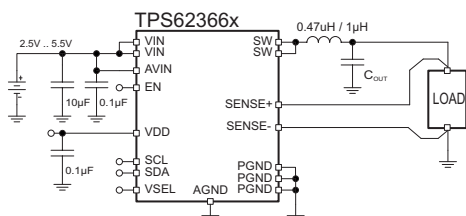
Check for Samples: [TPS62366A](#), [TPS62366B](#)

### FEATURES

- **4A Peak Output Current**
- **Highest Efficiency:**
  - Low  $R_{DS, on}$  Switch and Active Rectifier
  - Power Save Mode for Light Loads
- **I<sup>2</sup>C High Speed Compatible Interface**
- **Programmable Output Voltage for Digital Voltage Scaling**
  - 0.5V to 1.77V, 10mV Steps
- **Excellent DC/AC Output Voltage Regulation**
  - Differential Load Sensing
  - Precise DC Output Voltage Accuracy
  - DCS-Control™ Architecture for Fast and Precise Transient Regulation
- **Multiple Robust Operation/Protection Features:**
  - Soft Start
  - Programmable Slew Rate at Voltage Transition
  - Over Temperature Protection
  - Input Under Voltage Detection / Lock Out
- **Available in 16-Bump, 2mm x 2mm NanoFree™ Package**
- **Low External Device Count: < 25mm<sup>2</sup> Solution Size**

### APPLICATIONS

- **Application Processors and DSPs Power Supply**
- **Dynamic Voltage Scaling, SmartReflex™ Compliant Processor Supply**
- **Cell Phones, Smart Phones, Feature Phones**
- **Tablets, PDAs, MIDs, Netbooks**



### DESCRIPTION

The TPS62366x is a high-frequency synchronous step down dc-dc converter optimized for battery-powered portable applications for a small solution size. With an input voltage range of 2.5V to 5.5V, common battery technologies are supported. The device provides up to 4A peak load current, operating at 2.5MHz typical switching frequency.

The device converts to an output voltage range of 0.5V to 1.77V, programmable via I<sup>2</sup>C interface in 10mV steps. Dedicated inputs allow fast voltage transition to address processor performance operating points.

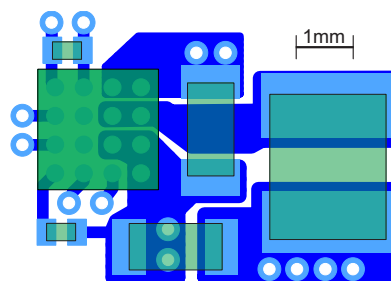
The TPS62366x supports low-voltage DSPs and processor cores in smart-phones and handheld computers including latest submicron processes. A dedicated hardware input pin allows simple transitions to performance operating points and retention modes of processors.

The devices focus on a high output voltage accuracy. The differential sensing and the DCS-Control™ architecture achieve precise static and dynamic, transient output voltage regulation.

The TPS62366x device offers high efficiency step down conversion. The area of highest efficiency is extended towards low output currents to increase the efficiency while the processor is operating in retention mode, as well as towards highest output currents increasing the battery on-time.

The robust architecture and multiple safety features allow perfect system integration.

The 2mm x 2mm package and the low number of required external components lead to a tiny solution size of less than 25mm<sup>2</sup>.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DCS-Control, NanoFree, SmartReflex are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| PART NUMBER              | PACKAGE MARKING                             | PACKAGE | DEVICE SPECIFIC FEATURES <sup>(1)</sup>      |                        |
|--------------------------|---------------------------------------------|---------|----------------------------------------------|------------------------|
|                          |                                             |         | Output Voltage Range                         | Output Voltage Presets |
| TPS62366A <sup>(2)</sup> | See <a href="#">PACKAGE SUMMARY</a> Section | CSP-16  | V <sub>OUT</sub> = 0.5V to 1.77V, 10mV Steps | 1.20V, 1.16V           |
| TPS62366B <sup>(3)</sup> | See <a href="#">PACKAGE SUMMARY</a> Section | CSP-16  | V <sub>OUT</sub> = 0.5V to 1.77V, 10mV Steps | 0.96V, 1.40V           |

- (1) Contact the factory to check availability of other output voltage or feature versions.
- (2) The YZH package is available in tape and reel. Add R suffix (TPS62366AYZHR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel (TPS62366AYZHT). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.
- (3) The YZH package is available in tape and reel. Add R suffix (TPS62366BYZHR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel (TPS62366BYZHT). For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                        |                                                | VALUE |                           | UNIT |
|--------------------------------------------------------|------------------------------------------------|-------|---------------------------|------|
|                                                        |                                                | MIN   | MAX                       |      |
| Voltage range <sup>(2)</sup>                           | VIN, AVIN, SW pin                              | –0.3  | 7                         | V    |
|                                                        | EN, VSEL, SENSE+                               | –0.3  | (V <sub>AVIN</sub> +0.3V) | V    |
|                                                        | SENSE–                                         | –0.3  | 0.3                       | V    |
|                                                        | SCL, SDA                                       | –0.3  | (V <sub>DD</sub> +0.3V)   | V    |
|                                                        | VDD                                            | –0.3  | 3.6                       | V    |
| Continuous RMS VIN / SW current per Pin <sup>(3)</sup> | T <sub>A</sub> < 85°C                          |       | 1275                      | mA   |
| Temperature range                                      | Operating junction temperature, T <sub>J</sub> | –40   | 150                       | °C   |
|                                                        | Storage temperature, T <sub>stg</sub>          | –65   | 150                       | °C   |
| ESD rating <sup>(4)</sup>                              | Machine model                                  |       | 200                       | V    |
|                                                        | Charge device model                            |       | 500                       | V    |
|                                                        | Human body model                               |       | 2                         | kV   |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) In order to be consistent with the TI reliability requirement for the silicon chips (100K Power-On-Hours at 105°C junction temperature), the current should not continuously exceed 2550mA in the VIN pins and 2550mA in the SW pins so as to prevent electromigration failure in the solder. See [THERMAL AND DEVICE LIFETIME INFORMATION](#).
- (4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |                                                             | TPS62366x | UNITS |
|-------------------------------|-------------------------------------------------------------|-----------|-------|
|                               |                                                             | YZH       |       |
|                               |                                                             | 16 PINS   |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 94.8      | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance <sup>(3)</sup>    | 25        |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance <sup>(4)</sup>         | 60        |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter <sup>(5)</sup>   | 3.2       |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter <sup>(6)</sup> | 57        |       |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance <sup>(7)</sup> | n/a       |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|               |                                                       | MIN                 | TYP | MAX | UNIT        |
|---------------|-------------------------------------------------------|---------------------|-----|-----|-------------|
| $V_{IN}$      | Input voltage range, $V_{IN}$                         | $I_{OUT} \leq 2.5A$ | 2.5 | 5.5 | V           |
|               |                                                       | $I_{OUT} \geq 2.5A$ | 2.8 | 5.5 |             |
| $I_{OUT,avg}$ | Continuous output current <sup>(1)</sup>              |                     |     | 2.5 | A           |
| $t_{rf}$      | Rising and falling signal transition time at EN, VSEL | 30                  |     |     | mV/ $\mu$ s |
| $T_A$         | Operating ambient temperature <sup>(2)</sup>          | –40                 |     | 85  | °C          |
| $T_J$         | Operating junction temperature                        | –40                 |     | 150 | °C          |

- (1) Refer to the [APPLICATION INFORMATION](#) section for further information.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature  $[T_{A(max)}]$  is dependent on the maximum operating junction temperature  $[T_{J(max)}]$ , the maximum power dissipation of the device in the application  $[P_{D(max)}]$ , and the junction-to-ambient thermal resistance of the part/package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the specification applies for  $V_{IN} = 3.6V$  over an operating ambient temp.  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for  $T_A = 25^{\circ}C$ .

| PARAMETER                    |                                                     | TEST CONDITIONS                                  |                             | MIN                  | TYP  | MAX                  | UNIT |
|------------------------------|-----------------------------------------------------|--------------------------------------------------|-----------------------------|----------------------|------|----------------------|------|
| INPUT                        |                                                     |                                                  |                             |                      |      |                      |      |
| V <sub>IN</sub>              | Input voltage range at VIN, AVIN                    |                                                  |                             | 2.5                  |      | 5.5                  | V    |
| V <sub>DD</sub>              | I <sup>2</sup> C and registers supply voltage range |                                                  |                             | 1.15                 |      | 3.6                  | V    |
| I <sub>SD(AVIN)</sub>        | Shutdown current into AVIN                          | EN = LOW, V <sub>DD</sub> = 0V                   |                             | 0.65                 |      | 5                    | μA   |
| I <sub>SD(VIN)</sub>         | Shutdown current into VIN                           | EN = LOW, V <sub>DD</sub> = 0V                   | T <sub>A</sub> = 25°C       | 0.5                  |      | 1                    | μA   |
|                              |                                                     |                                                  | T <sub>A</sub> = 85°C       | 1                    |      | 3                    | μA   |
| I <sub>SD(VDD)</sub>         | Shutdown current into VDD                           | EN = LOW, I <sup>2</sup> C bus idle              |                             | 0.01                 |      |                      | μA   |
| I <sub>Q</sub>               | Operating quiescent current into (AVIN + VIN)       | EN = HIGH, I <sub>OUT</sub> = 0mA, not switching | PFM mode                    | 56                   |      |                      | μA   |
|                              |                                                     |                                                  | Forced PWM mode (Test Mode) | 180                  |      |                      | μA   |
| V <sub>UVLO</sub>            | Under voltage lock out at AVIN                      | Input voltage falling, EN = High                 |                             | 2.3                  |      | 2.45                 | V    |
|                              |                                                     | Input voltage rising, EN = Low                   |                             | 1.3                  |      |                      | V    |
| V <sub>UVLO,HYST(AVIN)</sub> | Under voltage lock out hysteresis at AVIN           | Input voltage rising                             |                             | 110                  |      |                      | mV   |
| V <sub>DD,UVLO</sub>         | Under voltage lock out at VDD                       | Input voltage falling                            |                             | 0.7                  | 0.92 | 1.1                  | V    |
| V <sub>UVLO,HYST(VDD)</sub>  | Under voltage lock out hysteresis at VDD            | Input voltage rising                             |                             | 50                   |      |                      | mV   |
| I <sub>VDD</sub>             | Input current at VDD                                | I <sup>2</sup> C not active                      |                             | 0                    |      |                      | μA   |
|                              |                                                     | I <sup>2</sup> C active (r/w)                    |                             | 0.02                 |      | 1                    | mA   |
| LOGIC INTERFACE              |                                                     |                                                  |                             |                      |      |                      |      |
| V <sub>IH</sub>              | High-level input voltage at EN, VSEL                |                                                  |                             | 1.2                  |      |                      | V    |
| V <sub>IL</sub>              | Low-level input voltage at EN, VSEL                 |                                                  |                             |                      |      | 0.4                  | V    |
| V <sub>IH,I2C</sub>          | High-level input voltage at SCL, SDA                |                                                  |                             | 0.7x V <sub>DD</sub> |      |                      | V    |
| V <sub>IL,I2C</sub>          | Low-level input voltage at SCL, SDA                 |                                                  |                             |                      |      | 0.3x V <sub>DD</sub> | V    |
| I <sub>LKG</sub>             | Logic input leakage current at EN, VSEL, SDA, SCL   | Internal pulldown resistors disabled             |                             | 0.05                 |      |                      | μA   |
| R <sub>PD</sub>              | Pull down resistance at EN, VSEL                    | Internal pulldown resistors enabled              |                             | 300                  |      |                      | kΩ   |
|                              | I <sup>2</sup> C clock frequency                    | Fast mode                                        |                             |                      |      | 400                  | kHz  |
|                              |                                                     | High speed mode                                  |                             |                      |      | 3.4                  | MHz  |
| POWER SWITCH                 |                                                     |                                                  |                             |                      |      |                      |      |
| R <sub>DS(on)</sub>          | High side MOSFET switch                             | V <sub>IN</sub> = 3.6V                           |                             | 25                   | 44   | 75                   | mΩ   |
|                              | Low side MOSFET switch                              | V <sub>IN</sub> = 3.6V                           |                             | 25                   | 32   | 50                   | mΩ   |
| I <sub>LIMF</sub>            | High side MOSFET forward current limit              | V <sub>IN</sub> = 3.6V                           |                             | 4.3                  | 4.9  | 5.5                  | A    |
|                              | Low side MOSFET forward current limit               | V <sub>IN</sub> = 3.6V                           |                             | 3.9                  | 4.4  | 4.9                  | A    |
|                              | Low side MOSFET negative current limit              | V <sub>IN</sub> = 3.6V, PWM mode                 |                             | 2.2                  | 2.5  | 2.9                  | A    |
| f <sub>SW</sub>              | Nominal switching frequency                         | PWM mode                                         |                             | 2.5                  |      |                      | MHz  |
| T <sub>JEW</sub>             | Die temperature early warning                       |                                                  |                             | 120                  |      |                      | °C   |
| T <sub>JSD</sub>             | Thermal shutdown                                    |                                                  |                             | 150                  |      |                      | °C   |
| T <sub>JSD,HYST</sub>        | Thermal shutdown hysteresis                         |                                                  |                             | 20                   |      |                      | °C   |
| t <sub>ON,min</sub>          | Minimum on time                                     |                                                  |                             | 120                  |      |                      | ns   |

## ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, the specification applies for  $V_{IN} = 3.6V$  over an operating ambient temp.  $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ ; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for  $T_A = 25^{\circ}C$ .

| PARAMETER     |                                         | TEST CONDITIONS                                                                                                                           | MIN   | TYP         | MAX   | UNIT        |
|---------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------|-------------|-------|-------------|
| <b>OUTPUT</b> |                                         |                                                                                                                                           |       |             |       |             |
| $V_{OUT}$     | Output voltage range                    | 10mV increments                                                                                                                           | 0.5   |             | 1.77  | V           |
|               | Output voltage accuracy                 | $V_{IN} = 2.8V \dots 5.5V$<br>$V_{OUT} = 0.5V \dots 1.77V$<br>No load,<br>Forced PWM,<br>$V_{OUT} = [0.77V, 1.3V]$<br>$T_J = 85^{\circ}C$ | -0.5% |             | +0.5% |             |
|               |                                         | No load,<br>Forced PWM,<br>$T_J = -40 \dots 150^{\circ}C$                                                                                 | -1%   | $\pm 0.5\%$ | +1%   |             |
|               | Line regulation                         | $I_{OUT} = 1A$ , forced PWM                                                                                                               |       | < 0.1       |       | %/V         |
|               | Load regulation                         | $V_{OUT} = 1.2V$ , forced PWM                                                                                                             |       | < 0.05      |       | %/A         |
| $t_{Start}$   | Start-up time                           | Time from active EN to<br>$V_{OUT} = 1.4V$ ,<br>$C_{OUT} < 100\mu F$ , RMP[2:0] = 000,<br>$I_{OUT} = 0mA$                                 |       |             | 1     | ms          |
| $R_{Sense}$   | Input resistance between Sense+, Sense– |                                                                                                                                           |       | 2.2         |       | M $\Omega$  |
|               | Ramp timer                              | RMP[2:0] = 000                                                                                                                            |       | 32          |       | mV/ $\mu s$ |
|               |                                         | RMP[2:0] = 001                                                                                                                            |       | 16          |       |             |
|               |                                         | RMP[2:0] = 010                                                                                                                            |       | 8           |       |             |
|               |                                         | RMP[2:0] = 011                                                                                                                            |       | 4           |       |             |
|               |                                         | RMP[2:0] = 100                                                                                                                            |       | 2           |       |             |
|               |                                         | RMP[2:0] = 101                                                                                                                            |       | 1           |       |             |
|               |                                         | RMP[2:0] = 110                                                                                                                            |       | 0.5         |       |             |
|               |                                         | RMP[2:0] = 111                                                                                                                            |       | 0.25        |       |             |

**I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS<sup>(1)</sup>**

| PARAMETER         |                                                                                       | TEST CONDITIONS                                       | MIN            | MAX  | UNIT    |
|-------------------|---------------------------------------------------------------------------------------|-------------------------------------------------------|----------------|------|---------|
| $f_{(SCL)}$       | SCL clock frequency                                                                   | Standard mode                                         |                | 100  | kHz     |
|                   |                                                                                       | Fast mode                                             |                | 400  | kHz     |
|                   |                                                                                       | High-speed mode (write operation), $C_B - 100$ pF max |                | 3.4  | MHz     |
|                   |                                                                                       | High-speed mode (read operation), $C_B - 100$ pF max  |                | 3.4  | MHz     |
|                   |                                                                                       | High-speed mode (write operation), $C_B - 400$ pF max |                | 1.7  | MHz     |
|                   |                                                                                       | High-speed mode (read operation), $C_B - 400$ pF max  |                | 1.7  | MHz     |
| $t_{BUF}$         | Bus free time between a STOP and START condition                                      | Standard mode                                         | 4.7            |      | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 1.3            |      | $\mu$ s |
| $t_{HD}, t_{STA}$ | Hold time (repeated) START condition                                                  | Standard mode                                         | 4              |      | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 600            |      | ns      |
|                   |                                                                                       | High-speed mode                                       | 160            |      | ns      |
| $t_{LOW}$         | Low period of the SCL clock                                                           | Standard mode                                         | 4.7            |      | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 1.3            |      | $\mu$ s |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 160            |      | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 320            |      | ns      |
| $t_{HIGH}$        | High period of the SCL clock                                                          | Standard mode                                         | 4              |      | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 600            |      | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 60             |      | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 120            |      | ns      |
| $t_{SU}, t_{STA}$ | Setup time for a repeated START condition                                             | Standard mode                                         | 4.7            |      | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 600            |      | ns      |
|                   |                                                                                       | High-speed mode                                       | 160            |      | ns      |
| $t_{SU}, t_{DAT}$ | Data setup time                                                                       | Standard mode                                         | 250            |      | ns      |
|                   |                                                                                       | Fast mode                                             | 100            |      | ns      |
|                   |                                                                                       | High-speed mode                                       | 10             |      | ns      |
| $t_{HD}, t_{DAT}$ | Data hold time                                                                        | Standard mode                                         | 0              | 3.45 | $\mu$ s |
|                   |                                                                                       | Fast mode                                             | 0              | 0.9  | $\mu$ s |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 0              | 70   | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 0              | 150  | ns      |
| $t_{RCL}$         | Rise time of SCL signal                                                               | Standard mode                                         | $20 + 0.1 C_B$ | 1000 | ns      |
|                   |                                                                                       | Fast mode                                             | $20 + 0.1 C_B$ | 300  | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 10             | 40   | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 20             | 80   | ns      |
| $t_{RCL1}$        | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard mode                                         | $20 + 0.1 C_B$ | 1000 | ns      |
|                   |                                                                                       | Fast mode                                             | $20 + 0.1 C_B$ | 300  | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 10             | 80   | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 20             | 160  | ns      |
| $t_{FCL}$         | Fall time of SCL signal                                                               | Standard mode                                         | $20 + 0.1 C_B$ | 300  | ns      |
|                   |                                                                                       | Fast mode                                             | $20 + 0.1 C_B$ | 300  | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 10             | 40   | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 20             | 80   | ns      |
| $t_{RDA}$         | Rise time of SDA signal                                                               | Standard mode                                         | $20 + 0.1 C_B$ | 1000 | ns      |
|                   |                                                                                       | Fast mode                                             | $20 + 0.1 C_B$ | 300  | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 100$ pF max                   | 10             | 80   | ns      |
|                   |                                                                                       | High-speed mode, $C_B - 400$ pF max                   | 20             | 160  | ns      |

(1) S/M = standard mode; F/M = fast mode

## I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS<sup>(1)</sup> (continued)

| PARAMETER                                       | TEST CONDITIONS                     | MIN            | MAX | UNIT    |
|-------------------------------------------------|-------------------------------------|----------------|-----|---------|
| $t_{FDA}$ Fall time of SDA signal               | Standard mode                       | $20 + 0.1 C_B$ | 300 | ns      |
|                                                 | Fast mode                           | $20 + 0.1 C_B$ | 300 | ns      |
|                                                 | High-speed mode, $C_B = 100$ pF max | 10             | 80  | ns      |
|                                                 | High-speed mode, $C_B = 400$ pF max | 20             | 160 | ns      |
| $t_{SU}, t_{STO}$ Setup time for STOP condition | Standard mode                       | 4              |     | $\mu$ s |
|                                                 | Fast mode                           | 600            |     | ns      |
|                                                 | High-speed mode                     | 160            |     | ns      |
| $C_B$ Capacitive load for SDA and SCL           |                                     |                | 400 | pF      |

## I<sup>2</sup>C TIMING DIAGRAMS

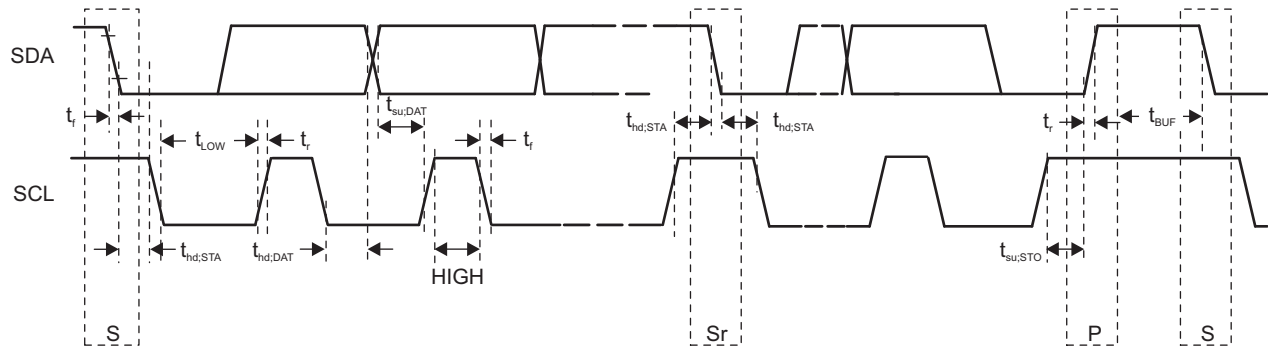
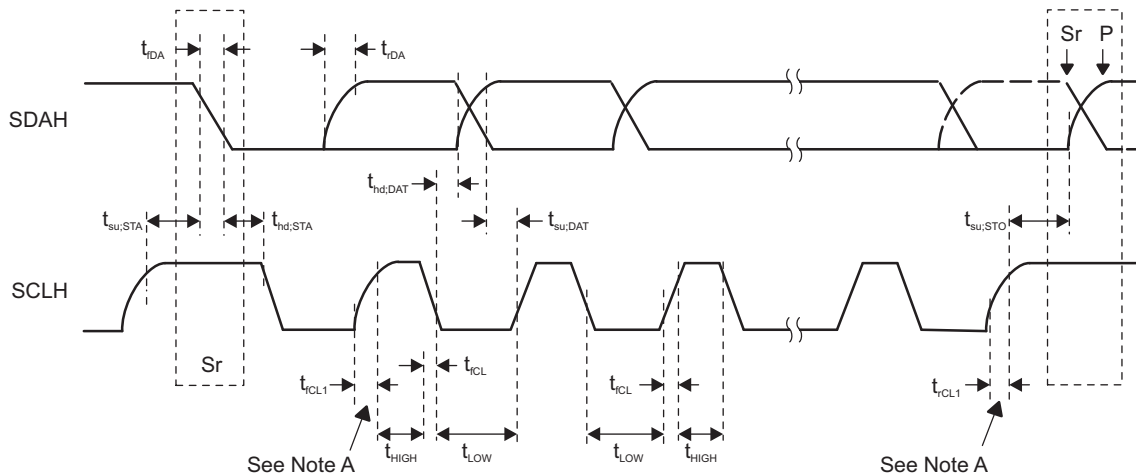


Figure 1. Serial Interface Timing for F/S Mode



= MCS Current Source Pull-Up

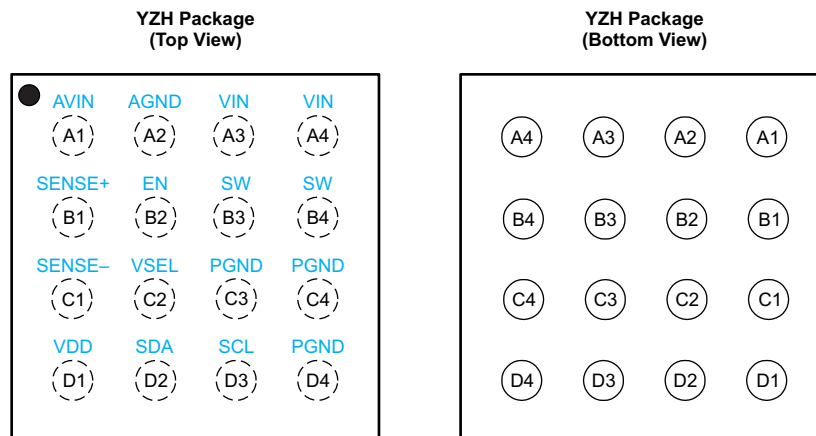
=  $R_{(P)}$  Resistor Pull-Up

Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 2. Serial Interface Timing for H/S Mode

## DEVICE INFORMATION

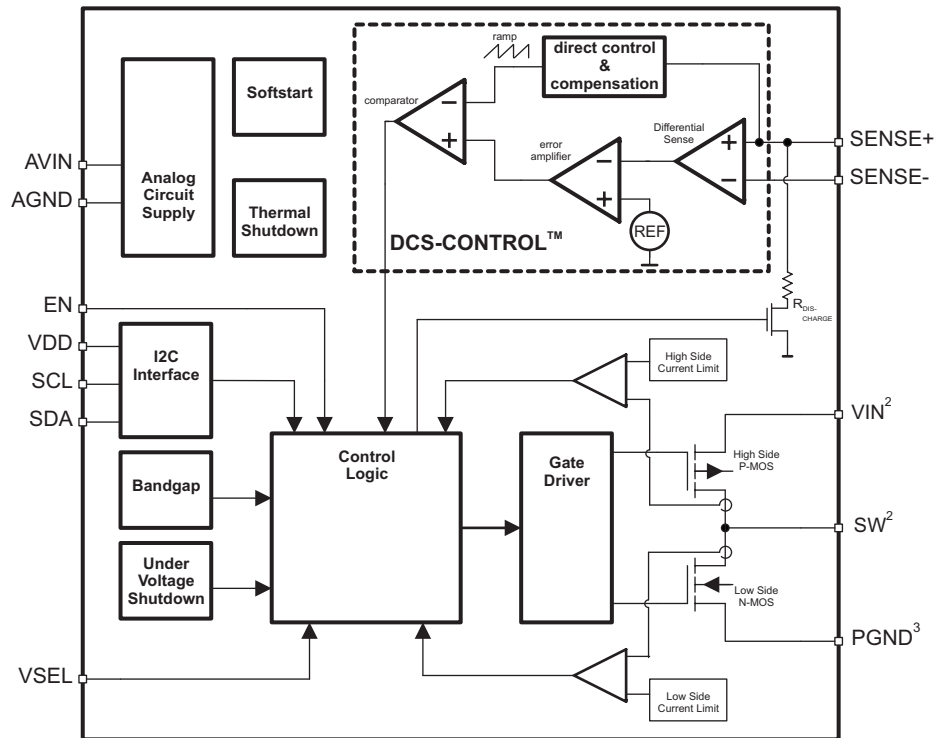
### PIN ASSIGNMENTS



### PIN FUNCTIONS

| PIN    |     | I/O | DESCRIPTION                                                                                                                                                                                                               |
|--------|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME   | NO. |     |                                                                                                                                                                                                                           |
| AVIN   | A1  | I   | Analog Supply Voltage Input.                                                                                                                                                                                              |
| AGND   | A2  | –   | Analog Ground Connection.                                                                                                                                                                                                 |
| EN     | B2  | I   | Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown. The pin must be terminated to either HIGH or LOW if the internal pull down resistor is deactivated.   |
| VDD    | D1  | I   | I <sup>2</sup> C Logic and Registers supply voltage. For resetting the internal registers, this connection must be pulled below its UVLO level.                                                                           |
| SCL    | D3  | I/O | I <sup>2</sup> C clock signal.                                                                                                                                                                                            |
| SDA    | D2  | I/O | I <sup>2</sup> C data signal.                                                                                                                                                                                             |
| VSEL   | C2  | I   | Output Settings Selection Logic Input. Predefined register settings can be chosen for setting output voltage and mode. The pin must be terminated to logic HIGH or LOW if the internal pull down resistor is deactivated. |
| SW     | B3  | –   | Inductor connection                                                                                                                                                                                                       |
|        | B4  |     |                                                                                                                                                                                                                           |
| SENSE+ | B1  | I   | Positive Output Voltage Remote Sense. Must be connected closest to the load supply node.                                                                                                                                  |
| SENSE– | C1  | I   | Negative Output Voltage Remote Sense. Must be connected closest to the load ground node.                                                                                                                                  |
| VIN    | A4  | I   | Power Supply Voltage Input.                                                                                                                                                                                               |
|        | A3  |     |                                                                                                                                                                                                                           |
| PGND   | C3  | –   | Power Ground Connection.                                                                                                                                                                                                  |
|        | C4  |     |                                                                                                                                                                                                                           |
|        | D4  |     |                                                                                                                                                                                                                           |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

|                             |                                  |                                                     | FIGURE                                                        |
|-----------------------------|----------------------------------|-----------------------------------------------------|---------------------------------------------------------------|
| $\eta$                      | Efficiency                       | vs. Output Current (Power Save and Forced PWM Mode) | $V_{OUT} = 1.5V$                                              |
|                             |                                  |                                                     | $V_{OUT} = 1.2V$                                              |
|                             |                                  |                                                     | $V_{OUT} = 0.9V$                                              |
|                             |                                  |                                                     | $V_{OUT} = 0.6V$                                              |
|                             |                                  | vs. Input Voltage (Power Save and Forced PWM Mode)  | $I_{OUT} = 4000mA$                                            |
|                             |                                  |                                                     | $I_{OUT} = 1000mA$                                            |
|                             |                                  |                                                     | $I_{OUT} = 100mA$                                             |
|                             |                                  |                                                     | $I_{OUT} = 10mA$                                              |
| $V_O$                       | DC Output Voltage                | vs. Output Current (Power Save and Forced PWM Mode) | $V_{OUT} = 1.5V, T_A = 25^\circ C$                            |
|                             |                                  |                                                     | $V_{OUT} = 1.2V, T_A = 25^\circ C$                            |
|                             |                                  |                                                     | $V_{OUT} = 0.9V, T_A = 25^\circ C$                            |
|                             |                                  |                                                     | $V_{OUT} = 0.6V, T_A = 25^\circ C$                            |
|                             | Startup                          | Into No Load                                        | $V_{OUT} = 0.5V, I_{OUT} = 0mA$                               |
|                             |                                  |                                                     | $V_{OUT} = 1.5V, I_{OUT} = 0mA$                               |
|                             |                                  | Into Load                                           | $V_{OUT} = 0.5V, I_{OUT} = 1000mA$                            |
|                             |                                  |                                                     | $V_{OUT} = 1.5V, I_{OUT} = 1000mA$                            |
|                             | Switching Wave forms             | $L = 1\mu H$                                        | $I_{OUT} = 10mA$                                              |
|                             |                                  |                                                     | $I_{OUT} = 200mA$                                             |
|                             |                                  |                                                     | $I_{OUT} = 1000mA$                                            |
|                             |                                  |                                                     | $I_{OUT} = 4000mA$                                            |
|                             |                                  | $L = 0.47\mu H$                                     | $I_{OUT} = 10mA$                                              |
|                             |                                  |                                                     | $I_{OUT} = 200mA$                                             |
|                             |                                  |                                                     | $I_{OUT} = 1000mA$                                            |
|                             |                                  |                                                     | $I_{OUT} = 4000mA$                                            |
|                             | Output Voltage Ramp Control      | Transition 0.5V .. 1.5V                             | $I_{OUT} = 0mA$                                               |
|                             |                                  |                                                     | $I_{OUT} = 1000mA$                                            |
|                             | Load Transient Response          | $L = 1\mu H$                                        | $I_{OUT} = 50mA$ to 200mA                                     |
|                             |                                  |                                                     | $I_{OUT} = 200mA$ to 1000mA                                   |
|                             |                                  |                                                     | $I_{OUT} = 2500mA$ to 4000mA                                  |
|                             |                                  | $L = 0.47\mu H$                                     | $I_{OUT} = 50mA$ to 200mA                                     |
|                             |                                  |                                                     | $I_{OUT} = 200mA$ to 1000mA                                   |
|                             |                                  |                                                     | $I_{OUT} = 2500mA$ to 4000mA                                  |
|                             | Line Transient Response          |                                                     | $V_{IN} = 3.6$ to $4.2V, I_{OUT} = 3500mA$                    |
| $I_{SD(VIN)}, I_{SD(AVIN)}$ | Shutdown Current at AVIN and VIN | vs. Input Voltage                                   | $T_A = [-40^\circ C, 25^\circ C, 125^\circ C]$                |
| $I_Q$                       | Operating Quiescent Current      | vs. Input Voltage                                   | $T_A = [-40^\circ C, 25^\circ C, 125^\circ C]$ , auto PFM/PWM |
| $f_{SW}$                    | Switching Frequency              | vs. Output Current                                  | $V_{OUT} = 1.2V$                                              |
| $I_{LIM}$                   | Current Limit                    | vs. Input Voltage                                   |                                                               |
| $I_{OUT}$                   | Maximum DC Output current        | vs. Input Voltage                                   | $V_{OUT} = [0.6V, 0.9V, 1.2V, 1.5V]$                          |

# TYPICAL CHARACTERISTICS (continued)

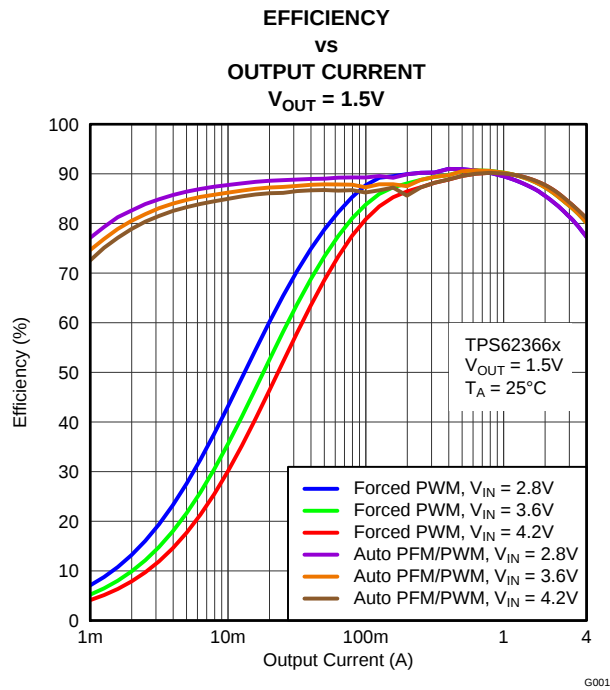


Figure 3.

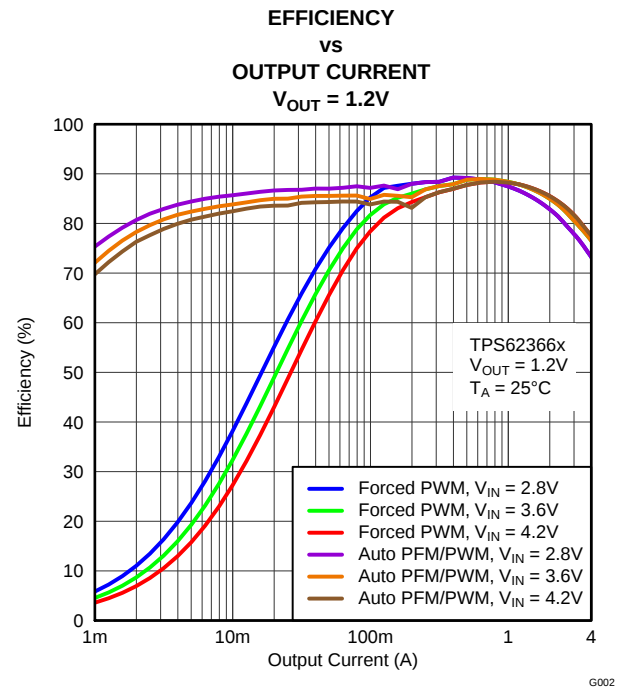


Figure 4.

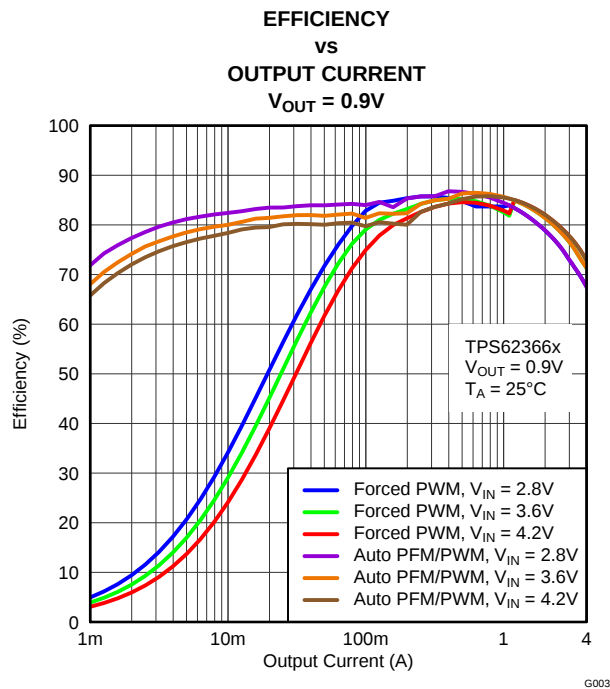


Figure 5.

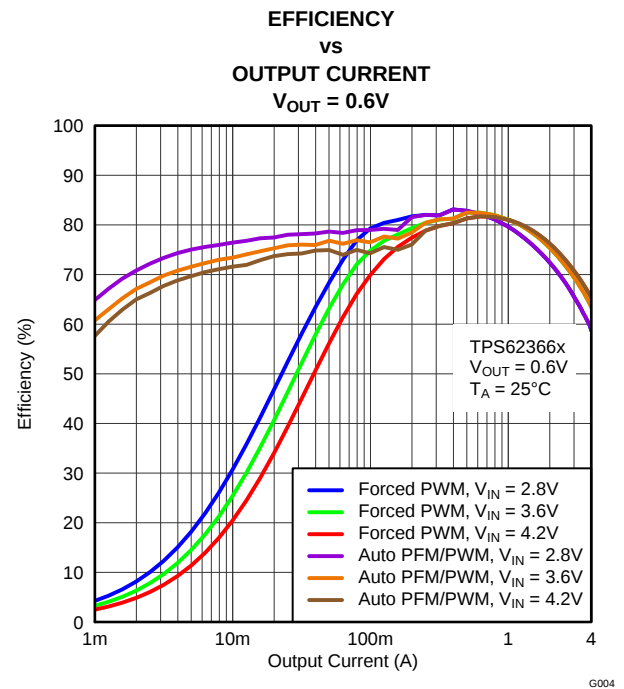


Figure 6.

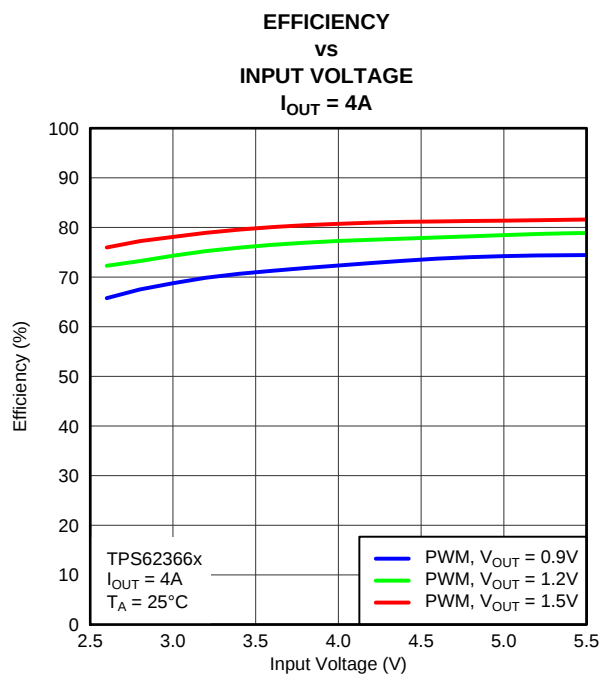
**TYPICAL CHARACTERISTICS (continued)**

Figure 7.

G005

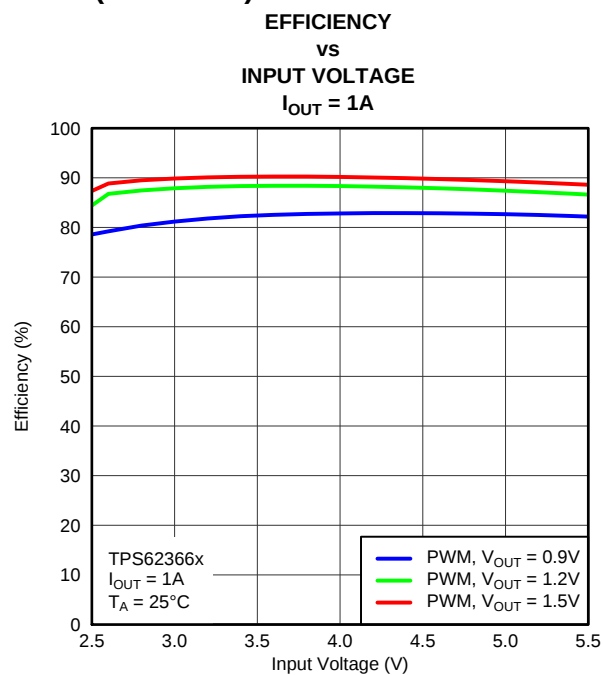


Figure 8.

G006

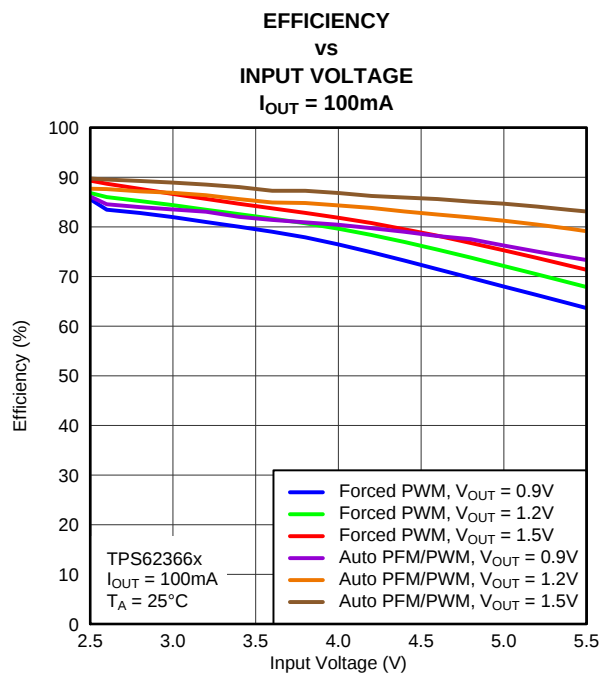


Figure 9.

G007

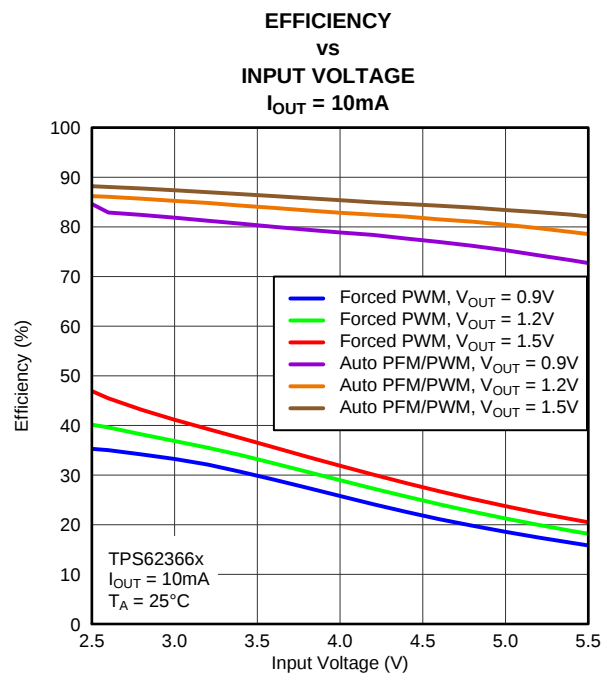


Figure 10.

G008

## TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE

vs

OUTPUT CURRENT

$V_{OUT} = 1.5V$

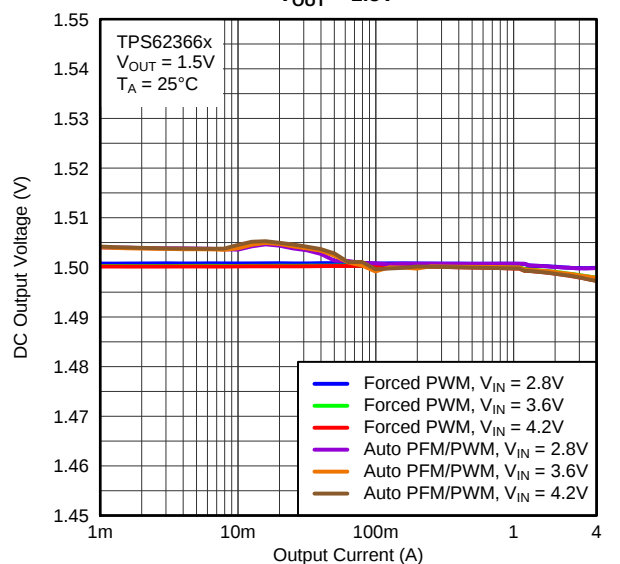


Figure 11.

DC OUTPUT VOLTAGE

vs

OUTPUT CURRENT

$V_{OUT} = 1.2V$

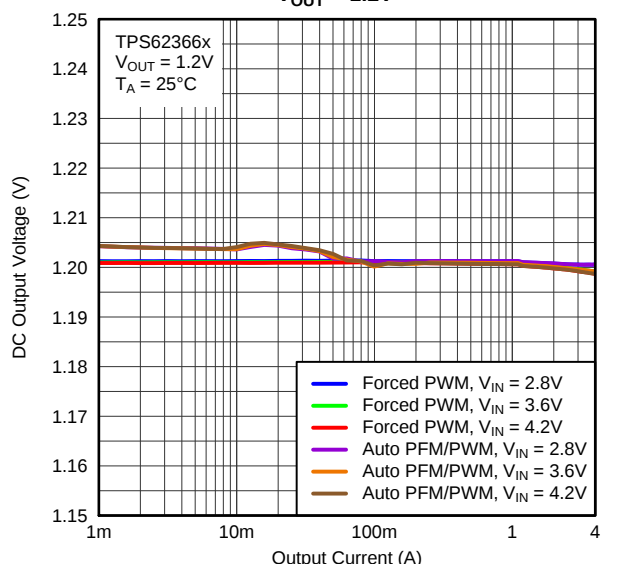


Figure 12.

DC OUTPUT VOLTAGE

vs

OUTPUT CURRENT

$V_{OUT} = 0.9V$

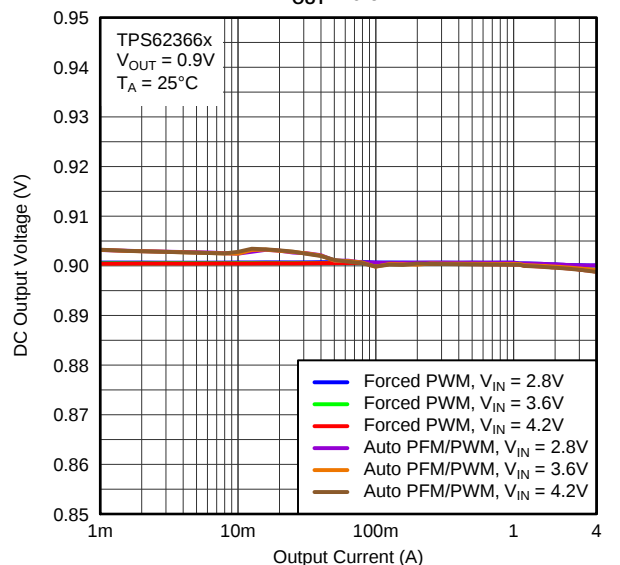


Figure 13.

DC OUTPUT VOLTAGE

vs

OUTPUT CURRENT

$V_{OUT} = 0.6V$

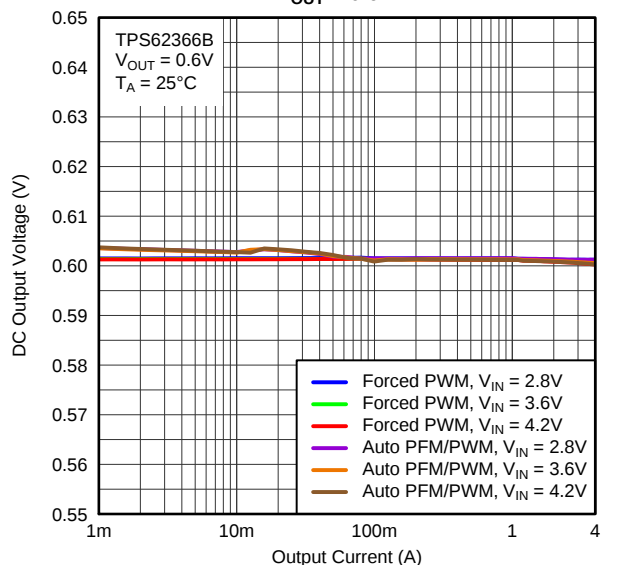


Figure 14.

## TYPICAL CHARACTERISTICS (continued)

### STARTUP INTO NO LOAD

$V_{OUT} = 0.5V$

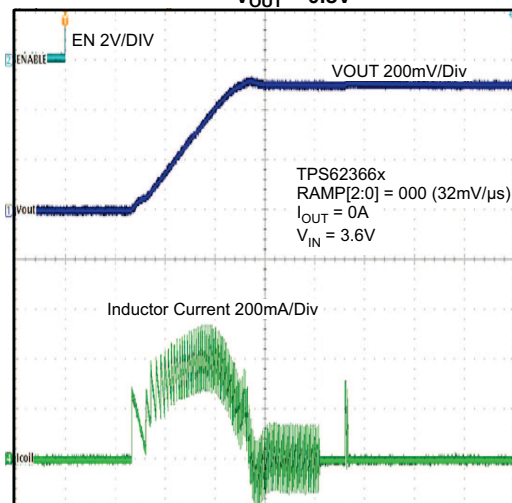


Figure 15.

G013

### STARTUP INTO NO LOAD

$V_{OUT} = 1.5V$

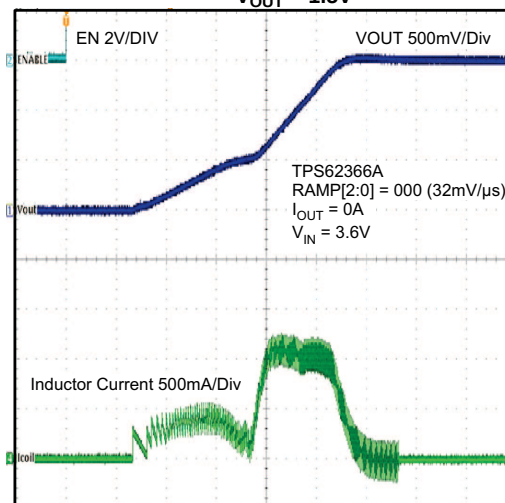


Figure 16.

G014

### STARTUP INTO LOAD

$V_{OUT} = 0.5V$

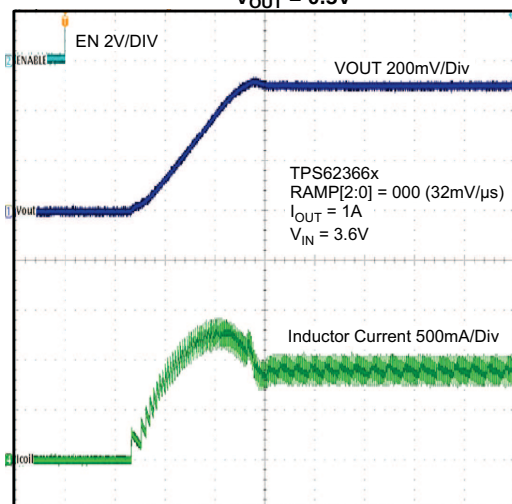


Figure 17.

G015

### STARTUP INTO LOAD

$V_{OUT} = 1.5V$

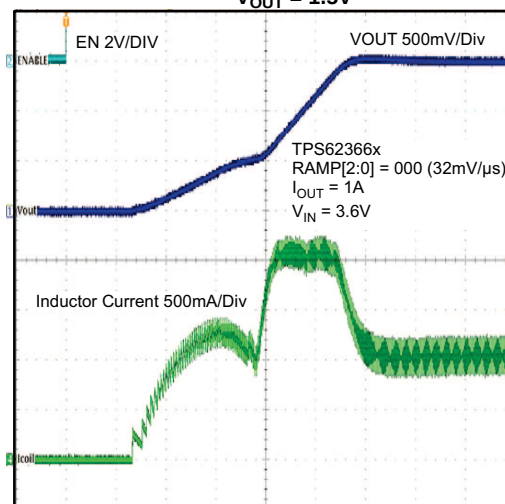


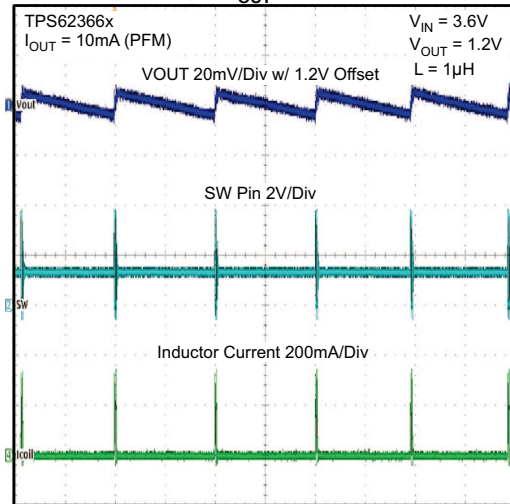
Figure 18.

G016

## TYPICAL CHARACTERISTICS (continued)

### SWITCHING WAVE FORMS

$I_{OUT} = 10\text{mA}$



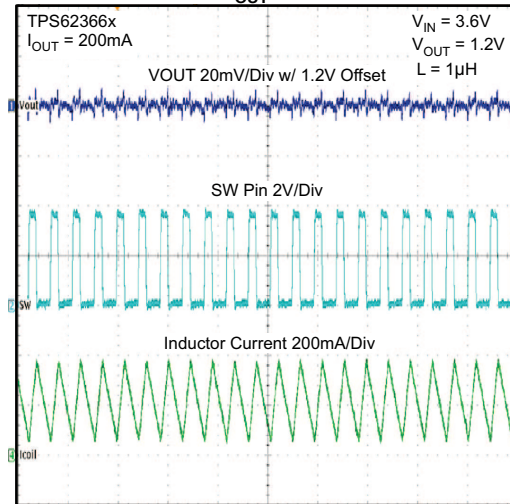
Time Base - 20 $\mu\text{s}$ /Div

G017

Figure 19.

### SWITCHING WAVE FORMS

$I_{OUT} = 200\text{mA}$



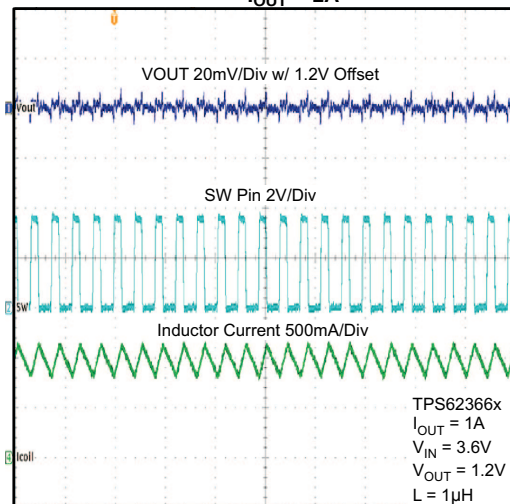
Time Base - 1 $\mu\text{s}$ /Div

G018

Figure 20.

### SWITCHING WAVE FORMS

$I_{OUT} = 1\text{A}$



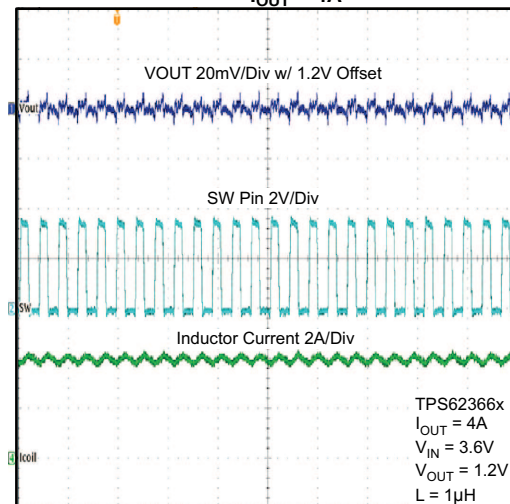
Time Base - 1 $\mu\text{s}$ /Div

G019

Figure 21.

### SWITCHING WAVE FORMS

$I_{OUT} = 4\text{A}$



Time Base - 1 $\mu\text{s}$ /Div

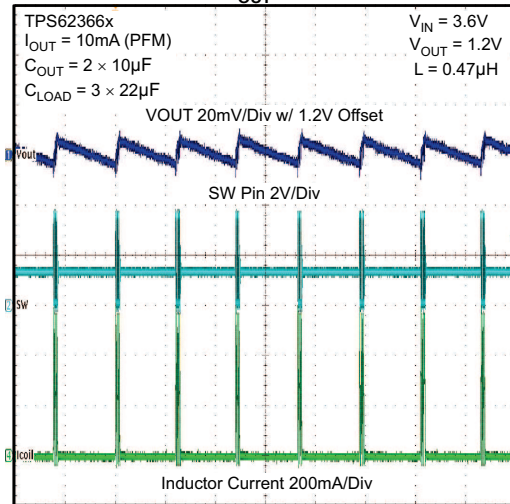
G020

Figure 22.

## TYPICAL CHARACTERISTICS (continued)

### SWITCHING WAVE FORMS

$I_{OUT} = 10\text{mA}$



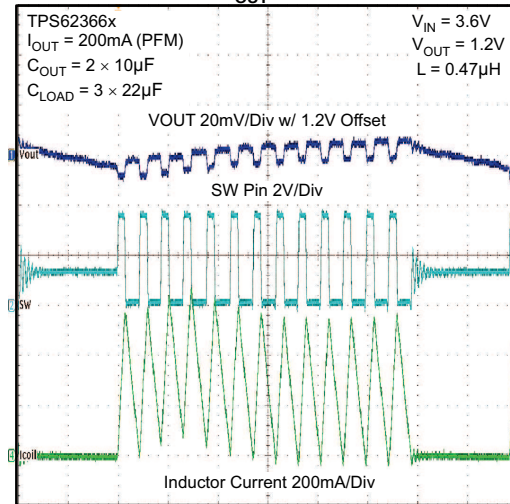
Time Base - 20µs/Div

Figure 23.

G037

### SWITCHING WAVE FORMS

$I_{OUT} = 200\text{mA}$



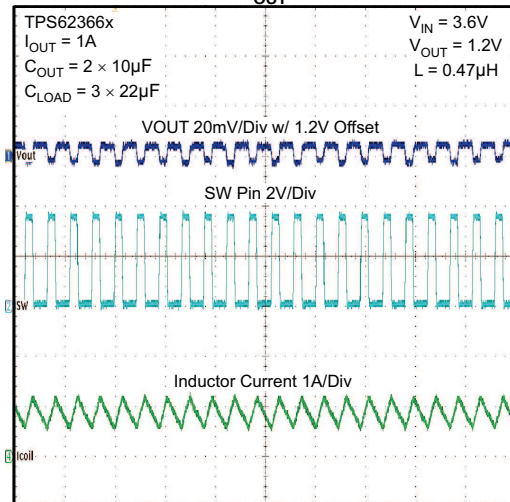
Time Base - 1µs/Div

Figure 24.

G038

### SWITCHING WAVE FORMS

$I_{OUT} = 1\text{A}$



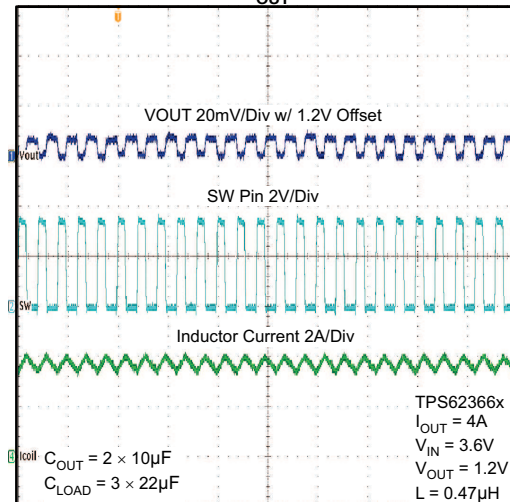
Time Base - 1µs/Div

Figure 25.

G039

### SWITCHING WAVE FORMS

$I_{OUT} = 4\text{A}$



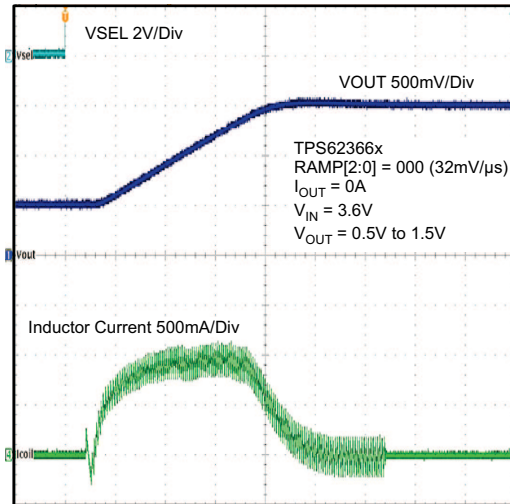
Time Base - 1µs/Div

Figure 26.

G040

## TYPICAL CHARACTERISTICS (continued)

### OUTPUT VOLTAGE RAMP CONTROL NO LOAD

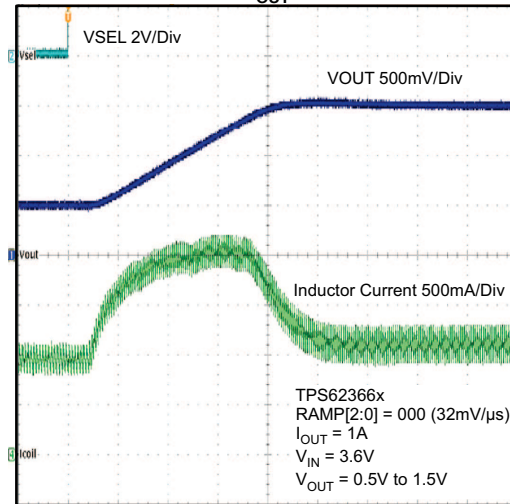


Time Base - 10µs/Div

G021

Figure 27.

### OUTPUT VOLTAGE RAMP CONTROL $I_{OUT} = 1A$

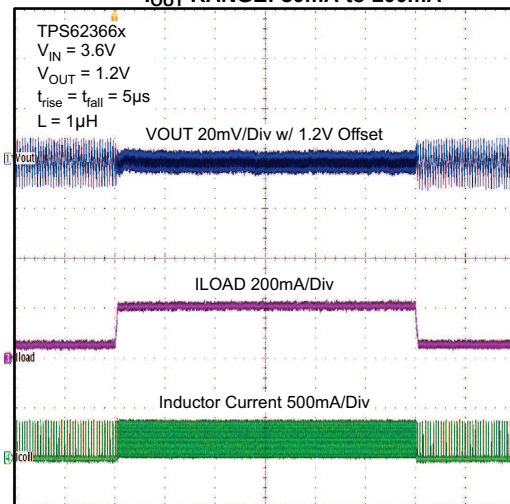


Time Base - 10µs/Div

G022

Figure 28.

### LOAD TRANSIENT RESPONSE $I_{OUT}$ RANGE: 50mA to 200mA

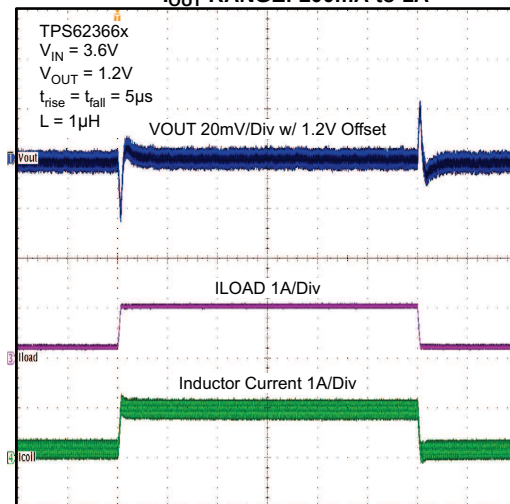


Time Base - 100µs/Div

G023

Figure 29.

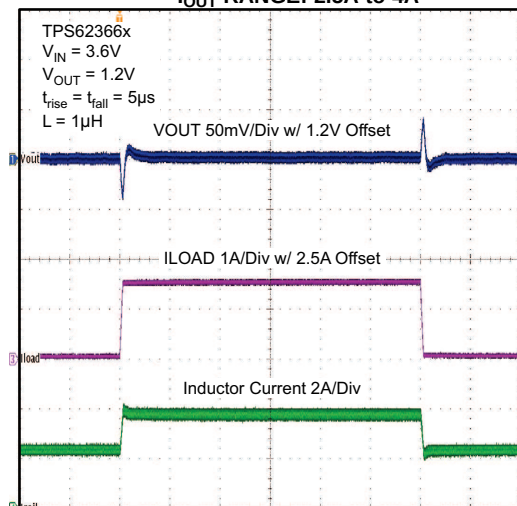
### LOAD TRANSIENT RESPONSE $I_{OUT}$ RANGE: 200mA to 1A



Time Base - 100µs/Div

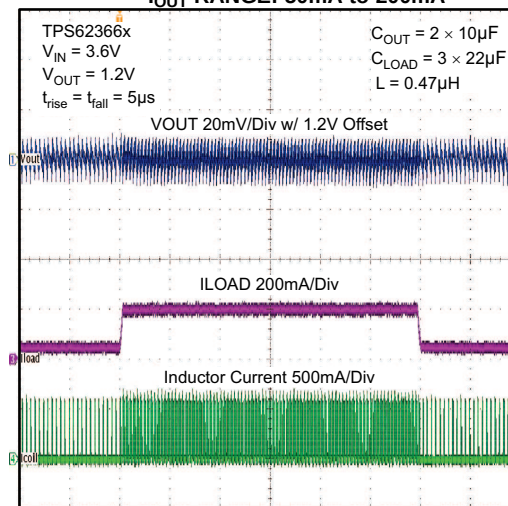
G024

Figure 30.

**TYPICAL CHARACTERISTICS (continued)****LOAD TRANSIENT RESPONSE****I<sub>OUT</sub> RANGE: 2.5A to 4A**

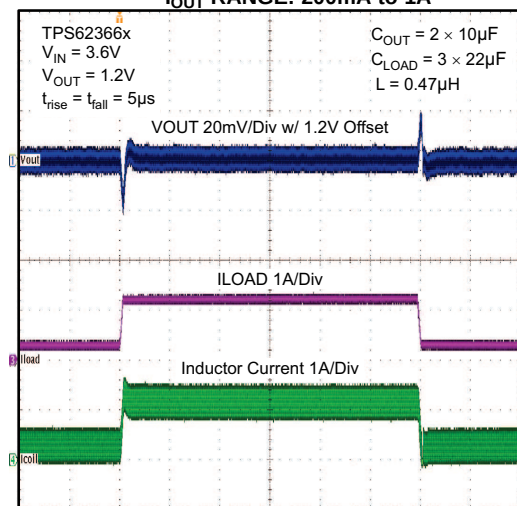
Time Base - 100µs/Div

G025

**Figure 31.****LOAD TRANSIENT RESPONSE****I<sub>OUT</sub> RANGE: 50mA to 200mA**

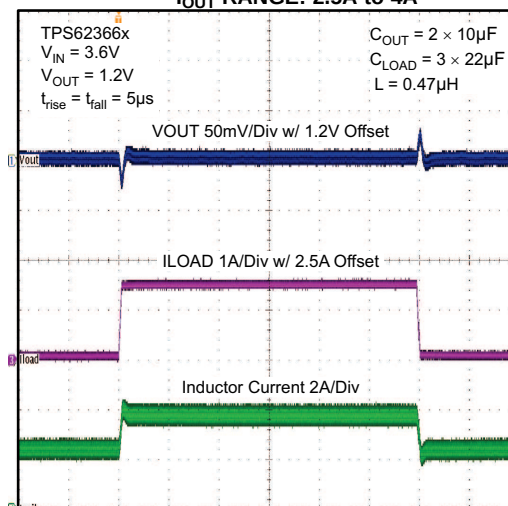
Time Base - 100µs/Div

G041

**Figure 32.****LOAD TRANSIENT RESPONSE****I<sub>OUT</sub> RANGE: 200mA to 1A**

Time Base - 100µs/Div

G042

**Figure 33.****LOAD TRANSIENT RESPONSE****I<sub>OUT</sub> RANGE: 2.5A to 4A**

Time Base - 100µs/Div

G043

**Figure 34.**

# TYPICAL CHARACTERISTICS (continued)

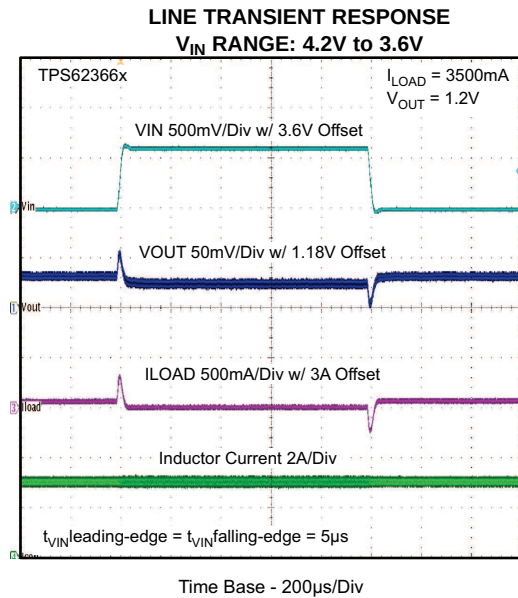


Figure 35.

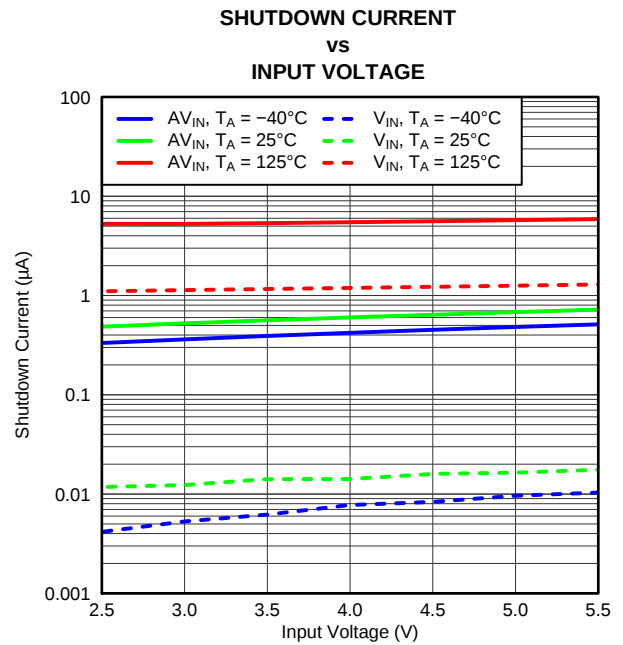


Figure 36.

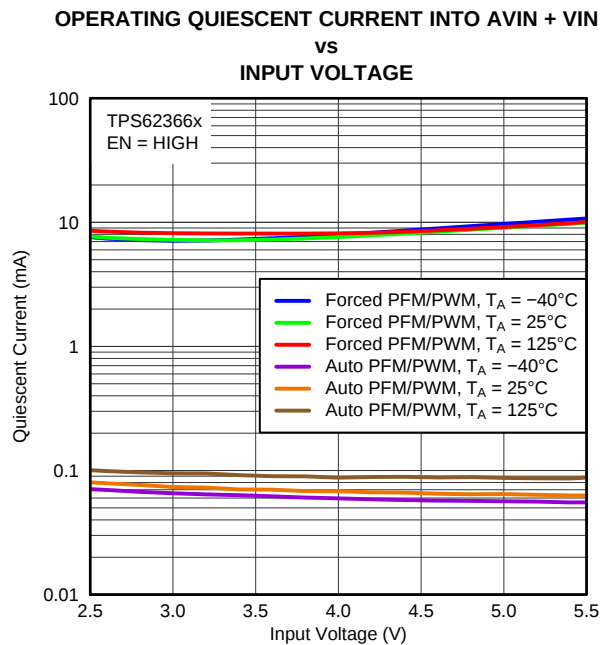


Figure 37.

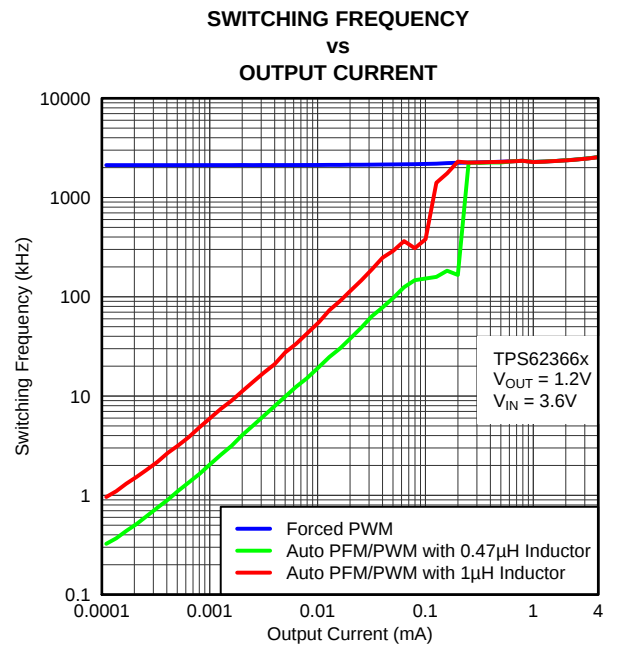


Figure 38.

## TYPICAL CHARACTERISTICS (continued)

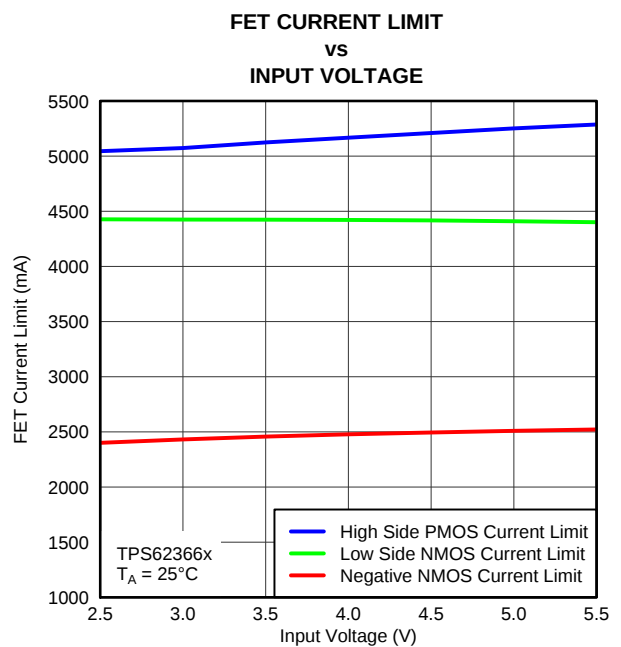


Figure 39.

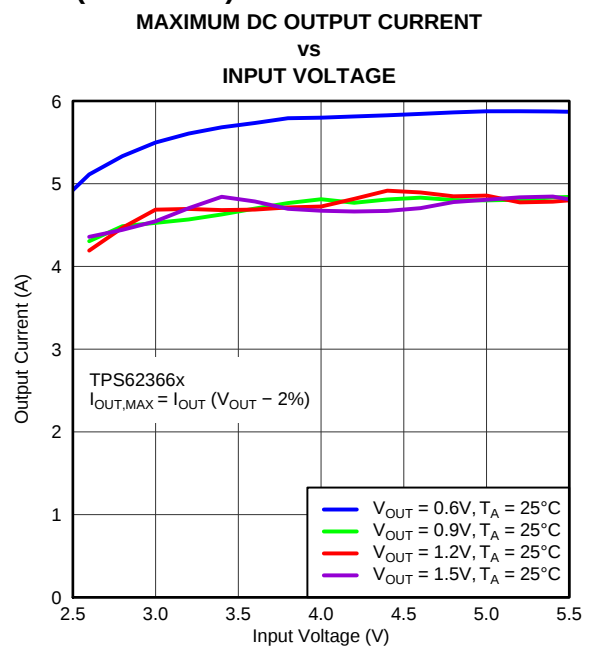
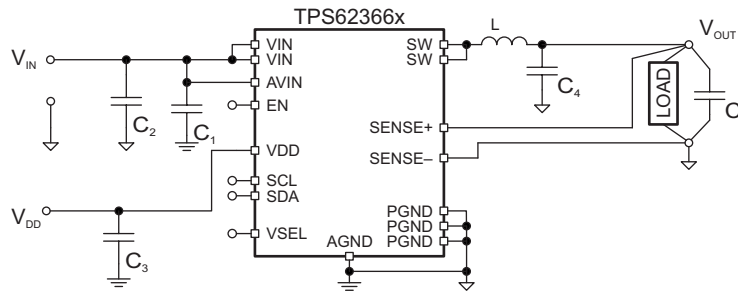


Figure 40.

## PARAMETER MEASUREMENT INFORMATION



**Table 2. List of Components**

| REFERENCE                       | DESCRIPTION                                                                                                    | MANUFACTURER                 | SETUP                                                                      |
|---------------------------------|----------------------------------------------------------------------------------------------------------------|------------------------------|----------------------------------------------------------------------------|
| TPS62366x                       | 4A Processor Supply with I <sup>2</sup> C Compatible Interface and Remote Sense, 2.076 mm x 2.076 mm x 0.625mm | Texas Instruments            | All Typical Characteristics<br>Figures 3-40                                |
| C <sub>1</sub> , C <sub>3</sub> | 0.1 $\mu$ F, Ceramic, 10V, X5R                                                                                 | Standard                     |                                                                            |
| C <sub>2</sub>                  | 10 $\mu$ F, Ceramic, 6.3V, X5R                                                                                 | Standard                     |                                                                            |
| L                               | 1 $\mu$ H, 4 mm x 4 mm x 2.1 mm                                                                                | Coilcraft (XFL4020-102ME1.0) | 1 $\mu$ H Setup:<br>Typical Characteristics<br>Figures 3-22, 27- 31, 36-40 |
| C <sub>4</sub>                  | 10 $\mu$ F, Ceramic, 6.3V, X5R                                                                                 | Standard                     |                                                                            |
| C <sub>L</sub>                  | Load Capacitors, 2x10 $\mu$ F + 4.7 $\mu$ F, Ceramic, 6.3V, X5R                                                | Standard                     |                                                                            |
| C <sub>4</sub>                  | 2 x 10 $\mu$ F, Ceramic, 6.3V, X5R                                                                             | Standard                     | 0.47 $\mu$ H Setup:<br>Typical Characteristics<br>Figures 23-26, 32-34     |
| C <sub>L</sub>                  | Load Capacitors, 3x22 $\mu$ F, Ceramic, 6.3V, X5R                                                              | Standard                     |                                                                            |
| L                               | 0.47 $\mu$ H, 4 mm x 4 mm x 1.5 mm                                                                             | Coilcraft (XFL4015-471MEC)   |                                                                            |

## DETAILED DESCRIPTION

The TPS62366x are a family of high-frequency synchronous step down dc-dc converter optimized for battery-powered portable applications. With an input voltage range of 2.5V to 5.5V, common battery technologies are supported.

The device provides up to 4A peak load current, operating at 2.5MHz typical switching frequency.

The devices convert to an output voltage range of 0.5V to 1.77V, programmable via I<sup>2</sup>C interface in 10mV steps.

The TPS62366x supports low-voltage DSPs and processor cores in smart-phones and handheld computers, including latest submicron processes and their retention modes and addresses digital voltage scaling technologies such as SmartReflex™.

Output Voltages and Modes can be fully programmed via I<sup>2</sup>C. To address different performance operating points and/or startup conditions, the device offers two output voltage / mode presets which can be chosen via a dedicated VSEL pin allowing simple and zero latency output voltage transition.

The devices focus on a high output voltage accuracy. The fully differential sensing and the DCS-Control™ architecture achieve precise static and dynamic, transient output voltage regulation. This accounts for stable processor operation. Output voltage security margins can be kept small, resulting in an increased overall system efficiency.

The TPS62366x devices offer high efficiency step down conversion. The area of highest efficiency is extended towards low output currents to increase the efficiency while the processor is operating in retention mode, as well as towards highest output currents reducing the power loss. This addresses the power profile of processors. High efficiency conversion is required for low output currents to support the retention modes of processors, resulting in an increased battery on-time. To address the processor maximum performance operating points with highest output currents, high efficiency conversion is enabled as well to save the battery on-time and reduce input power.

The robust architecture and multiple safety features allow perfect system integration.

The 2mm x 2mm package and the low number of required external components lead to a tiny solution size of approximately less than 25 mm<sup>2</sup>.

## OPERATION

The TPS62366x synchronous switched mode power converters are based on DCS-Control™, an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control architectures.

While a comparator stage provides excellent load transient response, an additional voltage loop ensures high DC accuracy as well. The TPS62366x compensates ground shifts at the load by the differentially sensing the output voltage at the point of load.

The internal ramp generator adds information about the load current and fast output voltage changes. The internally compensated regulation network achieves fast and stable operation with low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM mode it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5MHz with a controlled frequency variation depending on the input voltage. As the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to light loads. The transition from PWM to Power Save Mode is seamless and avoids output voltage transients.

The TPS62366x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

## ENABLING AND DISABLING THE DEVICE

The device is enabled by setting the EN input to a logic high. Accordingly, a logic low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the programmed threshold. The EN input must be terminated, unless the internal pull down resistor is activated.

The I<sup>2</sup>C interface is operable when VDD and AVIN are present, regardless of the state of the EN pin.

If the device is disabled by pulling the EN to a logic low, the output capacitor can actively be discharged. Per default, this feature is disabled. Programming the EN\_DISC bit to a logic high discharges the output capacitor via a typ. 300Ω path on the SENSE+ pin.

## SOFT START

The device incorporates an internal soft start circuitry that controls the ramp up of the output voltage after enabling the device. This circuitry eliminates inrush current to avoid excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

During soft start, the output voltage is monotonically ramped up to the minimum programmable output voltage. After reaching this threshold, the output voltage is further increased following the slope as programmed in the ramp rate settings (see [RAMP RATE CONTROLLING](#)) until reaching the programmed output voltage. Once the nominal voltage is reached, regular operation continues.

The device is able to start into a pre biased output capacitor as well.

## PROGRAMMING THE OUTPUT

The TPS62366x devices offer two similar registers to program the output. A dedicated hardware input pin (VSEL) is implemented for choosing the active register. The logic state of the VSEL pin selects the register whose settings are present at the output. The VSEL pin must be terminated, unless the internal pull-down resistor is activated.

The registers have a certain initial default value (see [Table 3](#)) and can be readjusted via I<sup>2</sup>C during operation.

This allows a simple transition between two output options by triggering the dedicated input pin. At the same time since the presets can be readjusted during operation, this offers highest flexibility.

**Table 3. Output Presets**

| VSEL PIN | PRESET | I <sup>2</sup> C REGISTER                                         | DEFAULT OPERATION MODE | DEFAULT OUTPUT VOLTAGE [V] |           |
|----------|--------|-------------------------------------------------------------------|------------------------|----------------------------|-----------|
|          |        |                                                                   |                        | TPS62366A                  | TPS62366B |
| 0        | SET0   | 0x00h – see <a href="#">Table 11</a> and <a href="#">Table 12</a> | Power Save Mode        | 1.20                       | 0.96      |
| 1        | SET1   | 0x01h – see <a href="#">Table 13</a> and <a href="#">Table 14</a> | Power Save Mode        | 1.16                       | 1.40      |

Via the I<sup>2</sup>C interface and/or the two preset options, the following output parameters can be changed:

- Output voltage from 0.5V to 1.77V with 10 mV granularity
- Mode of operation: Power Save Mode or forced PWM mode

The slope for transition between different output voltages (Ramp Rate) can be changed via I<sup>2</sup>C as well. The slope applies for all presets globally. See [RAMP RATE CONTROLLING](#) for further details.

Since the output parameters can be changed by a dedicated pin for selecting presets and by I<sup>2</sup>C, the following use scenarios are feasible:

- Control the device via VSEL pin only, after programming the presets, to choose and change within the programmed settings.
- Program via I<sup>2</sup>C only. The dedicated VSEL pin has a fixed connection. Changes are conducted by changing the preset values of the active register.
- Dedicated VSEL pin and I<sup>2</sup>C mixed operation. The non active preset might be changed. The VSEL pin is used for the transition to the new output condition. Changes within an active preset via I<sup>2</sup>C are feasible as well.

## DYNAMIC VOLTAGE SCALING

The output voltage can be adjusted dynamically. Each of the two output registers can be programmed individually by setting OV[6:0] in the SET0 and SET1 registers.

**Table 4. TPS62366x Output Voltage Settings for Registers SET0 and SET1**

| REGISTERS: SET0, SET1, SET2, SET3 |                |
|-----------------------------------|----------------|
| OV[D6:D0]                         | OUTPUT VOLTAGE |
| 000 0000                          | 500 mV         |
| 000 0001                          | 510 mV         |
| 000 0010                          | 520 mV         |
| 000 0011                          | 530 mV         |
| ...                               | ...            |
| 111 1101                          | 1750 mV        |
| 111 1110                          | 1760 mV        |
| 111 1111                          | 1770 mV        |

If the output voltage is changed at the active register (selected by the VSEL status), these changes apply after the I<sup>2</sup>C command is sent.

## POWER SAVE MODE AND FORCED PWM MODE

The TPS62366x devices feature a Power Save Mode to gain efficiency at light output current conditions. The device automatically transitions in both directions between pulse width modulation (PWM) operation at high load and pulse frequency modulation (PFM) operation at light load current. This maintains high efficiency at both light and heavy load currents. In PFM Mode, the device generates single switching pulses when required to maintain the programmed output voltage.

The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

The output current, at which the device transitions from PWM to PFM operation can be estimated as follows:

$$I_{OUT,TRANS} = \frac{V_{IN} - V_{OUT}}{2} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{(f \times L)} \quad (1)$$

With:

$V_{IN}$  = Input voltage

$V_{OUT}$  = Output Voltage

$f$  = Switching frequency, typ. 2.5 MHz

$L$  = Inductance (0.47uH - 1uH nominal)

The TPS62366x is optimized for low output voltage ripple. Therefore, the peak inductor current in PFM mode is kept small and can be calculated as follows:

$$I_{L,PFM,peak} = \frac{t_{ON}}{L} \times (V_{IN} - V_{OUT}) \quad (2)$$

And:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 350ns + 20ns \quad (3)$$

With:

$V_{IN}$  = Input Voltage

$V_{OUT}$  = Output Voltage

$t_{ON}$  = On-time of the High Side FET, from [Equation 3](#)

$L$  = Inductance

The TPS62366x offers a forced PWM mode as well. In this mode, the converter is forced in PWM mode even at light load currents. This comes with the benefit that the converter is operating with lower output voltage ripple. Compared to the PFM mode, the efficiency is lower during light load currents.

According to the output voltage, the Power Save Mode / forced PWM Mode can be programmed individually for each preset via I<sup>2</sup>C by setting the MODE0 and MODE1 bit D7. Table 3 shows the factory presets after enabling the I<sup>2</sup>C. For additional flexibility, the Power Save Mode can be changed at a preset that is currently active.

## RAMP RATE CONTROLLING

If the output voltage is changed, the TPS62366x actively controls the voltage ramp rate during the transition. An internal oscillator is embedded for high timing precision.

Figure 41 shows the operation principle. If the output voltage changes, the device changes the output voltage by adjusting through discrete steps with a programmable ramp rate resulting in a corresponding transition time. The connected output capacitor flattens the steps.

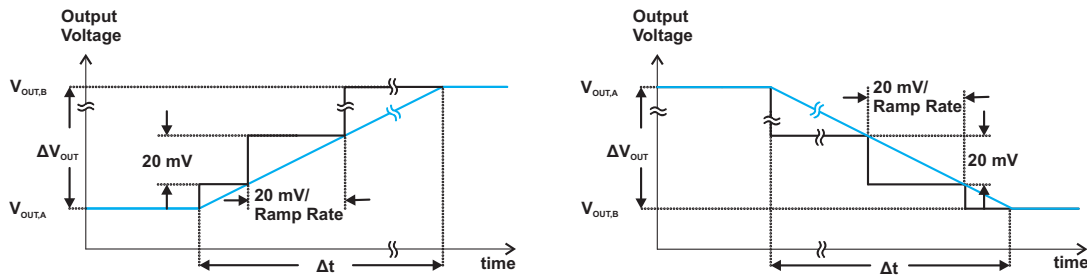


Figure 41. Ramp Up and Down

The ramp up/down slope can be programmed via I<sup>2</sup>C interface (see Table 5).

Table 5. Ramp Rates

| RMP [2:0] | RAMP RATE |           |
|-----------|-----------|-----------|
|           | [mV/μs]   | [μs/10mV] |
| 000       | 32        | 0.3125    |
| 001       | 16        | 0.625     |
| 010       | 8         | 1.25      |
| 011       | 4         | 2.5       |
| 100       | 2         | 5         |
| 101       | 1         | 10        |
| 110       | 0.5       | 20        |
| 111       | 0.25      | 40        |

For a transition of the output voltage from V<sub>OUT,A</sub> to V<sub>OUT,B</sub> and vice versa, the resulting ramp up/down slope can be calculated as

$$\frac{\Delta V_{OUT}}{\Delta t} = 32 \frac{\text{mV}}{\mu\text{s}} \frac{1}{2^{(RMP[2:0])_2}} \quad (4)$$

If the device is operating in forced PWM Mode, the device actively controls both the ramp up and down slope.

If Power Save Mode is activated, the ramp up phase follows the programmed slope.

To force the output voltage to follow the ramp down slope in Power Save Mode, the RAMP\_PFM bit needs to be set. This forces the converter to follow the ramp down slope during PFM operation as well.

If the RAMP\_PFM bit is not set in Power Save Mode, the slope can be less at low output currents since the device does not actively source energy back from the output capacitor to the input or it might be sharper at high output currents since the output capacitor is discharged quickly.

The TPS62366x ramps taking 20mV steps with a final 10mV step, if required, for reaching the target output voltage.

While the output voltage setpoint is changed in a digital stair step fashion, the output voltage change is linear due to the output capacitor whose voltage cannot change instantaneously.

## SAFE OPERATION AND PROTECTION FEATURES

### Inductor Current Limit

The inductor current limiting prevents the device from drawing high inductor current and excessive current from the battery. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current while the high side power MOSFET is turned on. Once the current limit is tripped, the high side MOSFET is turned off and the low side MOSFET is turned on to ramp down the inductor current. This prevents high currents to be drawn from the battery.

Once the low side MOSFET is on, the low side forward current limit keeps the low side MOSFET on until the current through it decreases below the low side forward current limit threshold.

The negative current limit acts if current is flowing back to the battery from the output. It works differently in PWM and PFM operation. In PWM operation, the negative current limit prevents excessive current from flowing back through the inductor to the battery, preventing abnormal voltage conditions at the switching node. In PFM operation, a zero current limits any power flow back to the battery by preventing negative inductor current.

### Die Temperature Monitoring and Over Temperature Protection

The TPS62366x offers two stages of die temperature monitoring and protection.

The Early Warning Monitoring Feature monitors the device temperature and provides the host an indication that the die temperature is in the higher range. If the device's junction temperature,  $T_J$ , exceeds 120°C typical, the TJEW bit is set high. To avoid the thermal shutdown being triggered, the current drawn from the TPS62366x should be reduced at this early stage.

The Over Temperature Protection feature disables the device if the temperature increases due to heavy load and/or high ambient temperature. It monitors the device die temperature and, if required, triggers the device into shutdown until the die temperature falls sufficiently.

If the junction temperature,  $T_J$ , exceeds 150°C typical, the device goes into thermal shutdown. In this mode, the power stage is turned off. During thermal shutdown, the I<sup>2</sup>C interface remains operable. All register values are kept.

For the thermal shutdown, a hysteresis of 20°C typical is implemented allowing the device to cool after the shutdown is triggered. Once the junction temperature  $T_J$  cools down to 130°C typical, the device resumes operation.

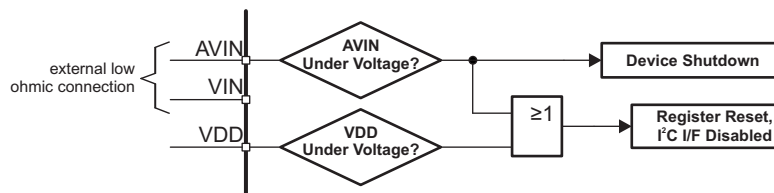
If a thermal shutdown has occurred, the TJTS bit is latched and remains a logic high as long as VDD and AVIN are present and until the bit is reset by the host.

### Input Under Voltage Protection

The input under voltage protection is implemented in order to prevent operation of the device for low input voltage conditions. If the device is enabled, it prevents the device from switching if AVIN falls below the under voltage lock out threshold. If the AVIN under voltage protection threshold is tripped, the device goes into under voltage shutdown instantaneously, turning the power stage off and resetting all internal registers. The input under voltage protection is also implemented on the VDD input. If the VDD under voltage protection threshold is tripped, the device resets all internal registers.

A under voltage lock out hysteresis of  $V_{UVLO,HYST(AVIN)}$  at AVIN and  $V_{UVLO,HYST(VDD)}$  at VDD is implemented.

The I<sup>2</sup>C compatible interface remains fully functional if AVIN and VDD are present. If the under voltage lock out of AVIN or VDD is triggered during operation, all internal registers are reset to their default values. [Figure 42](#) shows the UVLO block diagram.



**Figure 42. UVLO State Chart**

By connecting VIN and AVIN to the same potential, VIN is included in the under voltage monitoring. If a low pass input filter is applied at AVIN (not mandatory for the TPS62366x), the delay and shift in the voltage level can be calculated by taking the typical quiescent current  $I_Q$  at AVIN. As an example, for  $I_Q$  and 10Ω series resistance, this results in a minimal static shift of approx. 560μV.

VIN and AVIN must be connected to the same source for proper device operation.

## APPLICATION INFORMATION

### I<sup>2</sup>C INTERFACE

#### Serial Interface Description

I<sup>2</sup>C is a 2-wire serial interface developed by Philips Semiconductor (see I<sup>2</sup>C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C compatible devices connect to the I<sup>2</sup>C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a micro controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

The TPS62366x device works as a *slave* and supports the following data transfer *modes*, as defined in the I<sup>2</sup>C-Bus Specification:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode plus (1Mbps)
- High-speed mode (3.4 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as VDD and AVIN are present in the specified range. Tripping the under voltage lock out of AVIN or VDD deletes the registers and establishes the default values once the supply is present again.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS62366x device supports 7-bit addressing. 10-bit addressing and general call addressing are not supported.

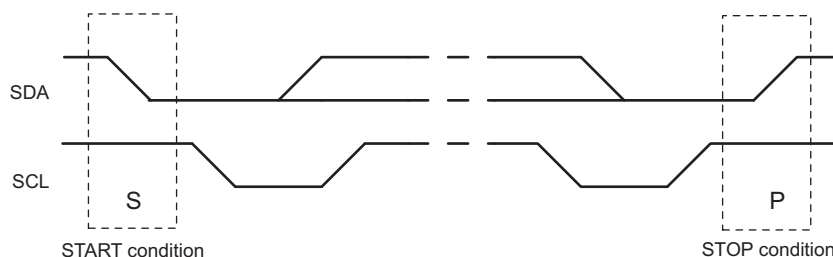
Table 6 shows the TPS62366x devices and their assigned I<sup>2</sup>C addresses.

**Table 6. I<sup>2</sup>C Address**

| DEVICE OPTION | I <sup>2</sup> C ADDRESS |                         |
|---------------|--------------------------|-------------------------|
|               | HEXADECIMAL CODED        | BINARY CODED            |
| TPS62366A     | (0x60) <sub>HEX</sub>    | (110 0000) <sub>2</sub> |
| TPS62366B     | (0x60) <sub>HEX</sub>    | (110 0000) <sub>2</sub> |

#### F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 43. All I<sup>2</sup>C-compatible devices should recognize a start condition.



**Figure 43. START and STOP Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 44). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 45) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

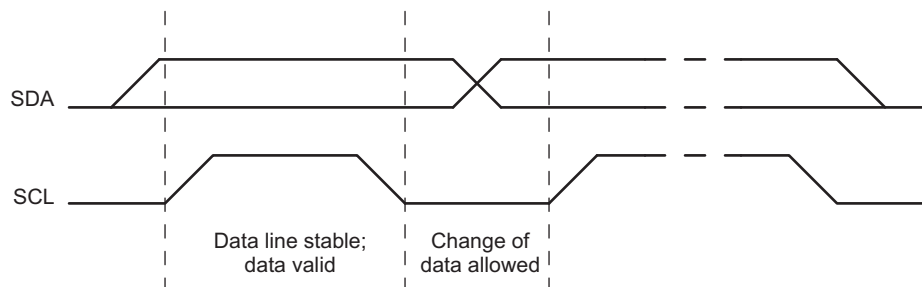


Figure 44. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 43). This releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

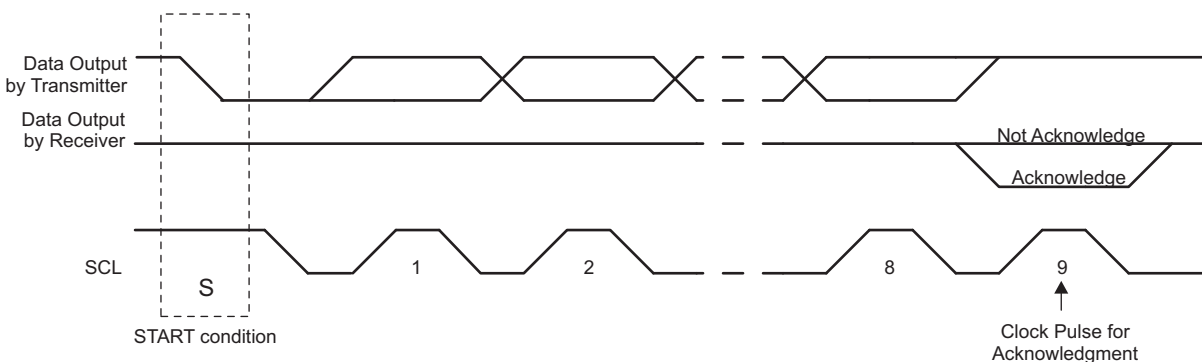


Figure 45. Acknowledge on the I<sup>2</sup>C Bus

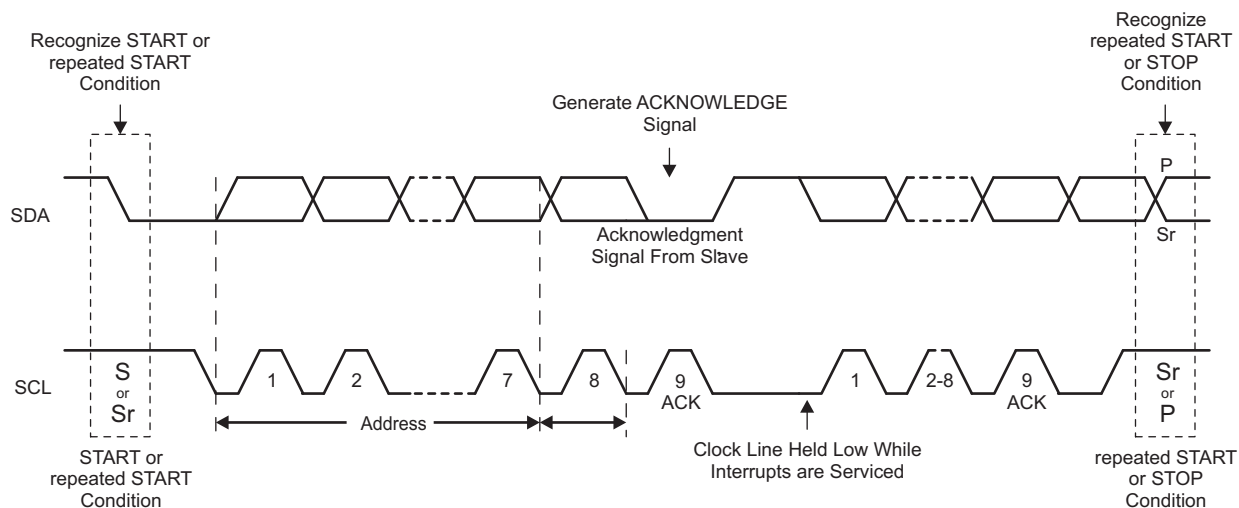


Figure 46. Bus Protocol

### HS-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

### I<sup>2</sup>C UPDATE SEQUENCE

The TPS62366x requires a start condition, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the TPS62366x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the TPS62366x. The TPS62366x performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

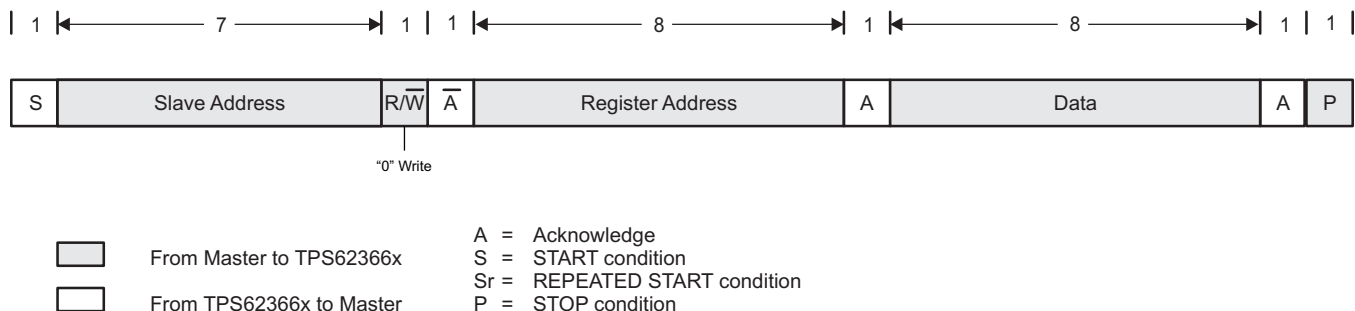


Figure 47. Write Data Transfer Format in F/S-Mode

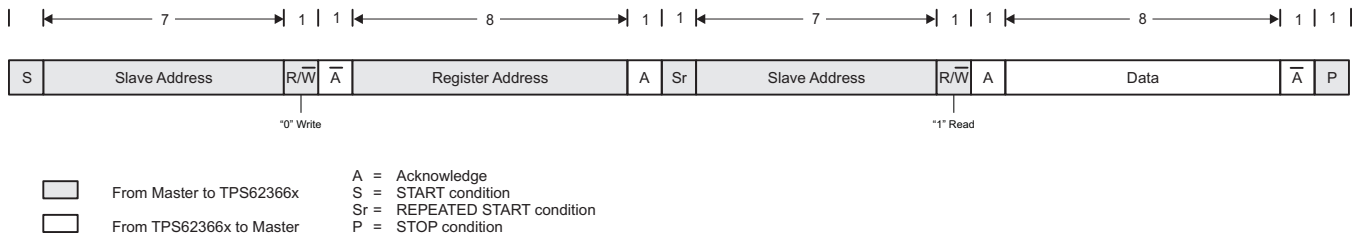


Figure 48. Read Data Transfer Format in F/S-Mode

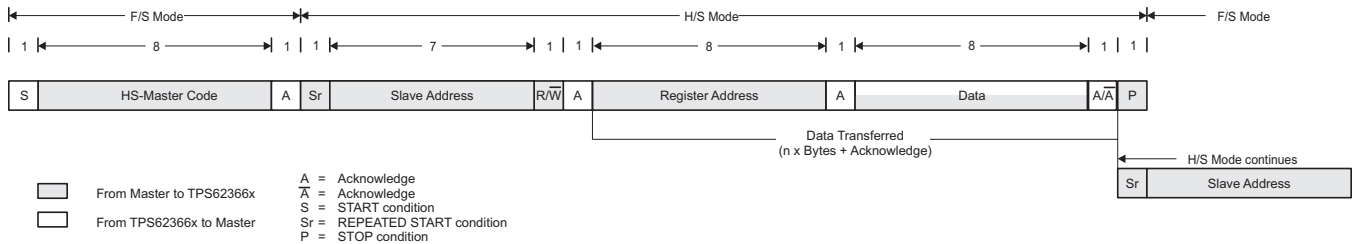


Figure 49. Data Transfer Format in H/S-Mode

## Slave Address Byte

| MSB |   |   |   |   |   |    | LSB |
|-----|---|---|---|---|---|----|-----|
| X   | X | X | X | X | X | A1 | A0  |

The slave address byte is the first byte received following the START condition from the master device.

## Register Address Byte

| MSB |   |   |   |   |    |    | LSB |
|-----|---|---|---|---|----|----|-----|
| 0   | 0 | 0 | 0 | 0 | D2 | D1 | D0  |

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPS62366x, which contains the address of the register to be accessed.

## I<sup>2</sup>C REGISTER RESET

The I<sup>2</sup>C registers can be reset by pulling VDD below the VDD Under Voltage Level,  $V_{DD,UVLO}$ . VDD can be used as a hardware reset function to reset the registers to defaults, if VDD is supplied by a GPIO of the host. The host's GPIO must be capable of driving  $I_{VDD,max}$ .

Refer to the [Input Under Voltage Protection](#) section for details.

## PULL DOWN RESISTORS

The EN and VSEL inputs feature internal pull down resistors to discharge the potential if one of the pins is not connected or is triggered by a high impedance source. See [Figure 50](#). By default, the pull down resistors are enabled.

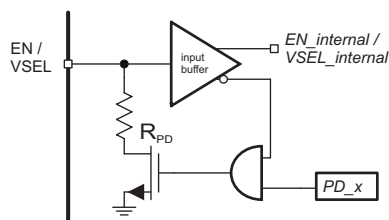


Figure 50. Pull Down Resistors at EN and VSEL pins

If a pin is read as a logic HIGH, its pull down resistor is disconnected dynamically to reduce power consumption.

To achieve lowest possible quiescent current or if external pull up/down resistors are employed, the internal pull down resistors can be disabled individually at EN and VSEL by I<sup>2</sup>C programming the registers PD\_EN and PD\_VSEL.

## INPUT CAPACITOR SELECTION

The input capacitor is required to buffer the pulsing current drawn by the device at VIN and reducing the input voltage ripple. The pulsing current is originated by the operation principles of a step down converter.

Low ESR input capacitors are required for best input voltage filtering and minimal interference with other system components. For best performance, ceramic capacitors with a low ESR at the switching frequency are recommended. X7R or X5R type capacitors should be used.

A ceramic input capacitor in the nominal range of C<sub>IN</sub> = 4.7μF to 22μF should be a good choice for most application scenarios. In general, there is no upper limit for increasing the input capacitor.

For typical operation, a 10μF X5R type capacitor is recommended. [Table 7](#) shows a list of recommended capacitors.

**Table 7. List of Recommended Capacitors**

| CAPACITANCE<br>[μF] | TYPE            | DIMENSIONS<br>L x W x H [mm <sup>3</sup> ] | MANUFACTURER |
|---------------------|-----------------|--------------------------------------------|--------------|
| 10                  | GRM188R60J106M  | 0603: 1.6 x 0.8 x 0.8                      | Murata       |
| 10                  | CL10A106MQ8NRNC | 0603: 1.6 x 0.8 x 0.8                      | Samsung      |
| 22                  | GRM188R60G226M  | 0603: 1.6 x 0.8 x 0.8                      | Murata       |
| 22                  | CL10A106MQ8NRNC | 0603: 1.6 x 0.8 x 0.8                      | Samsung      |

## DECOUPLING CAPACITORS AT AVIN, VDD

Noise impacts can be reduced by buffering AVIN and VDD with a decoupling capacitor. It is recommended to buffer AVIN and VDD with a X5R or X7R ceramic capacitor of at least 0.1μF connected between AVIN, AGND and VDD, AGND respectively. The capacitor closest to the pin should be kept small (< 0.22μF) in order to keep a low impedance at high frequencies. In general, there is no upper limit for the total capacitance.

## INDUCTOR SELECTION

The choice of the inductor type and value has an impact on the inductor ripple current, the transition point of PFM to PWM operation, the output voltage ripple and accuracy. The subsections below support for choosing the proper inductor.

### Inductance Value

The TPS62366x is designed for best operation with a nominal inductance value of 1μH.

Inductances down to 0.47μH nominal may be used to improve the load transient behavior or to decrease the total solution size. See [OUTPUT FILTER DESIGN](#) for details.

Depending on the inductance, using inductances lower than 1μH results in a higher inductor current ripple. It can be calculated as:

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (5)$$

With:

V<sub>IN</sub> = Input Voltage

V<sub>OUT</sub> = Output Voltage

f = Switching frequency, typ. 2.5MHz

L = Inductance

## Inductor Saturation Current

The inductor needs to be selected for its current rating. To pick the proper saturation current rating, the maximum inductor current can be calculated as:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (6)$$

With:

$\Delta I_L$  = Inductor ripple current (see [Equation 5](#))

$I_{OUT,MAX}$  = Maximum output current

Since the inductance can be decreased by saturation effects and temperature impact, the inductor needs to be chosen to have an effective inductance of at least 0.3μH under temperature and saturation effects.

[Table 8](#) shows a list of inductors that have been used with the TPS62366x. Special care needs to be taken for choosing the proper inductor, taking e.g. the load profile into account.

**Table 8. List of Recommended Inductors**

| INDUCTANCE<br>[μH] | SATURATION<br>CURRENT<br>RATING <sup>(1)</sup><br>( $\Delta I/L = 30\%$ ,<br>typ)<br>[A] | TEMPERATURE<br>CURRENT<br>RATING <sup>(1)</sup><br>( $\Delta T = 40^\circ\text{C}$ , typ)<br>[A] | DIMENSIONS<br>L x W x H<br>[mm <sup>3</sup> ] | DC<br>RESISTANCE<br>[mΩ typ] | TYPE                                   | MANUFACTURER |
|--------------------|------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------------------------------------|------------------------------|----------------------------------------|--------------|
| 1.0                | 5.4                                                                                      | 11.0                                                                                             | 4.0 x 4.0 x 2.1                               | 11                           | XFL4020-102ME1.0                       | Coilcraft    |
| 1.0                | 4.7                                                                                      | 3.6                                                                                              | 3.2 x 2.5 x 1.2                               | 34                           | DFE322512C                             | Toko         |
| 1.0                | 6.0                                                                                      | 4.1                                                                                              | 4.4 x 4.1 x 1.2                               | 38                           | SPM4012                                | TDK          |
| 1.0                | 4.7                                                                                      | 3.8                                                                                              | 3.2 x 2.5 x 1.2                               | 35                           | PILE32251B-<br>1R0MS-11 <sup>(2)</sup> | Cyntec       |
| 1.0                | 4.5                                                                                      | 7.0                                                                                              | 4.15 x 4.0 x 1.8                              | 24                           | PIMB042T-1R0MS-<br>11                  | Cyntec       |
| 1.0                | 4.2                                                                                      | 3.7                                                                                              | 2.5 x 2.0 x 1.2                               | 38                           | DFE252012R -H-<br>1R0N <sup>(2)</sup>  | Toko         |
| 0.47               | 6.6                                                                                      | 11.2                                                                                             | 4.0 x 4.0 x 1.5                               | 8                            | XFL4015-471M                           | Coilcraft    |
| 0.47               | 5                                                                                        | 4.5                                                                                              | 2.5 x 2.0 x 1.2                               | 23                           | PIFE25201B-<br>R47MS-11 <sup>(2)</sup> | Cyntec       |
| 0.47               | 5.2                                                                                      | 4.4                                                                                              | 2.5 x 2.0 x 1.2                               | 27                           | DFE252012R -H-<br>R47N <sup>(3)</sup>  | Toko         |

(1) Excessive inductor temperature might result in a further effective inductance drop which might be below or close to the max. current limit threshold,  $I_{LIM,max}$ , depending on the inductor, use case and thermal board design. Proper saturation current rating must be verified, taking into account the use scenario and thermal board layout.

(2) Product preview, release planned for Q3/4 2012. Contact manufacturer for details.

(3) Under development, typ. data might change. Contact manufacturer for schedule and details.

## OUTPUT CAPACITOR SELECTION

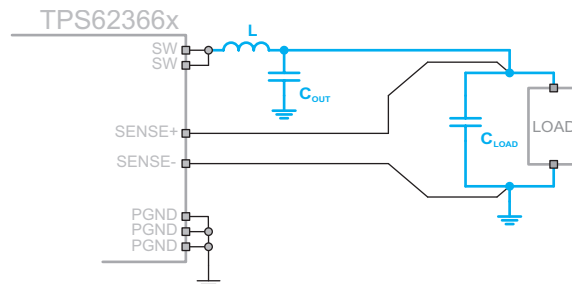
The unique hysteretic control scheme allows the use of tiny ceramic capacitors. For best performance, ceramic capacitors with low ESR values are recommended to achieve high conversion efficiency and low output voltage ripple. For stable operation, X7R or X5R type capacitors are recommended.

The TPS62366x is designed to operate with a minimum output capacitor of 10μF for a 1μH inductor and 2x10μF for a 0.47μH inductor, placed at the device's output. In addition, a 0.1μF capacitor can be added to the output to reduce the high frequency content created by a very sudden load change. For stability, an overall maximum output capacitance must not be exceeded. See [OUTPUT FILTER DESIGN](#).

[Table 7](#) shows a list of tested capacitors. The TPS62366x is not designed for use with polymer, tantalum, or electrolytic output capacitors.

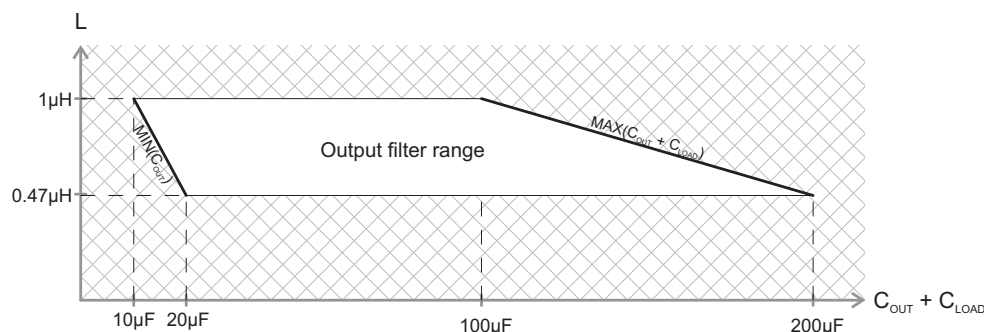
## OUTPUT FILTER DESIGN

The inductor and the output capacitors create the output filter. The output capacitors consist of  $C_{OUT}$  and buffer capacitors at the load,  $C_{LOAD}$ . See [Figure 51](#). Buffering the load by ceramic capacitors,  $C_{LOAD}$ , improves the voltage quality at the load input and the dynamic load step behavior. This is especially true if the trace between the TPS62366x and the load is longer than the smallest possible.



**Figure 51. L,  $C_{OUT}$  and  $C_{LOAD}$  Forming the Output Filter**

Depending on the chosen inductor value, a certain minimum output capacitor  $C_{OUT}$  must be present. Also depending on the chosen inductor value, a maximum output and buffer capacitor configuration ( $C_{OUT} + C_{LOAD}$ ) must not be exceeded. [Figure 52](#) shows the range of L,  $C_{OUT}$  and  $C_{LOAD}$  that create a stable output filter.



**Figure 52. Recommended L,  $C_{OUT}$  and  $C_{LOAD}$  Combinations**

Within the allowed output filter range, a certain filter can be chosen to improve further on application specific key parameters.

The choice of the inductance, L, affects the inductor current ripple, output voltage ripple, the PFM to PWM transition point and the PFM operation switching frequency.

The TPS62366x is designed for operation with a nominal inductance value of 1  $\mu$ H. Inductances down to 0.47  $\mu$ H nominal may be used to improve the load transient behavior (see [Figure 31](#) and [Figure 34](#)) or to decrease the total solution size. This increases the inductor current ripple (see [Equation 5](#)). As a consequence, the output voltage ripple is increased if the output capacitance is kept constant. The increased inductor ripple current also causes higher peak inductor currents (see [Equation 6](#)), requiring a higher saturation current rating. Furthermore, the PFM switching frequency is decreased (see [Figure 38](#)) and the automatic PFM to PWM transition occurs at a higher output current (see [Equation 1](#)).

The choice of the output and buffer capacitance ( $C_{OUT}$  and  $C_{LOAD}$ ) affects the load step behavior, output voltage ripple, PFM switching frequency and output voltage transition time.

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreasing the PFM switching frequency. For very large output filter combinations, the output voltage might be slower than the programmed ramp rate at voltage transitions (see [RAMP RATE CONTROLLING](#)) because of the higher energy stored on the output capacitance. At startup, the time required to charge the output capacitor to 0.5V might be longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor (see [ENABLING AND DISABLING THE DEVICE](#)), this requires more time to settle  $V_{OUT}$  down as a consequence of the increased time constant  $\tau = R_{DISCHARGE} \times (C_{OUT} + C_{LOAD})$ .

For further performance or specific demands, these values might be tweaked. In any case, the loop stability should be checked since the control loop stability might be affected. At light loads, if the device is operating in PFM Mode, choosing a higher value minimizes the voltage ripple resulting in a better DC output accuracy.

## THERMAL AND DEVICE LIFETIME INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different layers. Proper This results in reduced junction-to-ambient ( $\theta_{JA}$ ) and junction-to-board ( $\theta_{JB}$ ) thermal resistances and thereby reduces the device junction temperature,  $T_J$ .

The TI reliability requirement for the silicon chip's life time (100K Power-On-Hours at  $T_J = 105^\circ\text{C}$ ) is affected by the junction temperature and the continuously drawn output current. In order to be consistent with the TI reliability requirement for the silicon chips (100000 Power-On-Hours at  $T_J = 105^\circ\text{C}$ ), the average output current  $I_{OUT,avg}$  should not continuously exceed 2550mA so as to prevent electromigration failure in the SW pins solder bumps.

Exceeding  $I_{OUT,avg}$  and/or  $T_{J,max}$  might affect the device reliability by electromigration. Electromigration is a physical effect of wafer chip scale packages in general, being a first order function of DC current and temperature.

Refer to the application note [TPS62366x Thermal and Device Lifetime Information \(SLVA525\)](#) for detailed information.

For more details on how to use the thermal parameters, see the application notes: [Thermal Characteristics Application Note \(SZZA017\)](#), and [IC Package Thermal Metrics Application Note \(SPRA953\)](#).

## PCB LAYOUT

The PCB layout is an important step to maintain the high performance of the TPS62366x. Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the TPS62366x through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency.

### Signal Routing Strategy

The TPS62366x is a mixed signal IC. Depending on the function of a pin or trace, different board layout strategies must be addressed to achieve a good design. Due to the nature of a switching converter, some signals are sensitive to influence from other signals (aggressors). The sense lines, SENSE+ and SENSE-, are sensitive to the aggressors, which are high bandwidth I/O pins (SCL and SDA) and the switch node (SW) and their connected traces. Special care must be taken to avoid cross-talk between them.

The following recommendations need to be followed:

- PGND, VIN and SW should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND, VIN and SW. They create a flux which is determined by the switching frequency. The flux generated affects neighboring layers due to capacitive coupling across layers.
- AGND, AVIN and VDD must be isolated from noisy signals.
- If crossing layers is required for PGND, VIN and SW, they must be dimensioned to support the high currents to not cause high IR drops. In general, changing the layers frequently must be avoided.
- Signal traces, and especially the sense lines (SENSE+ and SENSE-), must be kept away from noisy traces/signals. Avoid capacitive coupling with neighboring noisy layers by cutting away the overlapping areas close to signal traces. Special care must be taken for the sense lines to avoid inductive / capacitive cross-talk from aggressors, both from noisy lines as well as the external inductor which generates a magnetic field.
- Care should be taken for a proper thermal layout. Wide traces, connecting with vias through the layers, provides a proper thermal path to sink the heat energy created from the device and inductor.

## External Components Placement

The input capacitor at VIN must be placed closest to the IC for proper operation. The decoupling caps at AVIN and VDD reduce noise impacts and should be placed as close to the IC as possible. The output filter, consisting of  $C_{OUT}$  and L, converts the switching signal at SW to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior.

## Trace routing

Route the VIN trace wide and thick to avoid IR drops. The trace between the input capacitor's higher node and VIN as well as the trace between the input capacitor's lower node and PGND must be kept as short as possible. Parasitic inductance on these traces must be kept as tiny as possible for proper device operation.

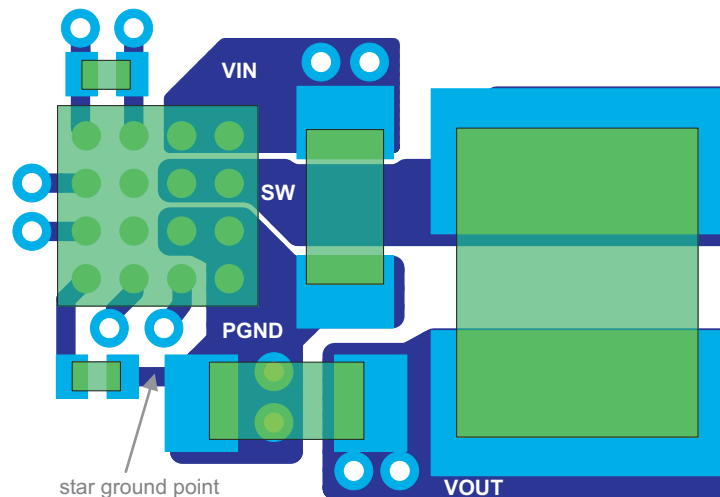
AVIN and AGND should be isolated from noisy signals. Route AGND to the star ground point where no IR drop occurs. The input cap at AVIN isolates noise. Proceed with VDD and AGND in a similar manner.

The switch node trace, SW, must connect directly to the inductor followed by the output capacitors,  $C_{OUT}$ . The switch node is an aggressor. Keeping this trace short reduces noise being radiated and improves EMI behavior. The lower node of the output capacitor,  $C_{OUT}$ , needs to connect to the star ground point. The TPS62366x supports the point of load concept (POL). Input caps at the POL do not need to be placed closest to the IC; they should be placed close to the POL. Route the traces between the TPS62366x's output capacitor and the load's input capacitors direct and wide to avoid losses due to the IR drop.

Connect the sense lines to the POL. This puts into practice the remote sensing concept, allowing the device to regulate the voltage at the POL, compensating IR drops. If possible, make a Kelvin connection to the load device. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND, VIN, and SW, as well as high bandwidth signals such as the I<sup>2</sup>C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.

The PGND nodes at  $C_{IN}$  and  $C_{OUT}$  can be connected underneath the IC at the PGND pins (star point). Make sure that small signal traces returning to the AGND do not share the high current path at PGND to  $C_{IN}$  and  $C_{OUT}$ .

See [Figure 53](#) for the recommended layout.



**Figure 53. Layout Suggestion (top view) with 3225 inductor. Overall Solution Size: 27.5mm<sup>2</sup>**

## REGISTER SETTINGS

### Overview

**Table 9. TPS62366A Register Settings Overview**

| ADDRESS | REGISTER   | RESET /<br>DEFAULT<br>STATE | READ /<br>WRITE | REGISTER (default / reset values) |          |    |    |    |         |          |      |
|---------|------------|-----------------------------|-----------------|-----------------------------------|----------|----|----|----|---------|----------|------|
|         |            |                             |                 | MSB                               |          |    |    |    |         |          | LSB  |
|         |            |                             |                 | D7                                | D6       | D5 | D4 | D3 | D2      | D1       | D0   |
| 0x00h   | SET0       | 0100 0110                   | R/W             | MODE0                             | OV0[6:0] |    |    |    |         |          |      |
| 0x01h   | SET1       | 0100 0010                   | R/W             | MODE1                             | OV1[6:0] |    |    |    |         |          |      |
| 0x02h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x03h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x04h   | Ctrl       | 11xx xxxx                   | R/W             | PD_EN                             | PD_VSEL  |    |    |    |         |          |      |
| 0x05h   | Temp       | xxxx x000                   | R/W             |                                   |          |    |    |    | DIS_TS  | TJEW     | TJTS |
| 0x06h   | RmpCtrl    | 000x x00x                   | R/W             | RMP[2:0]                          |          |    |    |    | EN_DISC | RAMP_PFM |      |
| 0x07h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x08h   | Chip_ID    | 1001 00xx                   | R               |                                   |          |    |    |    |         |          |      |
| 0x09h   | Chip_ID    |                             |                 |                                   |          |    |    |    |         |          |      |

**Table 10. TPS62366B Register Settings Overview**

| ADDRESS | REGISTER   | RESET /<br>DEFAULT<br>STATE | READ /<br>WRITE | REGISTER (default / reset values) |          |    |    |    |         |          |      |
|---------|------------|-----------------------------|-----------------|-----------------------------------|----------|----|----|----|---------|----------|------|
|         |            |                             |                 | MSB                               |          |    |    |    |         |          | LSB  |
|         |            |                             |                 | D7                                | D6       | D5 | D4 | D3 | D2      | D1       | D0   |
| 0x00h   | SET0       | 0010 1110                   | R/W             | MODE0                             | OV0[6:0] |    |    |    |         |          |      |
| 0x01h   | SET1       | 0101 1010                   | R/W             | MODE1                             | OV1[6:0] |    |    |    |         |          |      |
| 0x02h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x03h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x04h   | Ctrl       | 11xx xxxx                   | R/W             | PD_EN                             | PD_VSEL  |    |    |    |         |          |      |
| 0x05h   | Temp       | xxxx x000                   | R/W             |                                   |          |    |    |    | DIS_TS  | TJEW     | TJTS |
| 0x06h   | RmpCtrl    | 000x x00x                   | R/W             | RMP[2:0]                          |          |    |    |    | EN_DISC | RAMP_PFM |      |
| 0x07h   | (Reserved) | xxxx xxxx                   | -               |                                   |          |    |    |    |         |          |      |
| 0x08h   | Chip_ID    | 1001 01xx                   | R               |                                   |          |    |    |    |         |          |      |
| 0x09h   | Chip_ID    |                             |                 |                                   |          |    |    |    |         |          |      |

**Register 0x00h Description: SET0**

The register settings apply by choosing SET0 (VSEL = LOW).

**Table 11. TPS62366A Register 0x00h Description**

| REGISTER ADDRESS: 0x00h Read/Write |          |                                                                                            |                |                                                                                                   |          |                |          |        |
|------------------------------------|----------|--------------------------------------------------------------------------------------------|----------------|---------------------------------------------------------------------------------------------------|----------|----------------|----------|--------|
| BIT                                | NAME     | DEFAULT                                                                                    |                | DESCRIPTION                                                                                       |          |                |          |        |
| D7                                 | MODE0    | MSB                                                                                        | 0              | Operation mode for SET0<br>0 = PFM / PWM mode operation<br>1 = Forced PWM mode operation          |          |                |          |        |
| D6                                 | OV0[6:0] |                                                                                            | 1              | Output voltage for SET0                                                                           |          |                |          |        |
| D5                                 |          |                                                                                            | 0              | Default: $(100\ 0110)_2 = 1.2\text{V}$                                                            |          |                |          |        |
| D4                                 |          |                                                                                            | 0              | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table>                                     | D6-D0    | Output voltage |          |        |
| D6-D0                              |          |                                                                                            | Output voltage |                                                                                                   |          |                |          |        |
| D3                                 |          |                                                                                            | 0              | <table><tr><td>000 0000</td><td>500 mV</td></tr></table>                                          | 000 0000 | 500 mV         |          |        |
| 000 0000                           |          |                                                                                            | 500 mV         |                                                                                                   |          |                |          |        |
| D2                                 |          |                                                                                            | 1              | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV         | 000 0010 | 520 mV |
|                                    |          |                                                                                            |                | 000 0001                                                                                          | 510 mV   |                |          |        |
| 000 0010                           |          |                                                                                            | 520 mV         |                                                                                                   |          |                |          |        |
| D1                                 | 1        | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ...            | ...                                                                                               | 111 1111 | 1770 mV        |          |        |
|                                    |          | ...                                                                                        | ...            |                                                                                                   |          |                |          |        |
| 111 1111                           | 1770 mV  |                                                                                            |                |                                                                                                   |          |                |          |        |
| D0                                 |          | LSB                                                                                        | 0              | $V_{\text{OUT}} = (\text{xxx xxxx})_2 \times 10\text{mV} + 500\text{ mV}$                         |          |                |          |        |

**Table 12. TPS62366B Register 0x00h Description**

| REGISTER ADDRESS: 0x00h Read/Write |          |         |     |                                                                                          |
|------------------------------------|----------|---------|-----|------------------------------------------------------------------------------------------|
| BIT                                | NAME     | DEFAULT |     | DESCRIPTION                                                                              |
| D7                                 | MODE0    | MSB     | 0   | Operation mode for SET0<br>0 = PFM / PWM mode operation<br>1 = Forced PWM mode operation |
| D6                                 | OV0[6:0] |         | 0   | Output voltage for SET0<br>Default: (010 1110) <sub>2</sub> = 0.96V                      |
| D5                                 |          |         | 1   |                                                                                          |
| D4                                 |          |         | 0   |                                                                                          |
| D3                                 |          |         | 1   |                                                                                          |
| D2                                 |          |         | 1   |                                                                                          |
| D1                                 |          |         | 1   |                                                                                          |
| D0                                 |          |         | 0   |                                                                                          |
|                                    |          |         | LSB |                                                                                          |

## Register 0x01h Description: SET1

The register settings apply by choosing SET1 (VSEL = HIGH).

**Table 13. TPS62366A Register 0x01h Description**

| REGISTER ADDRESS: 0x01h Read/Write |          |                                                                                            |                |                                                                                                   |          |                |          |        |
|------------------------------------|----------|--------------------------------------------------------------------------------------------|----------------|---------------------------------------------------------------------------------------------------|----------|----------------|----------|--------|
| BIT                                | NAME     | DEFAULT                                                                                    |                | DESCRIPTION                                                                                       |          |                |          |        |
| D7                                 | MODE1    | MSB                                                                                        | 0              | Operation mode for SET1<br>0 = PFM / PWM mode operation<br>1 = Forced PWM mode operation          |          |                |          |        |
| D6                                 | OV1[6:0] |                                                                                            | 1              | Output voltage for SET1                                                                           |          |                |          |        |
| D5                                 |          |                                                                                            | 0              | Default: $(100\ 0010)_2 = 1.16\text{V}$                                                           |          |                |          |        |
| D4                                 |          |                                                                                            | 0              | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table>                                     | D6-D0    | Output voltage |          |        |
| D6-D0                              |          |                                                                                            | Output voltage |                                                                                                   |          |                |          |        |
| D3                                 |          |                                                                                            | 0              | <table><tr><td>000 0000</td><td>500 mV</td></tr></table>                                          | 000 0000 | 500 mV         |          |        |
| 000 0000                           |          |                                                                                            | 500 mV         |                                                                                                   |          |                |          |        |
| D2                                 |          |                                                                                            | 0              | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV         | 000 0010 | 520 mV |
|                                    |          |                                                                                            |                | 000 0001                                                                                          | 510 mV   |                |          |        |
| 000 0010                           |          |                                                                                            | 520 mV         |                                                                                                   |          |                |          |        |
| D1                                 | 1        | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ...            | ...                                                                                               | 111 1111 | 1770 mV        |          |        |
|                                    |          | ...                                                                                        | ...            |                                                                                                   |          |                |          |        |
| 111 1111                           | 1770 mV  |                                                                                            |                |                                                                                                   |          |                |          |        |
| D0                                 |          | LSB                                                                                        | 0              | $V_{\text{OUT}} = (\text{xxx xxxx})_2 \times 10\text{mV} + 500\text{ mV}$                         |          |                |          |        |

**Table 14. TPS62366B Register 0x01h Description**

| REGISTER ADDRESS: 0x01h Read/Write |          |                                                                                            |                |                                                                                                   |          |                |          |        |
|------------------------------------|----------|--------------------------------------------------------------------------------------------|----------------|---------------------------------------------------------------------------------------------------|----------|----------------|----------|--------|
| BIT                                | NAME     | DEFAULT                                                                                    |                | DESCRIPTION                                                                                       |          |                |          |        |
| D7                                 | MODE1    | MSB                                                                                        | 0              | Operation mode for SET1<br>0 = PFM / PWM mode operation<br>1 = Forced PWM mode operation          |          |                |          |        |
| D6                                 | OV1[6:0] |                                                                                            | 1              | Output voltage for SET1<br>Default: $(101\ 1010)_2 = 1.40\text{V}$                                |          |                |          |        |
| D5                                 |          |                                                                                            | 0              |                                                                                                   |          |                |          |        |
| D4                                 |          |                                                                                            | 1              | <table><tr><td>D6-D0</td><td>Output voltage</td></tr></table>                                     | D6-D0    | Output voltage |          |        |
| D6-D0                              |          |                                                                                            | Output voltage |                                                                                                   |          |                |          |        |
| D3                                 |          |                                                                                            | 1              | <table><tr><td>000 0000</td><td>500 mV</td></tr></table>                                          | 000 0000 | 500 mV         |          |        |
| 000 0000                           |          |                                                                                            | 500 mV         |                                                                                                   |          |                |          |        |
| D2                                 |          |                                                                                            | 0              | <table><tr><td>000 0001</td><td>510 mV</td></tr><tr><td>000 0010</td><td>520 mV</td></tr></table> | 000 0001 | 510 mV         | 000 0010 | 520 mV |
|                                    |          |                                                                                            |                | 000 0001                                                                                          | 510 mV   |                |          |        |
| 000 0010                           |          |                                                                                            | 520 mV         |                                                                                                   |          |                |          |        |
| D1                                 | 1        | <table><tr><td>...</td><td>...</td></tr><tr><td>111 1111</td><td>1770 mV</td></tr></table> | ...            | ...                                                                                               | 111 1111 | 1770 mV        |          |        |
|                                    |          | ...                                                                                        | ...            |                                                                                                   |          |                |          |        |
| 111 1111                           | 1770 mV  |                                                                                            |                |                                                                                                   |          |                |          |        |
| D0                                 |          | LSB                                                                                        | 0              | $V_{\text{OUT}} = (\text{xxx xxxx})_2 \times 10\text{mV} + 500\text{ mV}$                         |          |                |          |        |

**Register 0x04h Description: Ctrl****Table 15. TPS62366x Register 0x04h Description**

| REGISTER ADDRESS: 0x04h Read / Write |         |         |   |                                                                 |
|--------------------------------------|---------|---------|---|-----------------------------------------------------------------|
| BIT                                  | NAME    | DEFAULT |   | DESCRIPTION                                                     |
| D7                                   | PD_EN   | MSB     | 1 | EN internal pull down resistor<br>0 = disabled<br>1 = enabled   |
| D6                                   | PD_VSEL |         | 1 | VSEL internal pull down resistor<br>0 = disabled<br>1 = enabled |
| D5                                   |         |         | x | Reserved for future use                                         |
| D4                                   |         |         | x | Reserved for future use                                         |
| D3                                   |         |         | x | Reserved for future use                                         |
| D2                                   |         |         | x | Reserved for future use                                         |
| D1                                   |         |         | x | Reserved for future use                                         |
| D0                                   |         | LSB     | x | Reserved for future use                                         |

**Register 0x05h Description: Temp****Table 16. TPS62366x Register 0x05h Description**

| REGISTER ADDRESS: 0x05h Read/Write |        |         |   |                                                                                                                                                                                     |
|------------------------------------|--------|---------|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BIT                                | NAME   | DEFAULT |   | DESCRIPTION                                                                                                                                                                         |
| D7                                 |        | MSB     | x | Reserved for future use                                                                                                                                                             |
| D6                                 |        |         | x | Reserved for future use                                                                                                                                                             |
| D5                                 |        |         | x | Reserved for future use                                                                                                                                                             |
| D4                                 |        |         | x | Reserved for future use                                                                                                                                                             |
| D3                                 |        |         | x | Reserved for future use                                                                                                                                                             |
| D2                                 | DIS_TS |         | 0 | Disable temperature shutdown feature<br>0 = Temperature shutdown enabled<br>1 = Temperature shutdown disabled (not recommended)                                                     |
| D1                                 | TJEW   | LSB     | 0 | T <sub>J</sub> early warning bit<br>0 = T <sub>J</sub> < 120°C (typ)<br>1 = T <sub>J</sub> ≥ 120°C (typ)                                                                            |
| D0                                 | TJTS   |         | 0 | T <sub>J</sub> temperature shutdown bit<br>0 = die temperature within the valid range<br>1 = temperature shutdown was triggered<br>Bit needs to be reset after it has been latched. |

**Register 0x06h Description: RmpCtrl**
**Table 17. TPS62366x Register 0x06h Description**

| REGISTER ADDRESS: 0x06h Read/Write |          |         |   |                                                                                                                                                                                    |
|------------------------------------|----------|---------|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BIT                                | NAME     | DEFAULT |   | DESCRIPTION                                                                                                                                                                        |
| D7                                 | RMP[2:0] | MSB     | 0 | Output voltage ramp timing                                                                                                                                                         |
|                                    |          |         |   | D7-D5 Slope                                                                                                                                                                        |
|                                    |          |         |   | 000 32 mV / $\mu$ s                                                                                                                                                                |
|                                    |          |         |   | 001 16 mV / $\mu$ s                                                                                                                                                                |
|                                    |          |         |   | 010 8 mV / $\mu$ s                                                                                                                                                                 |
|                                    |          |         |   | ... ..                                                                                                                                                                             |
|                                    |          |         |   | 110 0.5 mV / $\mu$ s                                                                                                                                                               |
|                                    |          |         |   | 111 0.25 mV / $\mu$ s                                                                                                                                                              |
| D6                                 |          |         | 0 |                                                                                                                                                                                    |
| D5                                 |          |         | 0 | $\frac{\Delta V_{OUT}}{\Delta t} = 32 \frac{\text{mV}}{\mu\text{s}} \frac{1}{2^{(RMP[2-0])_2}}$                                                                                    |
| D4                                 |          |         | x | Reserved for future use                                                                                                                                                            |
| D3                                 |          |         | x | Reserved for future use                                                                                                                                                            |
| D2                                 | EN_DISC  |         | 0 | Active output capacitor discharge at shutdown<br>0 = disabled<br>1 = enabled                                                                                                       |
| D1                                 | RAMP_PFM |         | 0 | Defines the ramp behavior if the device is in Power Save (PFM) mode<br>0 = output cap is discharged by the load only<br>1 = output voltage is forced to follow the ramp down slope |
| D0                                 |          | LSB     | x | Reserved for future use                                                                                                                                                            |

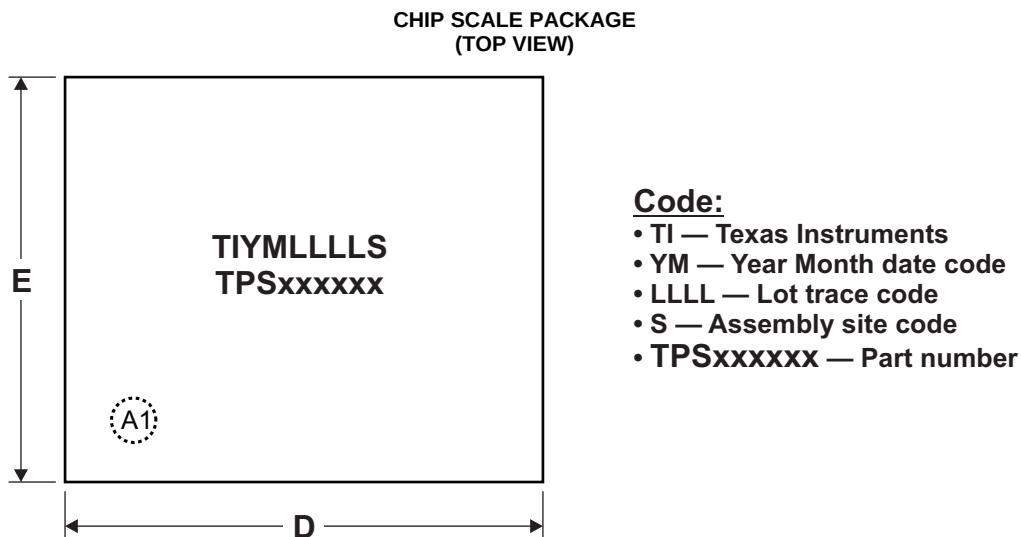
**Register 0x07h Description: (Reserved)**
**Table 18. TPS62366x Register 0x07h Description**

| REGISTER ADDRESS: 0x07h |      |         |   |                         |
|-------------------------|------|---------|---|-------------------------|
| BIT                     | NAME | DEFAULT |   | DESCRIPTION             |
| D7                      |      | MSB     | x | Reserved for future use |
| D6                      |      |         | x | Reserved for future use |
| D5                      |      |         | x | Reserved for future use |
| D4                      |      |         | x | Reserved for future use |
| D3                      |      |         | x | Reserved for future use |
| D2                      |      |         | x | Reserved for future use |
| D1                      |      |         | x | Reserved for future use |
| D0                      |      | LSB     | x | Reserved for future use |

**Register 0x08h, 0x09h Description Chip\_ID:****Table 19. TPS62366x Register 0x08h and 0x09h Description**

| REGISTER ADDRESS: 0x08h, 0x09 Read |        |         |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |
|------------------------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--|------------------|------------------|----|-----------|----|-----------|----|--------|----|--------|
| BIT                                | NAME   | DEFAULT |                                                                                                                                                                                                             | DESCRIPTION |  |                  |                  |    |           |    |           |    |        |    |        |
| D7                                 |        | MSB     | 1                                                                                                                                                                                                           | Vendor ID   |  |                  |                  |    |           |    |           |    |        |    |        |
| D6                                 |        |         | 0                                                                                                                                                                                                           |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D5                                 |        |         | 0                                                                                                                                                                                                           |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D4                                 |        |         | 1                                                                                                                                                                                                           |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D3                                 |        | x       | <table><tr><td>D3-D2</td><td>Part number ID</td></tr><tr><td>00</td><td>TPS62366A</td></tr><tr><td>01</td><td>TPS62366B</td></tr><tr><td>10</td><td>-</td></tr><tr><td>11</td><td>-</td></tr></table>       |             |  | D3-D2            | Part number ID   | 00 | TPS62366A | 01 | TPS62366B | 10 | -      | 11 | -      |
| D3-D2                              |        |         |                                                                                                                                                                                                             |             |  | Part number ID   |                  |    |           |    |           |    |        |    |        |
| 00                                 |        |         |                                                                                                                                                                                                             |             |  | TPS62366A        |                  |    |           |    |           |    |        |    |        |
| 01                                 |        |         |                                                                                                                                                                                                             |             |  | TPS62366B        |                  |    |           |    |           |    |        |    |        |
| 10                                 | -      |         |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |
| 11                                 | -      |         |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D2                                 | x      | 10      | -                                                                                                                                                                                                           |             |  |                  |                  |    |           |    |           |    |        |    |        |
|                                    |        | 11      | -                                                                                                                                                                                                           |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D1                                 |        | x       | <table><tr><td>D1-D0</td><td>Chip revision ID</td></tr><tr><td>00</td><td>Rev. 1</td></tr><tr><td>01</td><td>Rev. 2</td></tr><tr><td>10</td><td>Rev. 3</td></tr><tr><td>11</td><td>Rev. 4</td></tr></table> |             |  | D1-D0            | Chip revision ID | 00 | Rev. 1    | 01 | Rev. 2    | 10 | Rev. 3 | 11 | Rev. 4 |
| D1-D0                              |        |         |                                                                                                                                                                                                             |             |  | Chip revision ID |                  |    |           |    |           |    |        |    |        |
| 00                                 |        |         |                                                                                                                                                                                                             |             |  | Rev. 1           |                  |    |           |    |           |    |        |    |        |
| 01                                 |        |         |                                                                                                                                                                                                             |             |  | Rev. 2           |                  |    |           |    |           |    |        |    |        |
| 10                                 | Rev. 3 |         |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |
| 11                                 | Rev. 4 |         |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |
| D0                                 | x      | 00      | Rev. 1                                                                                                                                                                                                      |             |  |                  |                  |    |           |    |           |    |        |    |        |
|                                    |        | 01      | Rev. 2                                                                                                                                                                                                      |             |  |                  |                  |    |           |    |           |    |        |    |        |
|                                    |        | 10      | Rev. 3                                                                                                                                                                                                      |             |  |                  |                  |    |           |    |           |    |        |    |        |
|                                    |        | 11      | Rev. 4                                                                                                                                                                                                      |             |  |                  |                  |    |           |    |           |    |        |    |        |
|                                    |        | LSB     |                                                                                                                                                                                                             |             |  |                  |                  |    |           |    |           |    |        |    |        |

## PACKAGE SUMMARY



**Figure 54. Package Marking and Dimensions**

## CHIP SCALE PACKAGE DIMENSIONS

The TPS62366x device is available in a 16-bump chip scale package (YZH, NanoFree™). The package dimensions are given as:

- **D** = 2.076mm (+/- 0.03mm)
- **E** = 2.076mm (+/- 0.03mm)

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS62366AYZHR</a> | Active        | Production           | DSBGA (YZH)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS62366A           |
| TPS62366AYZHR.A               | Active        | Production           | DSBGA (YZH)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 150   | TPS62366A           |
| <a href="#">TPS62366AYZHT</a> | Active        | Production           | DSBGA (YZH)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS62366A           |
| TPS62366AYZHT.A               | Active        | Production           | DSBGA (YZH)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 150   | TPS62366A           |
| <a href="#">TPS62366BYZHR</a> | Active        | Production           | DSBGA (YZH)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS62366B           |
| TPS62366BYZHR.A               | Active        | Production           | DSBGA (YZH)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 150   | TPS62366B           |
| <a href="#">TPS62366BYZHT</a> | Active        | Production           | DSBGA (YZH)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS62366B           |
| TPS62366BYZHT.A               | Active        | Production           | DSBGA (YZH)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 150   | TPS62366B           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

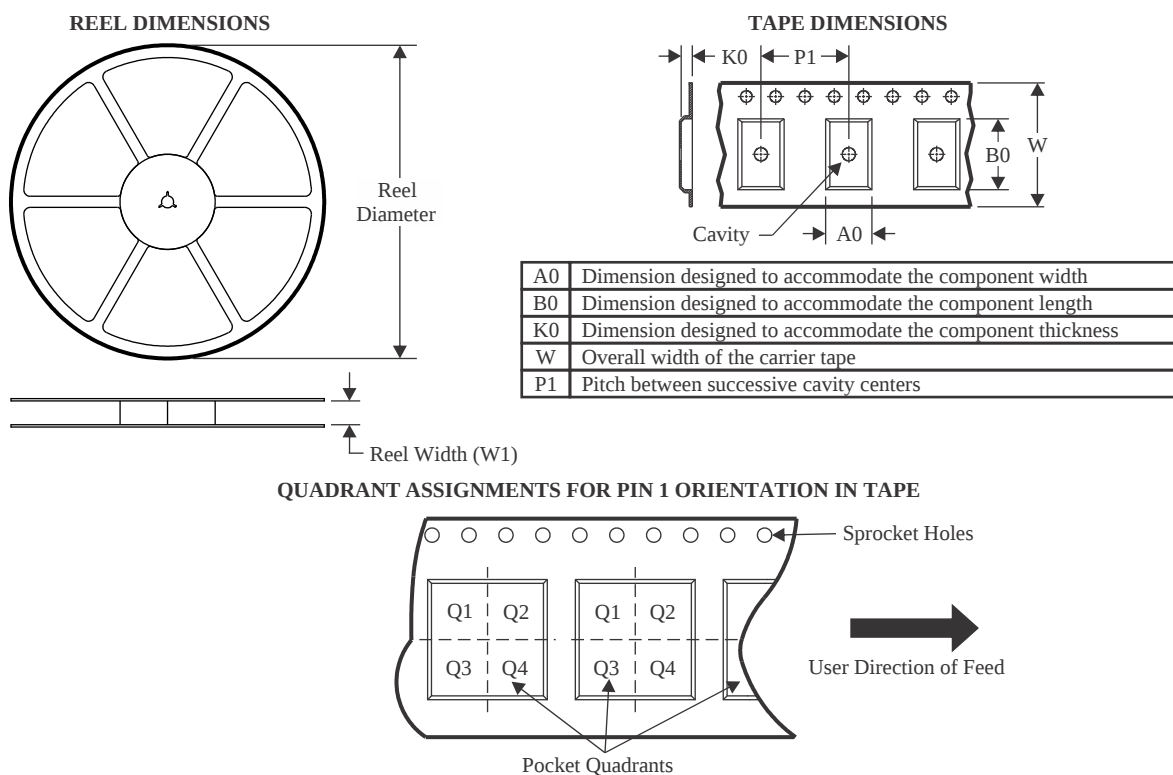
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

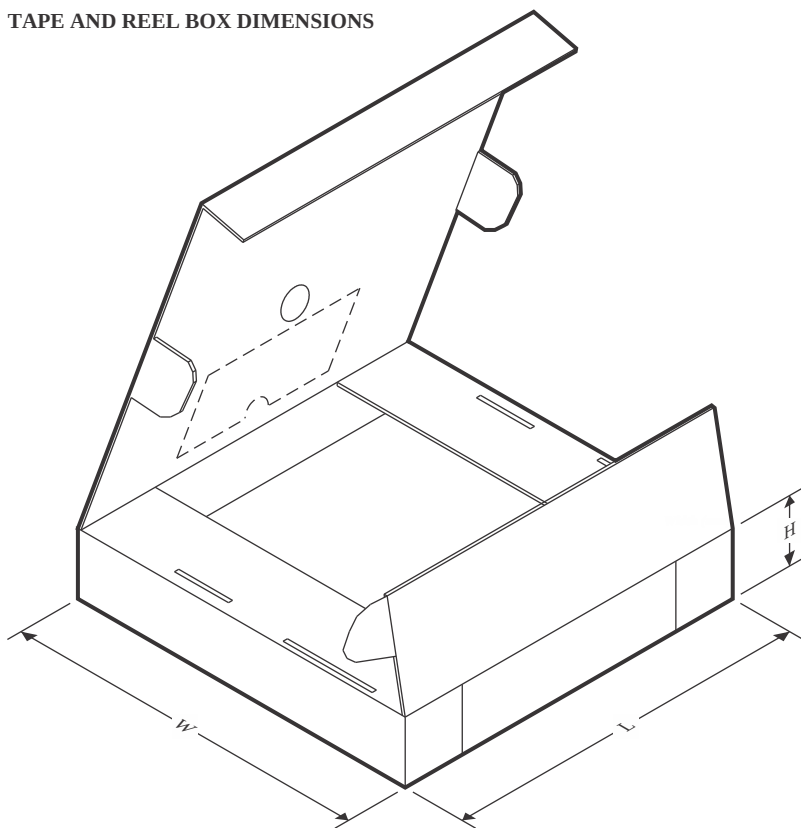
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62366AYZHR | DSBGA        | YZH             | 16   | 3000 | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |
| TPS62366AYZHT | DSBGA        | YZH             | 16   | 250  | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |
| TPS62366BYZHR | DSBGA        | YZH             | 16   | 3000 | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |
| TPS62366BYZHT | DSBGA        | YZH             | 16   | 250  | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |

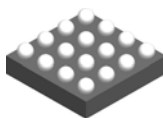
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62366AYZHR | DSBGA        | YZH             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| TPS62366AYZHT | DSBGA        | YZH             | 16   | 250  | 182.0       | 182.0      | 20.0        |
| TPS62366BYZHR | DSBGA        | YZH             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| TPS62366BYZHT | DSBGA        | YZH             | 16   | 250  | 182.0       | 182.0      | 20.0        |

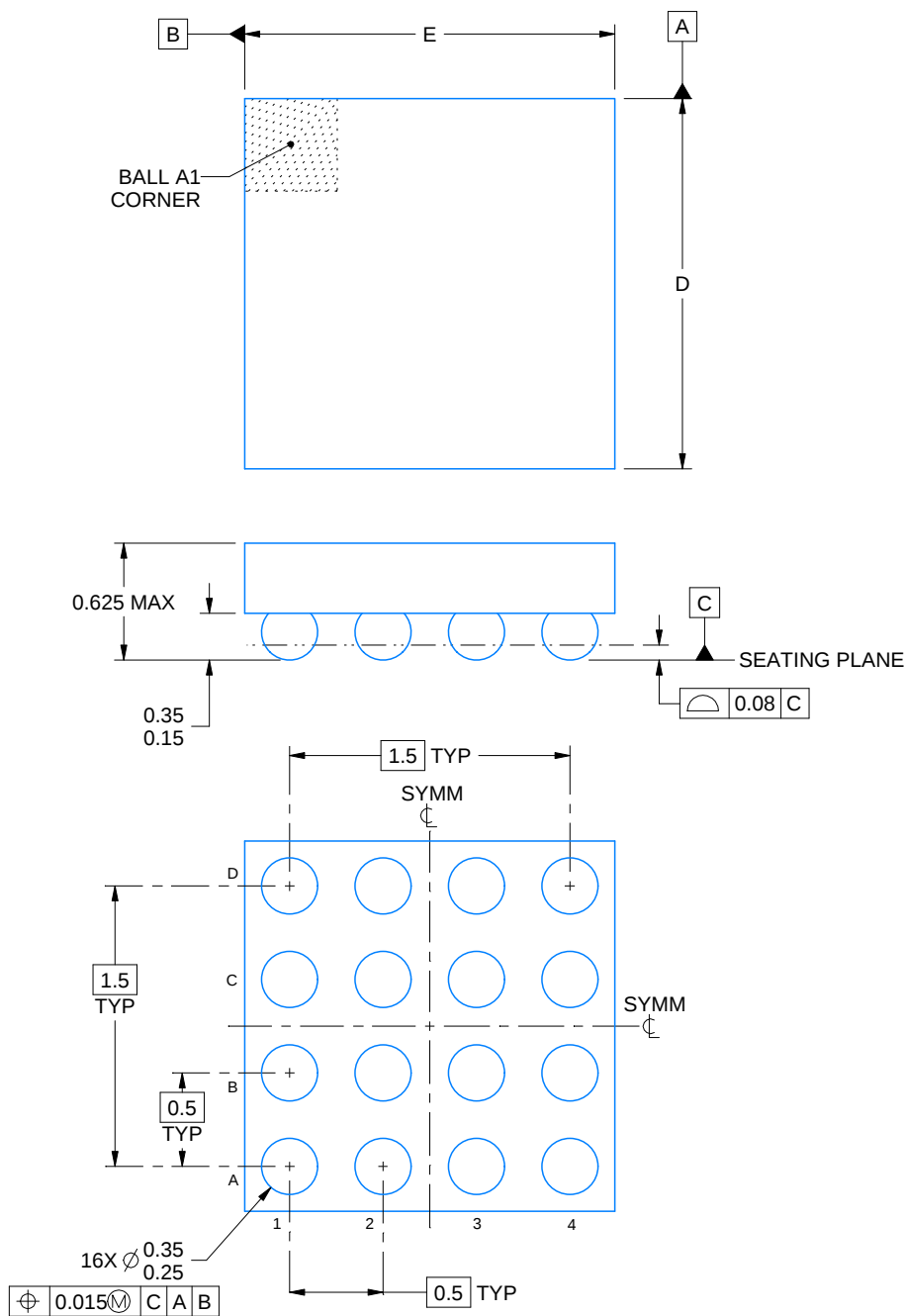
YZH0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4226617/A 03/2021

## NOTES:

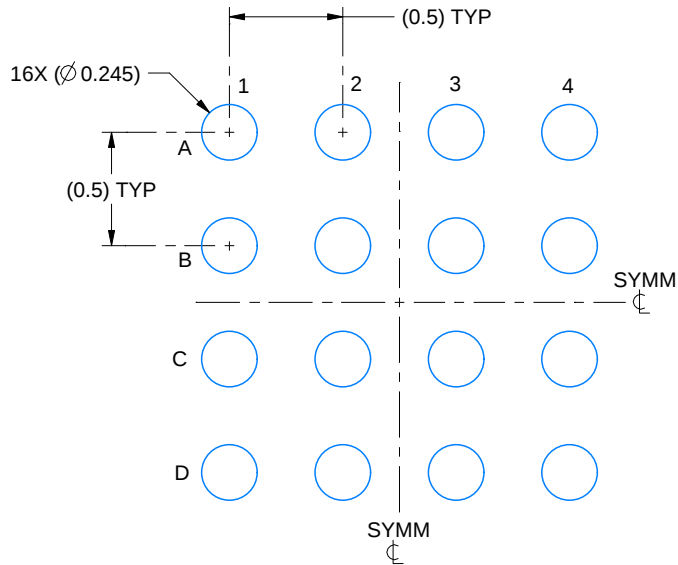
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

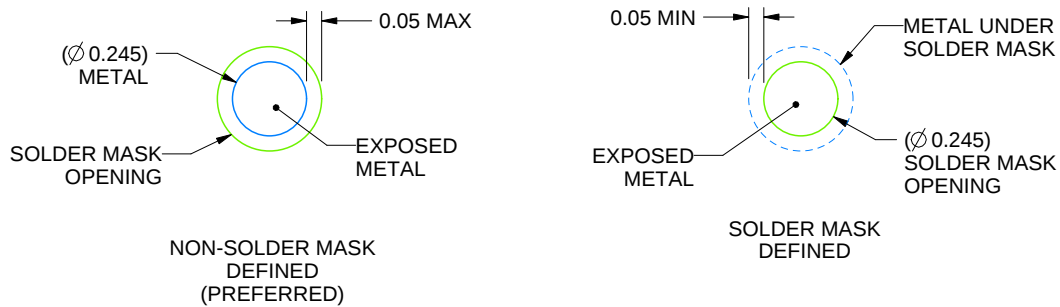
YZH0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



SOLDER MASK DETAILS  
NOT TO SCALE

4226617/A 03/2021

NOTES: (continued)

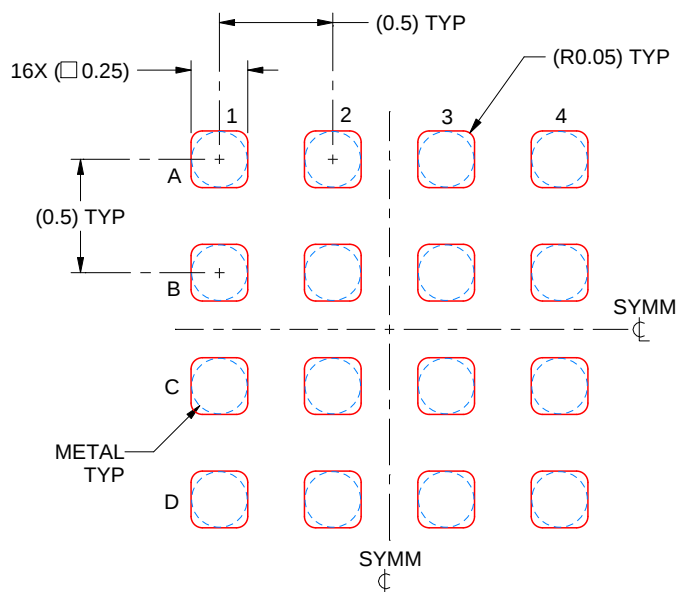
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZH0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
 BASED ON 0.075 mm THICK STENCIL  
 SCALE: 30X

4226617/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025