

FDZ493P

P-Channel 2.5V Specified PowerTrench® BGA MOSFET –20V, –4.6A, 46mΩ

Features

- Max $r_{DS(on)}$ = 46mΩ at $V_{GS} = -4.5V$, $I_D = -4.6A$
- Max $r_{DS(on)}$ = 72mΩ at $V_{GS} = -2.5V$, $I_D = -3.6A$
- Occupies only 2.25 mm² of PCB area. Less than 50% of the area of SSOT-6.
- Ultra-thin package: less than 0.80 mm height when mounted to PCB.
- Outstanding thermal transfer characteristics: 4 times better than SSOT-6.
- Ultra-low $Q_g \times r_{DS(on)}$ figure-of-merit.
- RoHS Compliant.

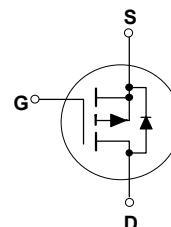
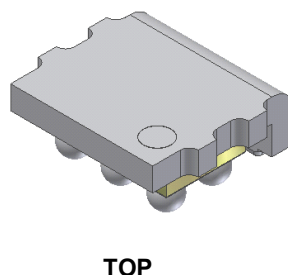
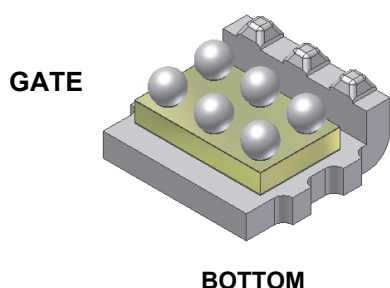


General Description

Combining Fairchild's advanced 2.5V specified PowerTrench® process with state of the art BGA packaging process, the FDZ493P minimizes both PCB space and $r_{DS(on)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

Application

- Battery management
- Load switch
- Battery protection



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current –Continuous $T_A = 25^\circ C$ (Note 1a)	–4.6	A
	–Pulsed	–10	
P_D	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	1.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	72	$^\circ C/W$
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
E	FDZ493P	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V}$, $V_{GS} = 0\text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-0.6	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -4.5\text{V}$, $I_D = -4.6\text{A}$		36	46	m Ω
		$V_{GS} = -2.5\text{V}$, $I_D = -3.6\text{A}$		58	72	
		$V_{GS} = -4.5\text{V}$, $I_D = -4.6\text{A}$, $T_J = 125^\circ\text{C}$		47	65	
$I_{D(on)}$	On to State Drain Current	$V_{GS} = -4.5\text{V}$, $V_{DS} = -5\text{V}$	-10			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{V}$, $I_D = -4.6\text{A}$		13		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		754		pF
C_{oss}	Output Capacitance			167		pF
C_{rss}	Reverse Transfer Capacitance			92		pF
R_g	Gate Resistance	$f = 1\text{MHz}$		6		Ω

Switching Characteristics (note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{V}$, $I_D = -1\text{A}$ $V_{GS} = -4.5\text{V}$, $R_{GEN} = 6\Omega$		11	20	ns
t_r	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
t_f	Fall Time			17	31	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{DS} = -10\text{V}$, $I_D = -4.6\text{A}$		7.5	11	nC
Q_{gs}	Gate to Source Gate Charge	$V_{GS} = -4.5\text{V}$		1.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.0		nC

Drain-Source Diode Characteristics

I_S	Maximum continuous Drain-Source Diode Forward Current				-1.4	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = -1.4\text{A}$ (Note 2)		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -4.6\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		17		ns
Q_{rr}	Reverse Recovery Charge			5		nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$ is defined for reference. For $R_{\theta JC}$ the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 72°C/W when mounted on a 1 in² pad of 2 oz copper, 1.5" X 1.5" X 0.062" thick PCB



b. 157°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

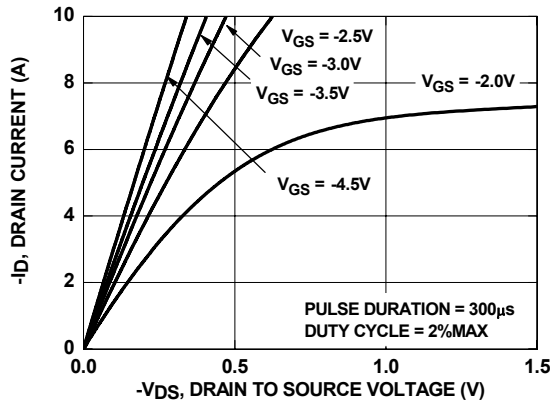


Figure 1. On Region Characteristics

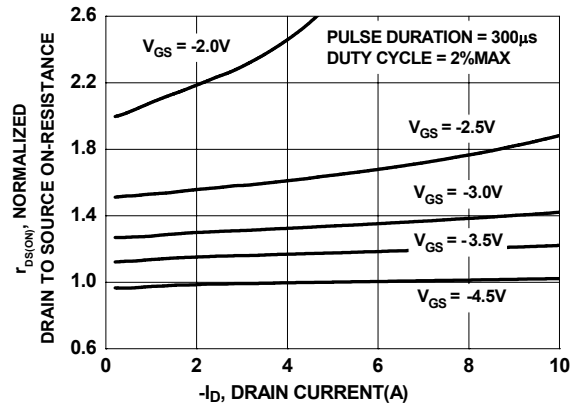


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

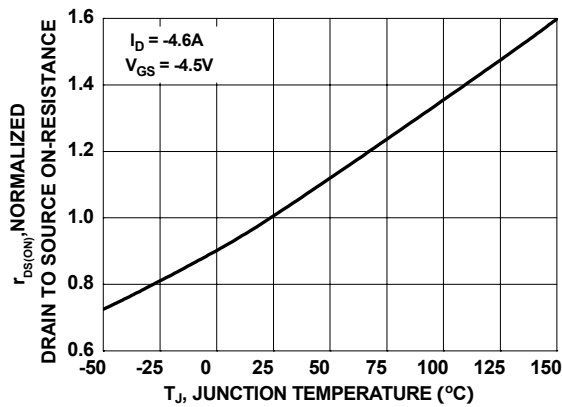


Figure 3. Normalized On Resistance vs Junction Temperature

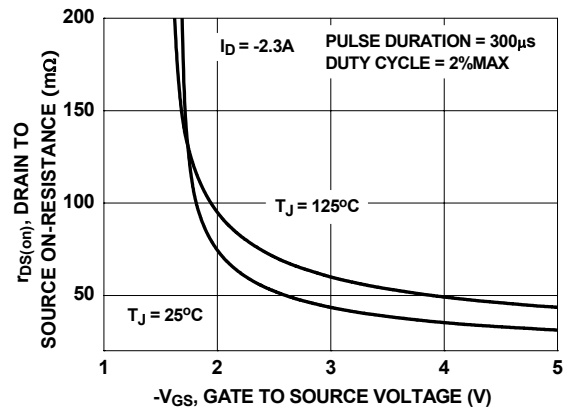


Figure 4. On-Resistance vs Gate to Source Voltage

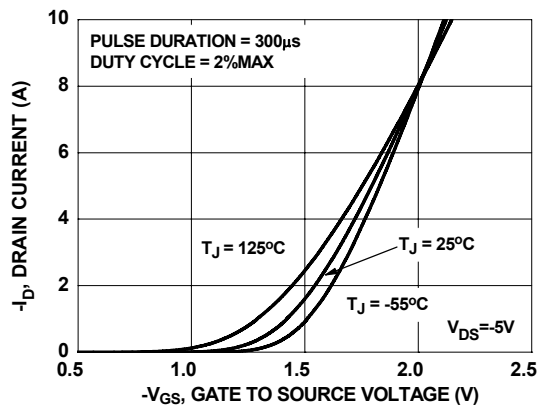


Figure 5. Transfer Characteristics

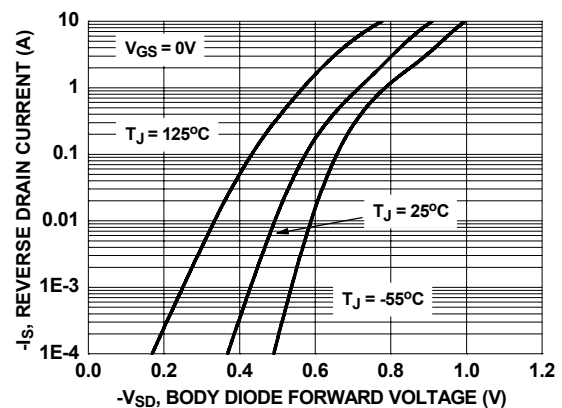


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

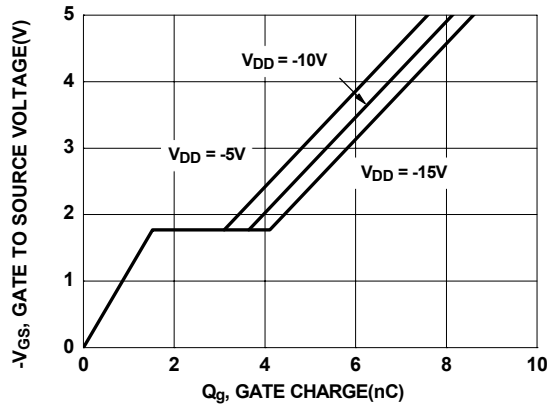


Figure 7. Gate Charge Characteristics

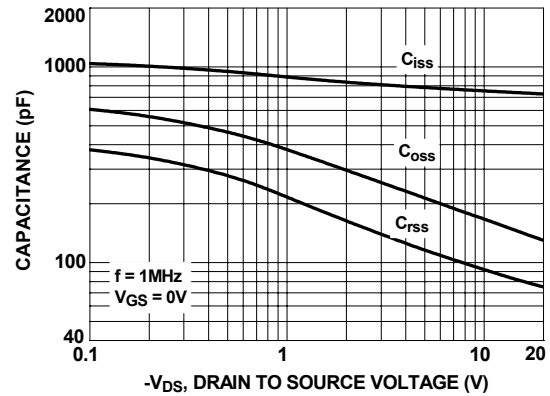


Figure 8. Capacitance vs Drain to Source Voltage

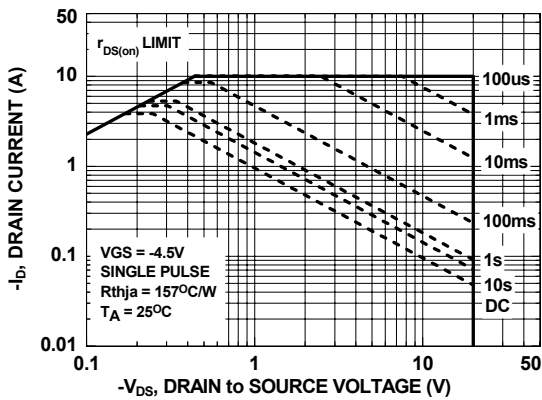


Figure 9. Forward Bias Safe Operating Area

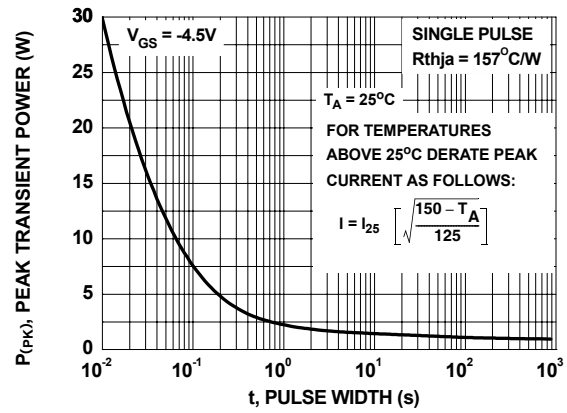


Figure 10. Single Pulse Maximum Power Dissipation

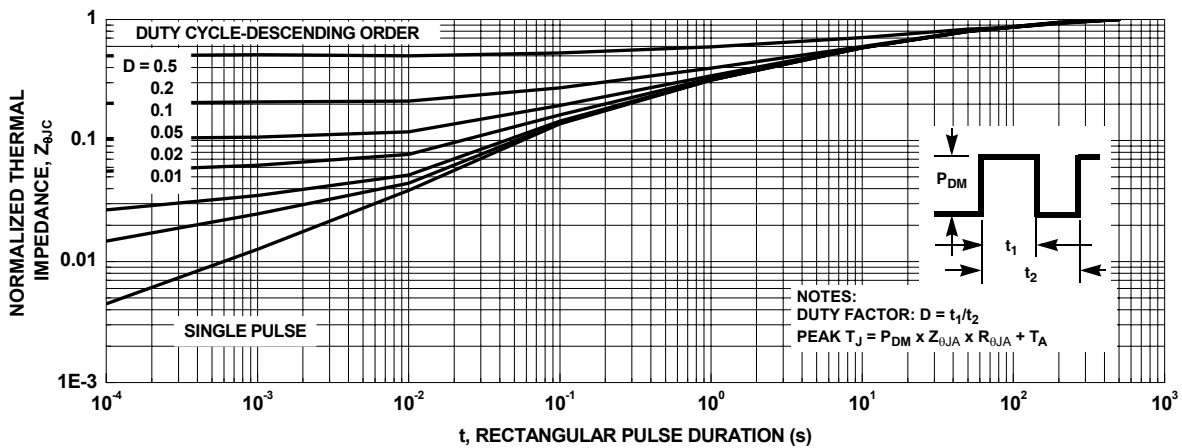
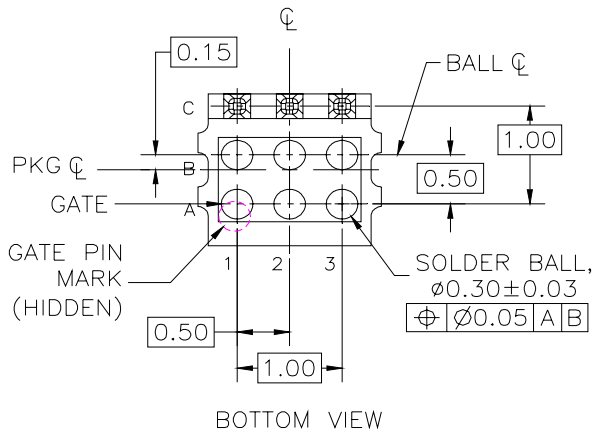
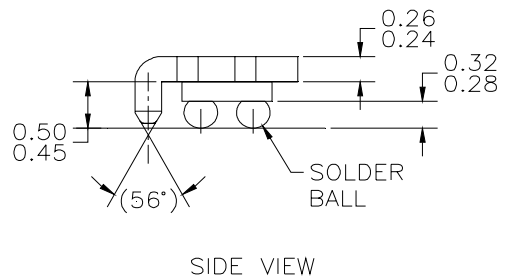
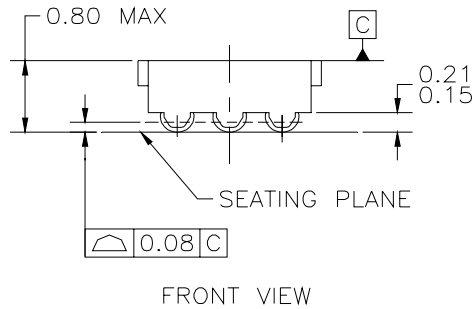
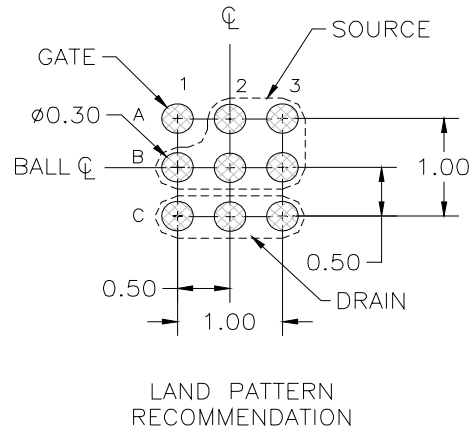
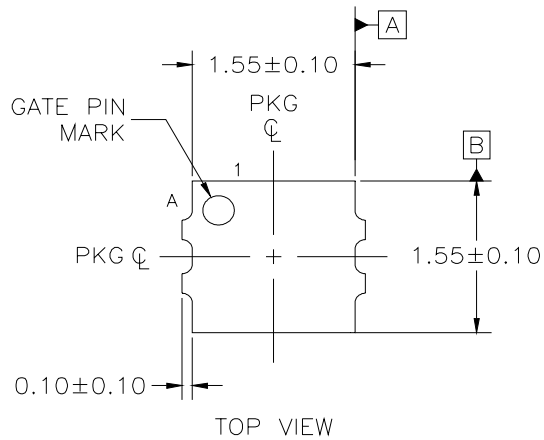


Figure 11. Transient Thermal Response Curve

Dimensional Pad and Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
- C) BALL/STUD CONFIGURATION TABLE

TERMINAL ID	DESIGNATION	TERMINAL TYPE
C1,C2,C3	DRAIN	COPPER STUD
A1	GATE	BALL
A2,A3,B1,B2,B3	SOURCE	BALL

BGA09CREVC

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FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
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