Integrated Low Profile Transceiver Module for Telecom Applications 9.6 kbit/s to 1.152 Mbit/s Data Transmission Rate

Description

The miniaturized TFDU5107 in the well-known Baby Face package is an ideal transceiver for applications in telecommunications like mobile phones, pagers, and PDAs of all kinds. The devices are designed for optimum performance and minimum package size.

The device covers the IrDA® physical layer specification with SIR specification and 1.152 Mbit/s IrDA® mode.

The new features

A current limiter is implemented to operate the device whitout external resistor in an IrDA compliant mode (> 1 m). For reduced current as for the “Low Power” mode a current limiting resistor might be added.

The device covers the supply voltage **from 3.6 V down to 2.4 V** and with its **low power consumption** it is optimum suited for battery powered applications. Double eye safety protection by pulse duration and current limitation is integrated.
As additional feature the logic voltage swing V_{logic} can be set externally.

Features

- Package:
  - **TFDU5107 Universal (Baby Face)**
  - SMD Side and Top View Solderability
- Internal IRED current limition to operate without external resistor. With external resistor adaptable to power reduced operation as IrDA “Low Power” Standard
- Wide Supply Voltage Range (2.4 V to 3.6 V)
- Operational down to 2.0 V
- **Logic Input and Output Voltage 1.5 V to 5.5 V set by external control pin**
- Tri – State – Receiver Output
- Lowest Power Consumption, typically 500 µA in Receive Mode, <1 µA Shutdown,
  only typical 5 mA Average Current Consumption in SIR and 1.152 Mbit/s Transmit Mode in Low Power IrDA mode
- Fewest External Components
- High EMI Immunity
- Eye Safety Protection Integrated
- Pin Assignment Backward Compatible to Legacy Baby Face Package

Applications

- Mobile Phones, Pagers, Hand–held Battery Operated Equipment
- Computers (WinCE, PalmPC, PDAs)
- Digital Still and Video Cameras
- Extended IR Adapters
- Medical and Industrial Data Collection

Package

TFDU5107
Baby Face (Universal)

Ordering Information

Part Number	Qty / Reel	Description
TFDU5107–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU5107–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting

Functional Block Diagram

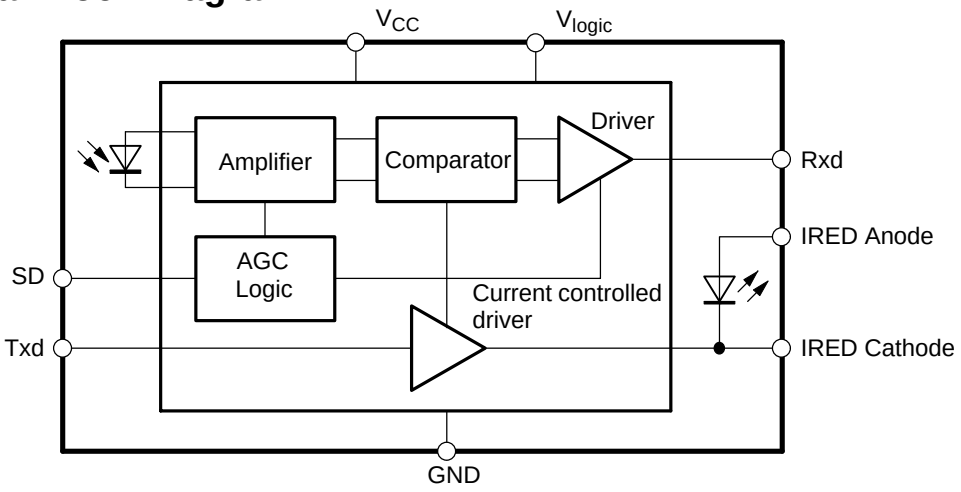

Figure 1. Functional Block Diagram

Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	IRED Anode to be externally connected to directly to V_{CC}. Alternatively the current can be decreased by an external resistor.This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled V_{CC} supply		
2	IRED Cathode	IRED Cathode, internally connected to driver transistor		
3	Txd	Transmit Data Input	I	HIGH
4	Rxd	Received Data Output, push–pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull–up or pull–down resistor is required. Pin is floating with a weak pull up to V_{CC}, when device is in shutdown mode. Rxd output is quiet during transmission.	O	LOW
5	SD	Shutdown, will switch the device into shutdown after a delay of 1 ms	I	HIGH
6	V_{CC}	Supply Voltage		
7	V_{logic}	Defines the input and output logic swing voltage	I	
8	GND	Ground		

Baby Face (Universal)

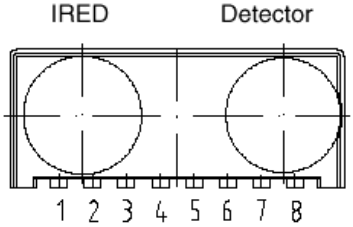

Figure 2. Pinning

Absolute Maximum Ratings

Reference Point Ground, Pin 8, unless otherwise noted

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range	0 V < V_{dd2} < 6 V	V_{dd1}	–0.5		6	V
	0 V < V_{dd1} < 6 V	V_{dd2}	–0.5		6	V
	0 V < V_{dd2} < 6 V 0 V < V_{dd1} < 6 V	V_{logic}	–0.5		6	V
Input Current	All Pins (Pin 1 excluded)				10	mA
Output Sink Current, Rxd	Pin 4				25	mA
Rep. Pulsed IRED Current	Pin 1, t_{on}< 20%, < 20 µs	I_{IRED}(RP)			500	mA
Average IRED Current		I_{IRED}(DC)			125	mA
Power Dissipation		P_{tot}			450	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		85	°C
Storage Temperature Range		T_{stg}	–25		85	°C
Soldering Temperature	t = 20 s @215°C			215	240	°C
Transmitter Data and Shutdown Input Voltage	2.4 V < V_{dd1} < 5.5 V	V_{Txd}, V_{SD}	–0.5		6	V
Receiver Data Output Voltage		V_{Rxd}	–0.5		V_{logic}+0.5	V
Virtual Source Size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1	IEC60825–1 or EN60825–1, edition Jan.2001	I_e			*) (500) **)	mW/sr

*) Due to the internal limitation measures the device is a “class 1” device
**) IrDA specifies the max. intensity with 500 mW/sr

Optoelectronic Characteristics

T_{amb} = 25°C, V_{dd1} = 2.4 V to 3.6 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supported Data Rates Rxd pulse duration 400 ns	Base band SIR mode		9.6		115.2	kbit/s
	Base band 1.152 Mbit/s		9.6		1152	kbit/s
Supply Voltage Range	specified operation	V_{dd1}	2.4		3.6	V
Supply Voltage	V_{dd2} = 2.4 V to 3.6 V	V_{dd2}	2.4		3.6	V
Supply Current receive mode	V_{dd1} = 2.4 V to 3.6 V	I_S		500	900	µA
Supply Current shutdown mode	V_{dd1} = 2.4 V to 3.6 V	I_{SSD}		0.1	1	µA
Average Supply Current *) Standart MIR transmit mode I_e > 100 mW/ sr	V_{dd1} = 2.4 V to 3.6 V, above V_{dd1} =3.3 V a serial resistor for reducing the internal power dissipation should be implemented, e.g. R_L = 2.7 Ω	I_S		60	110	mA
Logic Voltage Range	V_{dd2} = 2.4 V to 3.6 V	V_{logic}	1.5		3.6	V
Shutdown / Mode clock pulse duration		t_{prog}	0.2		20	µs
Shutdown delay ”Receive off”		t_{prog}	1		1.5	ms
Shutdown Delay ”Receive on”		t_{prog}	40		100	µs
Transceiver “Power On“ Settling Time	Time from switching on V_{dd1} to established specified operation				50	µs

*) Maximum data is for 20% (25%) duty cycle for SIR (MIR 1.152 Mbit/s) Low power mode. The typical value is given for the case of normal operation with statistical and equal ”0” and ”1” – distribution.

Optoelectronic Characteristics

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Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Minimum Detection Threshold Irradiance SIR 9.6 kbit/s to 115.2 kbit/s *)	$\|\alpha\| \le \pm 15°$ V_{dd1} = 2.4 V to 3.6 V	$E_{e,\,min}$		20	35	mW/m^2
Minimum Detection Threshold Irradiance 9.6 kbit/s to 1.152 Mbit/s *)	$\|\alpha\| \le \pm 15°$ V_{dd1} = 2.4 V to 3.6 V	$E_{e,\,min}$		50	80	mW/m^2
Maximum Detection Threshold Irradiance	$\|\alpha\| \le \pm 90°$ V_{dd1} = 5 V	$E_{e,\,max}$	3300	5000		W/m^2
	$\|\alpha\| \le \pm 90°$ V_{dd1} = 3 V	$E_{e,\,max}$	8000	15000		W/m^2
Logic Low Receiver Input Irradiance		$E_{e,max,low}$	4			mW/m^2
Output Voltage Rxd	Active C = 15 pF, R = 2.2 kΩ	V_{OL}		0.5	0.8	V
	Non active C = 15 pF, R = 2.2 kΩ	V_{OH}	V_{logic}–0.5			V
Output Current Rxd V_{OL} < 0.8 V					4	mA
Rise Time @Load: C = 15 pF, R = 2.2 kΩ	1.5 V ≤ V_{logic} ≤ 5.5 V	t_r	20		70	ns
Fall Time @Load: C = 15 pF, R = 2.2 kΩ	1.5 V ≤ V_{logic} ≤ 5.5 V	t_f	20		70	ns
Rxd Signal Electrical Output Pulse Width	1.5 V ≤ V_{logic} ≤ 5.5 V	t_p	300	400	500	ns
Latency		t_L		100	200	µs

*) Rxd output pulse duration 400 ns

Optoelectronic Characteristics

T_{amb} = 25°C, V_{dd1} = 2.4 V to 3.6 V unless otherwise noted.
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Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transmitter						
Logic CMOS High/Low Decision Threshold		V_{IL}(Txd)		1/2xV_{logic}		V
Logic Low Transmitter Input Voltage		V_{IL}(Txd)	0		0.2*) V_{logic}	V
Logic High Transmitter Input Voltage	1.5 V < V_{logic} < 3.6 V	V_{IH}(Txd)	0.8*) V_{logic}		V_{logic} +0.5	V
Current Limitation	V_{dd1} = 3.3 V	I_F		400		mA
Output Radiant Intensity, $\|\alpha\| \leq \pm 15°$ Standard MIR level	I_{F6} = 400 mA resistor limited	I_e	110	250	320	mW/sr
Maximum Output Pulse width (eye safety protection)	P_{WI} > 23 µs	P_{WOmin}	23		80	µs
Optical Pulse width	P_{WI} = 1.6 µs	P_{WO}	1.45		1.75	µs
	P_{WI} = 217 ns	P_{WO}	210		226	ns
Optical Rise/Falltime		t_r, t_f			40	ns
Peak Wavelength of Emission		λ_p	880		900	nm
Spectral Optical Radiation Bandwidth		$\Delta\lambda$		45		nm
Output Radiant Intensity	Txd logic low level				0.04	µW/sr
Overshoot, Optical					25	%
Rising Edge Peak to Peak Jitter		t_j			0.2	µs

*) Switch, current can be defined by external resistor, internal current limitation to 500 mA peak

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads.

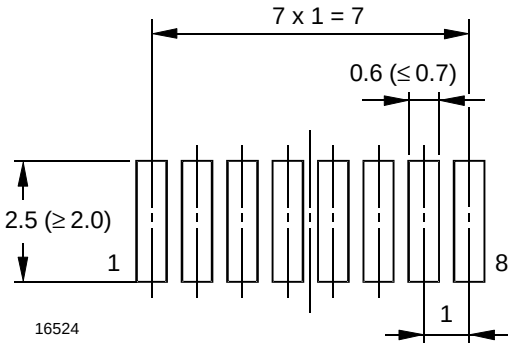


Figure 3. TFDU5107 Baby Face (Universal)

Recommended Solder Profile

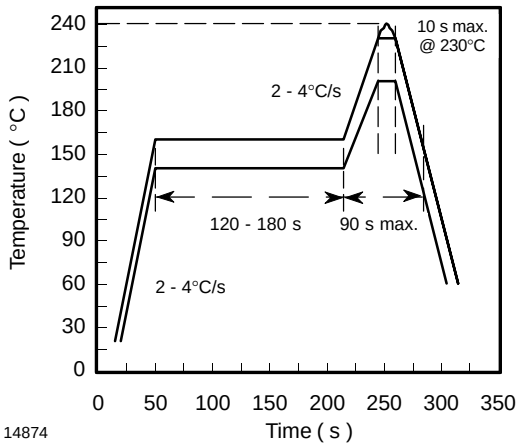


Figure 4. Recommended Solder Profile

Current Derating Diagram

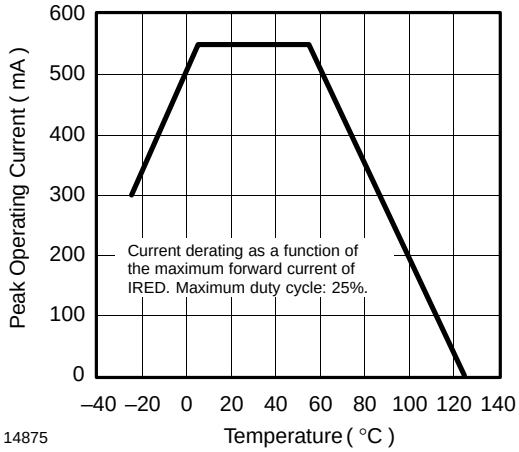


Figure 5. Current Derating Diagram

Identification

The identification of the device can be recalled by setting the SD active followed by activating Txd for a short period. With the low going edge of Txd a single pulse is generated at Rxd.
The SD is intendet to activate the shutdown function after a delay of 1 ms. Therefore the full sequence should be run with that 1 ms time limitation, see drawing.

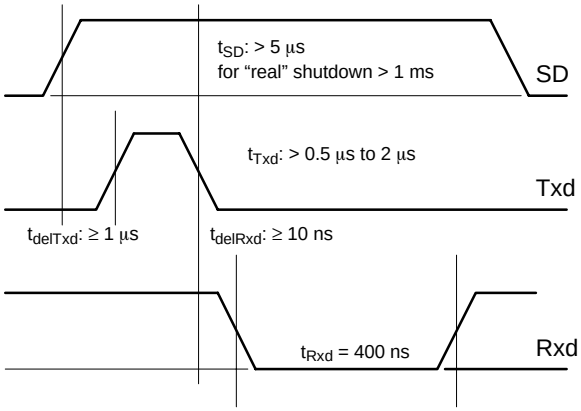


Figure 6.

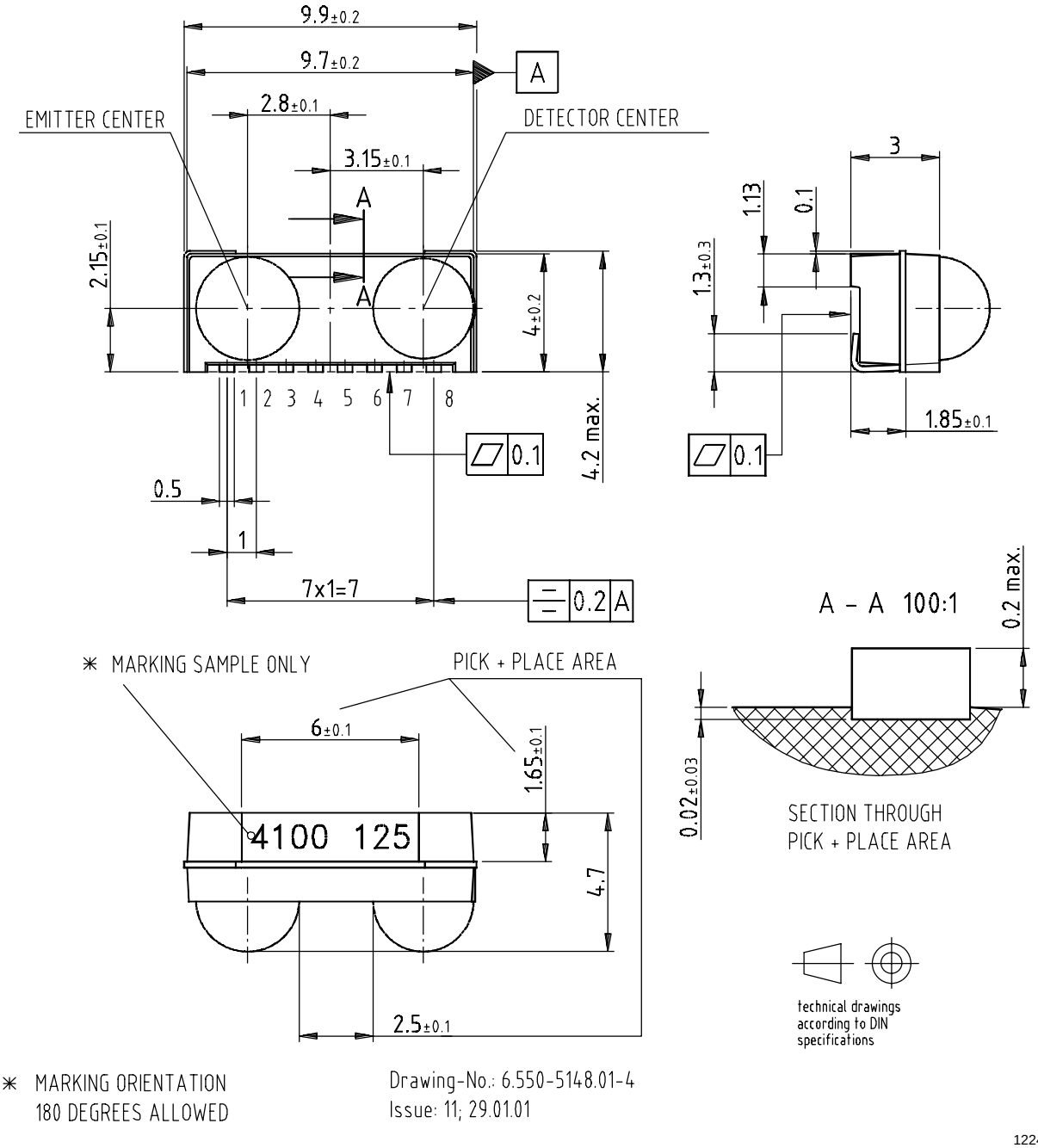
V_{logic} Setting

The logic voltage swing is set by applying an external voltage to the V_{logic} pin.

Table 1. Truth table

Inputs			Outputs	
SD	Txd	Optical input Irradiance mW/ m^2	Rxd	LED drive current resulting intensity I_e in mW/ sr
high < 1 ms	pulse	x	low going Txd triggers monostable to edit a 400 ns low pulse	0
high > 1 ms	x	x	floating (500 kΩ to V_{dd})	0
low	high	x	high	10 < I_e < 300 defined by an external resistor
low	high > 80 µs	x	high	0
low	low	< 4	high	0
low	low	> 40	low, pulse of 400 ns edge triggered	0

TFDU5107 – Baby Face (Universal) Package (Mechanical Dimensions)



✳ MARKING ORIENTATION
180 DEGREES ALLOWED

Drawing-No.: 6.550-5148.01-4
Issue: 11; 29.01.01

12249

Appendix

Application Hints

The TFDU5107 do not need any external components when operated at a ”clean” power supply. In a more power supply noisy ambient it is recommended to add a combination of a resistor and capacitor (R1, C1, C2) for noise suppression as shown in the figure below. A combination of a electrolytic for the low frequency range and a ceramic capacitor for suppressing the high frequency disturbance will be most effective. The capacitor C3 is only necessary when inductive wiring is used or the power supply cannot deliver the operating peak pulse current.

The inputs TXD and SD are high impedance CMOS inputs. Therefore, the lines from the I/O to those inputs should be carefully designed not to pick up ambient noise. If long lines are used, loads at the Txd input of the TFDx5x07 and at the Rxd input of the controller (!) are recommended. At the IRED Anode voltage supply line an additional capacitor might be necessary when inductive wiring is used. However, a low impedance layout is the better and more cost efficient solution. For adjusting the intensity depending on the application, see the diagrams.

Recommended Circuit Diagram

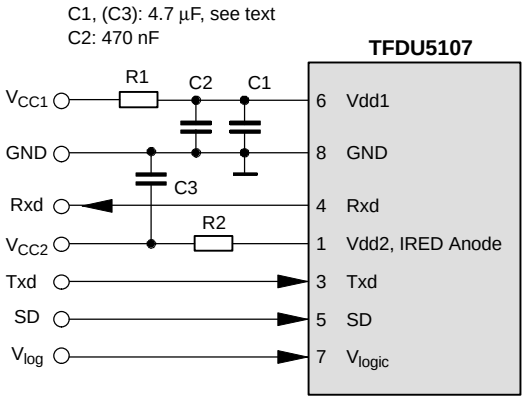


Figure 7. Recommended Application Circuit

Shut Down

To shut down the TFDx5x07 into a standby mode the SD pin has to be set active. After a delay of < 1 ms it will switch to the standby mode.

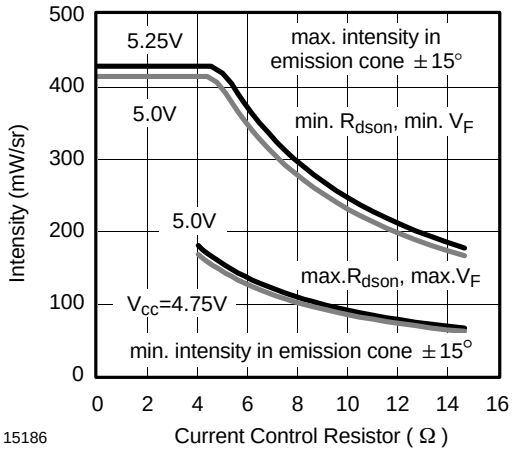


Figure 8. Intensity I_e vs. Current Control Resistor R2
5 V Applications

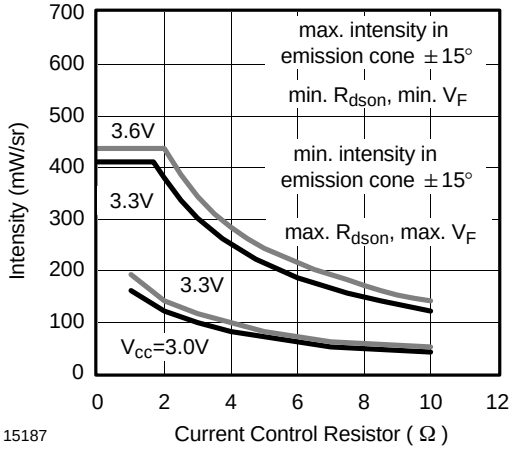


Figure 9. Intensity I_e vs. Current Control Resistor R1,
3 V Applications

Latency

The receiver is in specified conditions after the defined latency. In a UART related application after that time (typically 50 µs) the receiver buffer of the UART must be cleared. Therefore, the transceiver has to wait at least the specified latency after receiving the last bit before starting the transmission to be sure that the corresponding receiver is in a defined state.

Table 1. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1, C3	4.7 µF, 16 V	293D 475X9 016B 2T
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	47 Ω, 0.125 W	CRCW–1206–47R0–F–RT1
R2	5 V supply voltage: 14 Ω, 0.25 W (recommend using two 6.8 Ω, 0.125 W resistors in series) 3.0 V supply voltage: 4.5 Ω, 0.25 W (recommend using two 2.3 Ω, 0.125 W resistors in series)	CRCW–1206–6R80–F–RT2 CRCW–1206–2R26–F–RT1

Revision History:

A1.1a, 19/12/1999: Slightly changed feature description.
The pins 6 and 7 are exchanged by customer demand.

A1.2, 12/07/2000: Rxd Rise time and Fall time reduced typos corrected

A1.3, 13/10/2000: Typos corrected

A1.4, 01/11/2002: Eye safety statement adapted to the latest standard version

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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