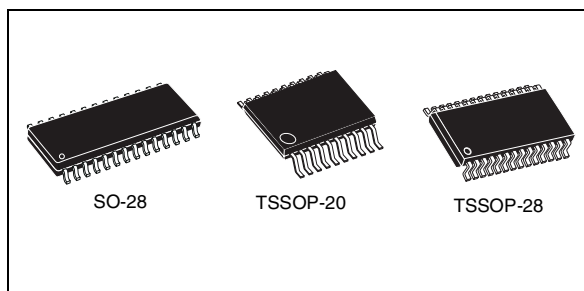


Features

- Designed to be compatible with the NDS conditional access system (except ST8024LTR)
- ISO 7816, GSM11.11 and EMV 4.2 (payment systems) compatible
- IC card interface
- 3 V or 5 V supply for the ST8024L device (V_{DD})
- Three specifically protected half-duplex bi-directional buffered I/O lines to card contacts C4, C7 and C8
- Step-up converter for V_{CC} generation separately powered by a $5\text{ V} \pm 20\%$ supply (V_{DDP} and PGND)
- $1.8\text{ V} \pm 6.5\%$, 3 V or $5\text{ V} \pm 5\%$ regulated card supply voltage (V_{CC}) with appropriate decoupling has the following capabilities:
 - $I_{CC} < 80\text{ mA}$ at $V_{DDP} = 4.75\text{ to }6.5\text{ V}$
 - Handles current spikes of 40 nA up to 20 MHz
 - Controls rise and fall times
 - Filtered overload detection at $\sim 120\text{ mA}$
- Thermal and short-circuit protection on all card contacts
- Automatic activation and deactivation sequences; initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, V_{DD} or V_{DDP} dropout



- Enhanced ESD protection on card side ($>6\text{ kV}$)
- 26 MHz integrated crystal oscillator
- Built-in debounce on card presence contacts
- One multiplexed status signal $\overline{OFF}$
- Non-inverted control of RST via pin RSTIN
- Clock generation for cards up to 20 MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
- Supply supervisor for spike-killing during power-on and power-off and power-on reset (threshold fixed internally or externally by a resistor divider)

Applications

- Smartcard readers for set-top boxes
- IC card readers for banking
- Identification, pay TV

Table 1. Device summary

Order code	PORADJ/ 1.8 V function	Temperature range	Package	Packaging	Package top mark
ST8024LCDR ⁽¹⁾	PORADJ	$-25\text{ to }85\text{ }^{\circ}\text{C}$	SO-28 (tape and reel)	1000 parts per reel	ST8024LC
ST8024LCTR ⁽¹⁾	PORADJ	$-25\text{ to }85\text{ }^{\circ}\text{C}$	TSSOP-28 (tape and reel)	2500 parts per reel	ST8024LC
ST8024LACDR ⁽¹⁾	1.8 V	$-25\text{ to }85\text{ }^{\circ}\text{C}$	SO-28 (tape and reel)	1000 parts per reel	ST8024LAC
ST8024LTR	1.8 V	$-25\text{ to }85\text{ }^{\circ}\text{C}$	TSSOP-20 (tape and reel)	2500 parts per reel	ST8024L
ST8024LACTR ⁽¹⁾	1.8 V	$-25\text{ to }85\text{ }^{\circ}\text{C}$	TSSOP-28 (tape and reel)	2500 parts per reel	ST8024LAC

1. Certified by NDS.

Contents

1	Description	5
2	Diagram	6
3	Pin configuration	7
4	Maximum ratings	9
5	Electrical characteristics	10
6	Functional description	18
6.1	Power supply	18
6.2	Voltage supervisor	18
6.2.1	Without external divider on pin PORADJ	18
6.2.2	With an external divider on pin PORADJ	19
6.2.3	Application examples	19
6.3	Clock circuitry (only on SO-28 and TSSOP-28 packages)	20
6.4	I/O transceivers	21
6.5	Inactive mode	21
6.6	Activation sequence	21
6.7	Active mode	23
6.8	Deactivation sequence	23
6.9	V _{CC} generator	24
6.10	Fault detection	25
6.11	V _{CC} selection settings	26
7	Applications	27
8	Package mechanical data	28
9	Revision history	34

List of tables

Table 1.	Device summary	1
Table 2.	Pin description	7
Table 3.	Absolute maximum ratings	9
Table 4.	Thermal data	9
Table 5.	Recommended operating conditions	9
Table 6.	Electrical characteristics over recommended operating condition	10
Table 7.	Step-up converter	11
Table 8.	Card supply voltage characteristics	11
Table 9.	Crystal connection (pins XTAL1 and XTAL2)	12
Table 10.	Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC, and AUX2UC)	12
Table 11.	Data lines to card reader (pins I/O, AUX1, and AUX2 with integrated 11 k Ω pull-up resistor to V _{CC})	13
Table 12.	Data lines to microcontroller (pins I/OUC, AUX1UC, and AUX2UC with integrated 11 k Ω pull-up resistor to V _{DD})	14
Table 13.	Internal oscillator	14
Table 14.	Reset output to card reader (pin RST)	14
Table 15.	Clock output to card reader (pin CLK)	15
Table 16.	Control inputs (pins CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, 5V/3V and PORADJ/1.8V)	15
Table 17.	Card presence inputs (pins PRES and $\overline{\text{PRES}}$)	16
Table 18.	Interrupt output (pin OFF NMOS drain with integrated 20 k Ω pull-up resistor to V _{DD})	16
Table 19.	Protection and limitation	16
Table 20.	Timing	16
Table 21.	Clock frequency selection	20
Table 22.	Card presence indicator	22
Table 23.	V _{CC} selection settings	26
Table 24.	SO-28 small outline, package mechanical data	28
Table 25.	TSSOP-20 package mechanical data	29
Table 26.	TSSOP-28 package mechanical data	30
Table 27.	SO-28 tape and reel mechanical data	31
Table 28.	TSSOP-20 tape and reel mechanical data	32
Table 29.	TSSOP-28 tape and reel mechanical data	33
Table 30.	Document revision history	34

List of figures

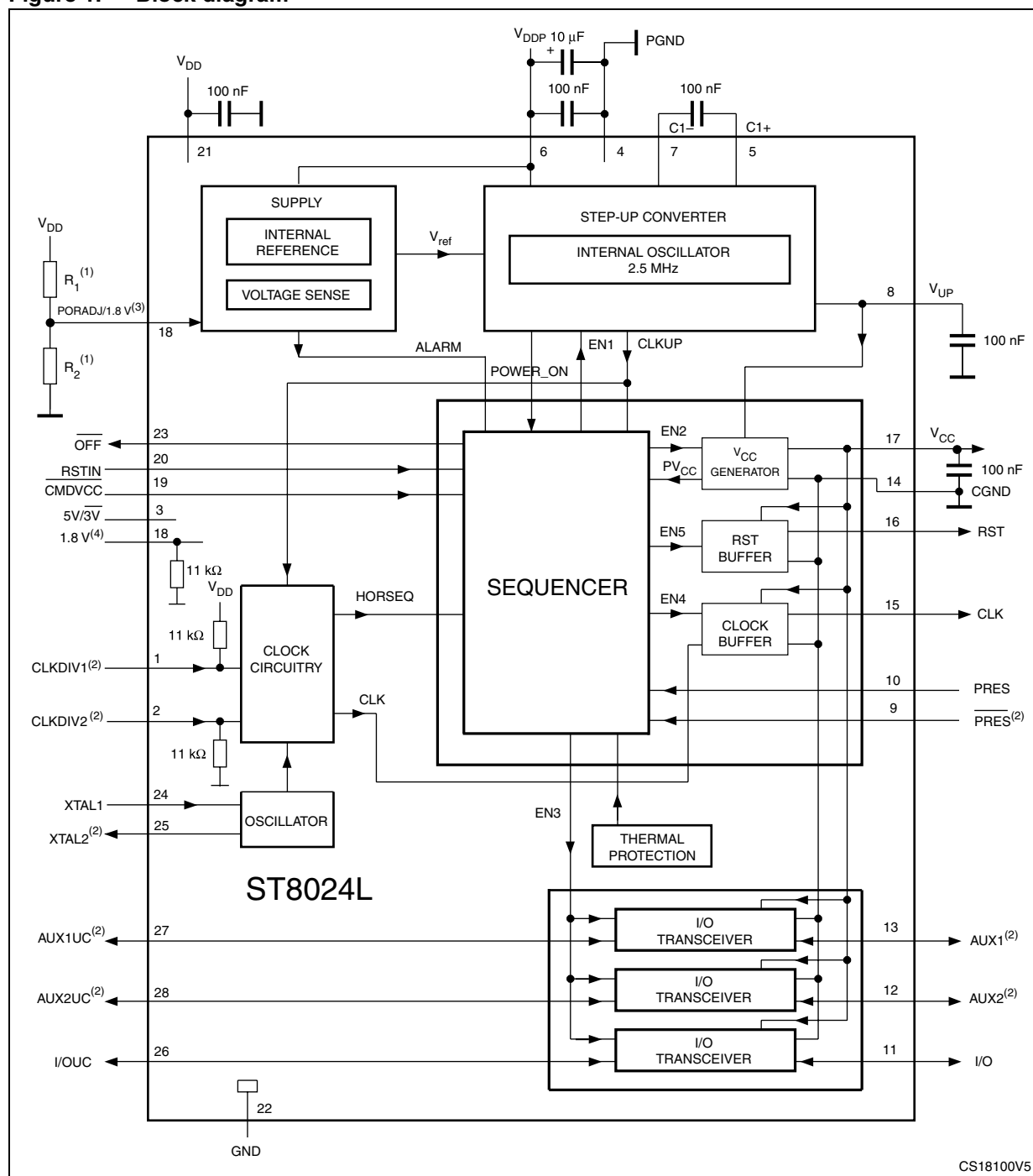
Figure 1.	Block diagram	6
Figure 2.	Pin connections	7
Figure 3.	Definition of output and input transition times	17
Figure 4.	Voltage supervisor	19
Figure 5.	Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$	22
Figure 6.	Activation sequence at t_3	23
Figure 7.	Deactivation sequence	24
Figure 8.	Behavior of $\overline{\text{OFF}}$, $\overline{\text{CMDVCC}}$, PRES, and V_{CC}	25
Figure 9.	Emergency deactivation sequence (card extraction)	26
Figure 10.	Hardware hookup	27
Figure 11.	SO-28 small outline, package mechanical drawing	28
Figure 12.	TSSOP-20 package mechanical drawing	29
Figure 13.	TSSOP-28 package mechanical drawing	30
Figure 14.	SO-28 tape and reel schematic	31
Figure 15.	TSSOP-20 tape and reel schematic	32
Figure 16.	TSSOP-28 tape and reel schematic	33

1 Description

The ST8024L is a complete low-cost analog interface for asynchronous Class A, B, and C smartcards. It can be placed between the card and the microcontroller with few external components to perform all supply protection and control functions. The ST8024LCDR and ST8024LCTR are compatible with the ST8024 (with the exception of $V_{th(ext)rise/fall}$ value).

2 Diagram

Figure 1. Block diagram



1. To be used with the PORADJ pin if needed.
2. Not available in the TSSOP-20L package.
3. ST8024LCDR, ST8024LCTR.
4. ST8024LACDR, ST8024LACTR, ST8024LTR.

3 Pin configuration

Figure 2. Pin connections

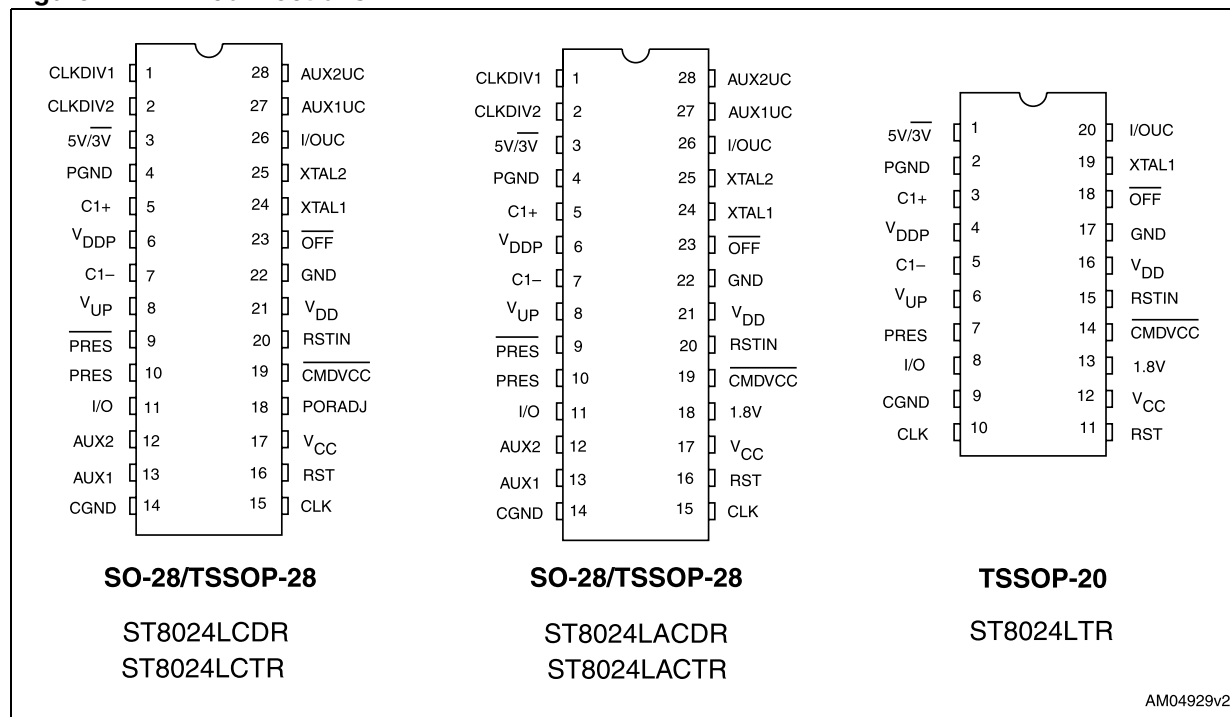


Table 2. Pin description

Symbol	Name and function	SO-28/ TSSOP-28	TSSOP-20
CLKDIV1	Control of CLK frequency (internal 11 kΩ pull-up resistor connected to V _{DD})	1	N. A.
CLKDIV2	Control of CLK frequency (internal 11 kΩ pull-down resistor connected to GND)	2	N. A.
5V/3V	5 V or 3 V V _{CC} selection for communication with the smartcard. Logic high selects 5 V operation and logic low selects 3 V operation (for ST8024LACDR, ST8024LACTR, and ST8024LTR: if the 1.8V pin is logic high, the 5V/3V pin is a "don't care"). See Table 23 for a description of the V _{CC} selection settings.	3	1
PGND	Power ground for step-up converter	4	2
C1+	External capacitor step-up converter	5	3
V _{DDP}	Power supply for step-up converter	6	4
C1-	External capacitor step-up converter	7	5
V _{UP}	Output of step-up converter	8	6
PRES	Card presence input (active low) - bonding option	9	N. A.
PRES	Card presence input (active high)	10	7
I/O	Data line to and from card (C7) (internal 11 kΩ pull-up resistor connected to V _{CC})	11	8

Table 2. Pin description (continued)

Symbol	Name and function	SO-28/ TSSOP-28	TSSOP-20
AUX2	Auxiliary line to and from card (C8) (internal 11 k Ω pull-up resistor connected to V _{CC})	12	N. A.
AUX1	Auxiliary line to and from card (C4) (internal 11 k Ω pull-up resistor to V _{CC})	13	N. A.
CGND	Ground for card signal (C5)	14	9
CLK	Clock to card (C3)	15	10
RST	Card reset (C2)	16	11
V _{CC}	Supply voltage for the card (C1)	17	12
PORADJ	Power-on reset threshold adjustment input (ST8024LCDR, ST8024LCTR)	18	N. A.
1.8V	1.8 V V _{CC} operation selection. Logic high selects 1.8 V operation and overrides any setting on the 5V/3V pin. With an internal 11 k Ω pull-down resistor to GND. (ST8024LACDR, ST8024LACTR and ST8024LTR)		13
$\overline{\text{CMDVCC}}$	Start activation sequence input (active low)	19	14
RSTIN	Card reset input from MCU	20	15
V _{DD}	Supply voltage	21	16
GND	Ground	22	17
$\overline{\text{OFF}}$	Interrupt to MCU (active low)	23	18
XTAL1	Crystal or external clock input	24	19
XTAL2	Crystal connection (leave this pin open if external clock is used)	25	N.A
I/OUC	MCU data I/O line (internal 11 k Ω pull-up resistor connected to V _{DD})	26	20
AUX1UC	Non-inverting receiver input (internal 11 k Ω pull-up resistor connected to V _{DD})	27	N. A.
AUX2UC	Non-inverting receiver input (internal 11 k Ω pull-up resistor connected to V _{DD})	28	N. A.

4 Maximum ratings

Table 3. Absolute maximum ratings⁽¹⁾

Symbol	Parameter	Min.	Max.	Unit
V_{DD}, V_{DDP}	Supply voltage	-0.3	7	V
V_{n1}	Voltage on pins XTAL1, XTAL2, $5V/\overline{3V}$, RSTIN, AUX2UC, AUX1UC, I/OUC, CLKDIV1, CLKDIV2, PORADJ/1.8V, CMDVCC, PRES, and $\overline{OFF}$	-0.3	$V_{DD} + 0.3$	V
V_{n2}	Voltage on card contact pins I/O, RST, AUX1, AUX2, and CLK	-0.3	$V_{CC} + 0.3$	V
V_{n3}	Voltage on pins V_{UP} , C1+, and C1-		7	V
ESD1	MIL-STD-883 class 3 on card contact pins, $\overline{PRES}$ and PRES ^{(2), (3)}	-6	6	kV
ESD2	MIL-STD-883 class 2 on μC contact pins and RSTIN ^{(2), (3)}	-2	2	kV
$T_{J(MAX)}$	Maximum operating junction temperature		150	°C
T_{STG}	Storage temperature range	-40	150	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. All card contacts are protected against any short with any other card contact.
3. Method 3015 (HBM, 1500 Ω , 100 pF) 3 positive pulses and 3 negative pulses on each pin referenced to ground.

Table 4. Thermal data

Symbol	Parameter	Condition	SO-28	TSSOP-20 TSSOP-28	Unit
R_{thJA}	Thermal resistance junction-ambient temperature	Multilayer test board (JEDEC standard)	56	50	°C/W

Table 5. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_A	Temperature range		-25		85	°C

5 Electrical characteristics

Table 6. Electrical characteristics over recommended operating condition

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7		6.5	V
V_{DDP}	Supply voltage for the step-up converter	$V_{CC} = 5\text{ V}; I_{CC} < 80\text{ mA}$	4.0	5	6.5	V
		$V_{CC} = 3\text{ V}; I_{CC} < 65\text{ mA}$	4.0	5	6.5	
		$V_{CC} = 5\text{ V}; I_{CC} < 20\text{ mA}$	3.0		6.5	
		$V_{CC} = 3\text{ V}; I_{CC} < 20\text{ mA}$	2.7		6.5	
		$V_{CC} = 1.8\text{ V}; I_{CC} < 20\text{ mA}$	2.7		6.5	
I_{DD}	Supply current	Card inactive			1.2	mA
		Card active; $f_{CLK} = f_{XTAL}$; $C_L = 30\text{ pF}$			1.5	
I_{DDP}	Step-up converter supply current	Inactive mode			0.1	mA
		Active mode; $f_{CLK} = f_{XTAL}$; $C_L = 30\text{ pF}$; $ I_{CC} = 0$			10	
		$V_{CC} = 5\text{ V}; I_{CC} = 80\text{ mA}$		50	200	
		$V_{CC} = 3\text{ V}; I_{CC} = 65\text{ mA}$		50	100	
		$V_{CC} = 1.8\text{ V}; I_{CC} = 45\text{ mA}$		30	60	
V_{th2}	Falling threshold voltage on V_{DD}	No external resistors at pin PORADJ; V_{DD} level falling. See Figure 4 .	2.35	2.45	2.55	V
V_{HYS2}	Hysteresis of threshold voltage V_{th2}	No external resistors at pin PORADJ. See Figure 4 .	50	100	150	mV
$V_{th(ext)rise}$	External rising threshold voltage at pin PORADJ	External resistor divider at pin PORADJ; V_{DD} level rising. See Section 6.2.2 .	1.17	1.20	1.23	V
$V_{th(ext)fall}$	External falling threshold voltage at pin PORADJ	External resistor divider at pin PORADJ; V_{DD} level falling. See Section 6.2.2 .	1.11	1.14	1.17	V
$V_{HYS(ext)}$	Hysteresis of threshold voltage $V_{th(ext)}$	External resistor divider at pin PORADJ. See Section 6.2.2 .	30	60	90	mV
$\Delta V_{HYS(ext)}$	Hysteresis of threshold voltage $V_{th(ext)}$ variation with temperature	External resistor divider at pin PORADJ			0.25	mV/K
t_W	Width of internal power-on reset pulse	No external resistor divider at pin PORADJ	4	8	12	ms
		External resistor divider at pin PORADJ	8	16	24	
I_L	Leakage current on pin PORADJ	$V_{PORADJ} < 0.5\text{ V}$	-0.1	4	10	μA
		$V_{PORADJ} > 1.0\text{ V}$	-1		1	
P_{TOT}	Total power dissipation	Continuous operation; $T_A = -25\text{ to }85\text{ }^\circ\text{C}$			0.56	W

1. $V_{DD} = 3.3\text{ V}$, $V_{DDP} = 5\text{ V}$, $f_{XTAL} = 10\text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25\text{ }^\circ\text{C}$.

Table 7. Step-up converter

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
f_{CLK}	Clock frequency	Card active	2.2		3.2	MHz
$V_{th(vd-vf)}$	Threshold voltage for step-up converter to change to voltage follower	5 V card	5.2	5.8	6.2	V
		3 V card	3.8	4.1	4.4	
		1.8 V card	3.8	4.1	4.4	
V_{UP}	Output voltage on pin V_{UP} (average value)	5 V card	5.2	5.7	6.2	V
		3 V card	3.5	3.9	4.3	
		1.8 V card	3.5	3.9	4.3	

1. $V_{DD} = 3.3$ V, $V_{DDP} = 5$ V, $f_{XTAL} = 10$ MHz, unless otherwise noted. Typical values are at $T_A = 25$ °C.

Table 8. Card supply voltage characteristics

Symbol	Parameter ⁽¹⁾	Test conditions		Min.	Typ.	Max.	Unit
C _{VCC}	External capacitance on pin V _{CC}	See ⁽²⁾		80		400	nF
V _{CC}	Card supply voltage (including ripple voltage)	Card inactive; I _{CC} = 0 mA	5 V, 3 V and 1.8 V card	-0.1	0	0.1	V
		Card inactive; I _{CC} = 1 mA	5 V, 3 V and 1.8 V card	-0.1	0	0.3	
		Card active; I _{CC} < 80 mA	5 V card	4.75	5	5.25	
		Card active; I _{CC} < 65 mA	3 V card	2.85	3	3.15	
		Card active; I _{CC} < 45 mA	1.8 V card	1.68	1.8	1.92	
		Card active; single current pulse I _P = −100 mA; t _p = 2 μs	5 V card	4.65	5	5.25	
		Card active; single current pulse I _P = −100 mA; t _p = 2 μs	3 V card	2.76	3	3.20	
		Card active; single current pulse I _P = −100 mA; t _p = 2 μs	1.8 V card	1.62	1.8	1.98	
		Card active; current pulses, Q _P = 40 nAs	5 V card	4.65	5	5.25	
			3 V card	2.76	3	3.20	
			1.8 V card	1.62	1.8	1.98	
		Card active; current pulses Q _P = 40 nAs with I _{CC} < 200 mA, t _p < 400 ns	5 V card	4.65	5	5.25	
			3 V card	2.76	3	3.20	
			1.8 V card	1.62	1.8	1.98	
V _{CC} (RIPPLE) (P-P)	Ripple voltage on V _{CC} (peak-to-peak value)	f _{RIPPLE} = 20 kHz to 200 MHz				350	mV

Table 8. Card supply voltage characteristics (continued)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Card supply current	$V_{CC} = 0$ to 5 V			80	mA
		$V_{CC} = 0$ to 3 V			65	
		$V_{CC} = 0$ to 1.8 V			45	
		V_{CC} short-circuit to GND	90		120	
S_R	Slew rate	Slew up or down, $V_{CC} = 5$ V; 3 V; 1.8 V; $I_{CC} < 30$ mA	0.08	0.15	0.22	V/ μ s

- $V_{DD} = 3.3$ V, $V_{DDP} = 5$ V, $f_{XTAL} = 10$ MHz, unless otherwise noted. Typical values are at $T_A = 25$ °C. (All parameters remain within limits but are tested only statistically for the temperature range. When a parameter is specified as a function of V_{DD} or V_{CC} it means their actual value at the moment of measurement.)
- To meet these specifications, pin VCC should be decoupled to CGND using two 100 nF ceramic multilayer capacitors of max. 350 m Ω ESR. If V_{CC} slew rate is not critical, the capacitance value can be up to 400 nF. (See [Figure 10](#)).

Table 9. Crystal connection (pins XTAL1 and XTAL2)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
$C_{XTAL1,2}$	External capacitance on pins XTAL1, XTAL2	Depends on type of crystal or resonator used		-	15	pF
f_{XTAL}	Crystal frequency		2	-	26	MHz
f_{XTAL1}	Frequency applied on pin XTAL1		0	-	26	MHz
V_{IH}	High level input voltage on pin XTAL1		0.7 V_{DD}	-	$V_{DD} + 0.3$	V
V_{IL}	Low level input voltage on pin XTAL1		-0.3	-	$+0.3$ V_{DD}	V

- $V_{DD} = 3.3$ V, $V_{DDP} = 5$ V, $f_{XTAL} = 10$ MHz, unless otherwise noted. Typical values are at $T_A = 25$ °C.

Table 10. Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC, and AUX2UC)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
$t_{D(I/O-I/OUC)}$, $t_{D(I/OUC-I/O)}$	I/O to I/OUC, I/OUC to I/O falling edge delay		-	-	200	ns
t_{PU}	Active pull-up pulse width		-	-	100	ns
$f_{I/O(MAX)}$	Maximum frequency on data lines		-	-	1	MHz
C_I	Input capacitance on data lines		-	-	10	pF

- $V_{DD} = 3.3$ V, $V_{DDP} = 5$ V, $f_{XTAL} = 10$ MHz, unless otherwise noted. Typical values are at $T_A = 25$ °C.

Table 11. Data lines to card reader (pins I/O, AUX1, and AUX2 with integrated 11 kΩ pull-up resistor to V_{CC})

Symbol	Parameter ⁽¹⁾	Test conditions		Min.	Typ.	Max.	Unit
V _{O(inactive)}	Output voltage	Inactive mode	No load	0		0.1	V
			I _{O(inactive)} = 1 mA			0.3	
I _{O(inactive)}	Output current	Inactive mode; pin grounded				-1	mA
V _{OH}	High level output voltage	No DC load		0.9 V _{CC}		V _{CC} + 0.1	V
		5 V and 3 V cards; I _{OH} < -40 μA		0.75 V _{CC}		V _{CC} + 0.1	
		1.8 V card I _{OH} < -40 μA		0.75 V _{CC}			
		I _{OH} ≥ 10 mA		0		0.4	
V _{OL}	Low level output voltage	I _{OL} = 1 mA		0		0.2	V
		I _{OL} ≥ 15 mA		V _{CC} - 0.4		V _{CC}	
V _{IH}	High level input voltage	5 V and 3 V cards		1.5		V _{CC} + 0.3	V
		1.8 V card		0.6 V _{CC}			
V _{IL}	Low level input voltage	5 V and 3 V cards		0.3		1.0	V
		1.8 V card		0		0.2	
I _{L IH}	High level input leakage current	V _{IH} = V _{CC}				10	μA
I _{L L}	Low level input current	V _{IL} = 0 V				600	μA
R _{PU}	Integrated pull-up resistor	Pull-up resistor to V _{CC}		9	11	13	kΩ
t _{T(DI)}	Data input transition time	V _{IL} max. to V _{IH} min.				1.2	μs
t _{T(DO)}	Data output transition time	V _O = 0 to V _{CC} ; C _L ≤ 80 pF; 10% to 90%				0.1	μs
I _{PU}	Current when pull-up active	V _{OH} = 0.9 V _{CC} ; C _L = 80 pF		-2			mA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{XTAL} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 12. Data lines to microcontroller (pins I/OUC, AUX1UC, and AUX2UC with integrated 11 k Ω pull-up resistor to V_{DD})

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V _{OH}	High level output voltage	5 V, 3 V and 1.8 V cards; I _{OH} < -40 μ A	0.75 V _{DD}		V _{DD} + 0.1	V
		No DC load	0.9 V _{DD}		V _{DD} + 0.1	
V _{OL}	Low level output voltage	I _{OL} = 1 mA	0		0.3	V
V _{IH}	High level input voltage		0.7 V _{DD}		V _{DD} + 0.3	V
V _{IL}	Low level input voltage		-0.3		0.3 V _{DD}	V
I _{L IH}	High level input leakage current	V _{IH} = V _{DD}			10	μ A
I _L	Low level input current	V _{IL} = 0 V			600	μ A
R _{PU}	Internal pull-up resistance to V _{DD}	Pull-up resistor to V _{DD}	9	11	13	k Ω
t _{T(DI)}	Data input transition time	V _{IL} max. to V _{IH} min.			1.2	μ s
t _{T(DO)}	Data output transition time	V _O = 0 to V _{DD} ; C _L < 30 pF; 10% to 90%			0.1	μ s
I _{PU}	Current when pull-up active	V _{OH} = 0.9 V _{DD} ; C _L = 30 pF	-1			mA

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{X_{TAL}} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 13. Internal oscillator

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
f _{OSC(INT)}	Frequency of internal oscillator	Inactive mode	55	140	200	kHz
		Active mode	2.2	2.7	3.2	MHz

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{X_{TAL}} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 14. Reset output to card reader (pin RST)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V _{O(inactive)}	Output voltage in inactive mode	I _{O(inactive)} = 1 mA	0	-	0.3	V
		No load	0	-	0.1	
I _{O(inactive)}	Output current	Inactive mode; pin grounded	0	-	-1	mA
t _{D(RSTIN-RST)}	RSTIN to RST delay	RST enable		-	2	μ s
V _{OL}	Low level output voltage	I _{OL} = 200 μ A	0	-	0.2	V
		I _{OL} = 20 mA (current limit)	V _{CC} - 0.4	-	V _{CC}	
V _{OH}	High level output voltage	I _{OH} = -200 μ A	0.9 V _{CC}	-	V _{CC}	V
		I _{OH} = -20 mA (current limit)	0	-	0.4	
t _R , t _F	Rise and fall time	C _L = 100 pF		-	0.1	μ s

1. V_{DD} = 3.3 V, V_{DDP} = 5 V, f_{X_{TAL}} = 10 MHz, unless otherwise noted. Typical values are at T_A = 25 °C.

Table 15. Clock output to card reader (pin CLK)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
$V_{O(inactive)}$	Output voltage in inactive mode	$I_{O(inactive)} = 1 \text{ mA}$	0	-	0.3	V
		No load	0	-	0.1	
$I_{O(inactive)}$	Output current	CLK inactive mode; pin grounded	0	-	-1	mA
V_{OL}	Low level output voltage	$I_{OL} = 200 \mu\text{A}$	0	-	0.3	V
		$I_{OL} = 70 \text{ mA}$ (current limit)	$V_{CC} - 0.4$	-	V_{CC}	
V_{OH}	High level output voltage	$I_{OH} = -200 \mu\text{A}$	$0.9 V_{CC}$	-	V_{CC}	V
		$I_{OH} = -70 \text{ mA}$ (current limit)	0	-	0.4	
t_R, t_F	Rise and fall time	$C_L = 30 \text{ pF}^{(2)}$		-	16	ns
δ	Duty factor (except for f_{XTAL})	$C_L = 30 \text{ pF}^{(2)}$	45	-	55	%
S_R	Slew rate	Slew up or down; $C_L = 30 \text{ pF}$	0.2	-		V/ns

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

2. Transition time and duty factor definitions are shown in [Figure 3](#); $d = t_1/(t_1 + t_2)$.

Table 16. Control inputs (pins CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, $5V/3V$ and PORADJ/1.8V)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage		-0.3		$0.3 V_{DD}$	V
V_{IH}	High level input voltage		$0.7 V_{DD}$		V_{DD}	V
$I_{L IH }$	High level input leakage current	$V_{IH} = V_{DD}$			1	μA
		$V_{IH} = V_{DD}$, 1.8V and CLKDIV2 pins with internal 11 k Ω pull-down resistor			800	μA
$I_{L IL }$	Low level input leakage current	$V_{IL} = 0$	-1			μA
		$V_{IL} = 0$, CLKDIV1 pin with internal 11 k Ω pull-up resistor	-800			μA
R_{PD}	Internal pull-down resistor to GND	Pull-down resistor to GND (1.8V and CLKDIV2 pins)	9	11	13	k Ω
R_{PU}	Internal pull-up resistor to V_{DD}	Pull-up resistor to V_{DD} (CLKDIV1 pin)	9	11	13	k Ω

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.
Pin $\overline{CMDVCC}$ is active low; pin RSTIN is active high; for CLKDIV1 and CLKDIV2 functions (see [Table 21](#)).

Table 17. Card presence inputs (pins PRES and $\overline{\text{PRES}}$)

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage		-0.3	-	$0.3 V_{DD}$	V
V_{IH}	High level input voltage		$0.7 V_{DD}$	-	$V_{DD} + 0.3$	V
$ I_{L IH} $	High level input leakage current	$V_{IH} = V_{DD}$		-	5	μA
$ I_{L IL} $	Low level input leakage current	$V_{IL} = 0$		-	5	μA

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.
Pin PRES is active low; pin $\overline{\text{PRES}}$ is active high, see [Figure 8](#) and [Figure 9](#); PRES has an integrated $1.25 \mu\text{A}$ current source to GND. ($\overline{\text{PRES}}$ to V_{DD}); the card is considered present if at least one of the inputs PRES or $\overline{\text{PRES}}$ is active.

Table 18. Interrupt output (pin $\overline{\text{OFF}}$ NMOS drain with integrated $20 \text{ k}\Omega$ pull-up resistor to V_{DD})

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	$I_{OL} = 2 \text{ mA}$	0		0.3	V
V_{OH}	High level output voltage	$I_{OH} = -15 \mu\text{A}$	$0.75 V_{DD}$			V
R_{PU}	Integrated pull-up resistor	$20 \text{ k}\Omega$ pull-up resistor to V_{DD}	16	20	24	$\text{k}\Omega$

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

Table 19. Protection and limitation

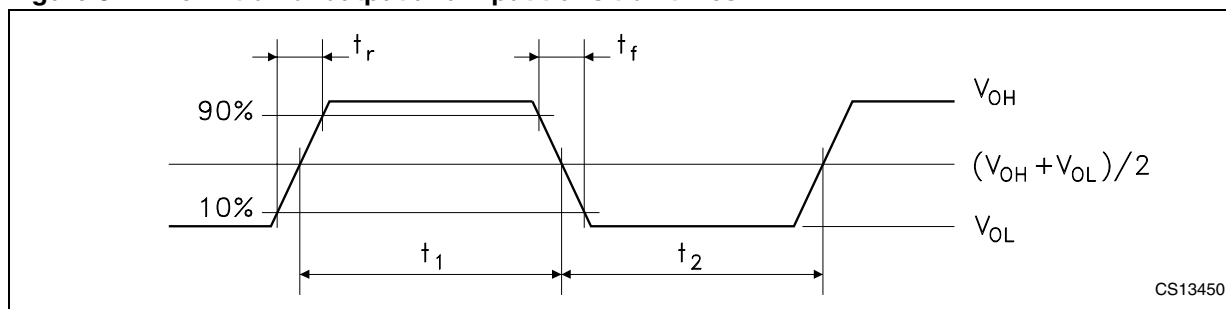
Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
$ I_{CC(SD)} $	Shutdown and limitation current pin V_{CC}		90		120	mA
$I_{I/O(lim)}$	Limitation current pins I/O, AUX1 and AUX2		-15		15	mA
$I_{CLK(lim)}$	Limitation current pin CLK		-70		70	mA
$I_{RST(lim)}$	Limitation current pin RST		-20		20	mA
T_{SD}	Shutdown temperature			150		$^\circ\text{C}$

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

Table 20. Timing

Symbol	Parameter ⁽¹⁾	Test conditions	Min.	Typ.	Max.	Unit
t_{ACT}	Activation time	For $V_{CC} = 5 \text{ V}$ (See Figure 5)	50		220	μs
t_{DE}	Deactivation time	(See Figure 7)	50	80	100	μs
t_3	Start of the window for sending CLK to card	(See Figure 6)			130	μs
t_5	End of the window for sending CLK to card	(See Figure 6)	140			μs
$t_{debounce}$	Debounce time pins PRES and $\overline{\text{PRES}}$	(See Figure 8)	5	8	11	ms

1. $V_{DD} = 3.3 \text{ V}$, $V_{DDP} = 5 \text{ V}$, $f_{XTAL} = 10 \text{ MHz}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$.

Figure 3. Definition of output and input transition times

6 Functional description

Throughout this document it is assumed that the reader is familiar with ISO7816 terminology.

6.1 Power supply

The supply pins for the ST8024L are V_{DD} and GND. V_{DD} should be in the range of 2.7 to 6.5 V. All signals interfacing with the system controller are referred to V_{DD} , therefore V_{DD} should also supply the system controller. All card reader contacts remain inactive during power-on or power-off.

The internal circuits are kept in the reset state until V_{DD} reaches $V_{th2} + V_{HYS2}$ and for the duration of the internal power-on reset pulse, t_W (see [Figure 4](#)). When V_{DD} falls below V_{th2} , an automatic deactivation of the contacts is performed.

A step-up converter is incorporated to generate the 1.8 V (for those devices with the 1.8V pin), 3 V, or 5 V card supply voltage (V_{CC}). The step-up converter should be supplied separately by V_{DDP} and PGND. Due to the possibility of large transient currents, the two 100 nF capacitors of the step-up converter should be located as near as possible to the ST8024L and have an ESR less than 350 m Ω .

During power-up, the V_{DD} supply voltage must be applied prior to the V_{DDP} supply voltage or at the same time

After powering the device, $\overline{OFF}$ remains low until $\overline{CMDVCC}$ is set high.

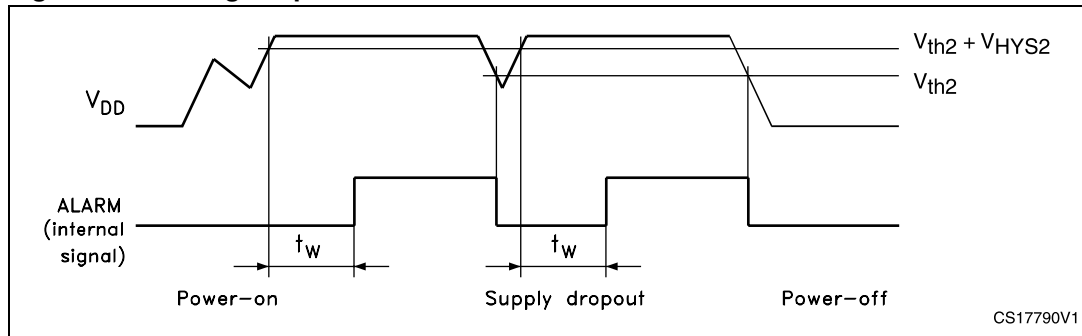
During power-off, $\overline{OFF}$ falls low when V_{DD} is below the falling threshold voltage.

6.2 Voltage supervisor

6.2.1 Without external divider on pin PORADJ

The voltage supervisor surveys the V_{DD} supply. A defined reset pulse of approximately 8 ms (t_W) is used internally to keep the ST8024L inactive during power-on or power-off of the V_{DD} supply (see [Figure 4](#)).

As long as V_{DD} is less than $V_{th2} + V_{HYS2}$, the ST8024L remains inactive regardless of the levels on the command lines. This state also lasts for the duration of t_W after V_{DD} has reached a level higher than $V_{th2} + V_{HYS2}$. When V_{DD} falls below V_{th2} , a deactivation sequence of the contacts is performed.

Figure 4. Voltage supervisor

6.2.2 With an external divider on pin PORADJ

In this case, a resistor divider is connected to the PORADJ pin (see [Figure 1](#)). $V_{th(ext) \text{ rise}}$ and $V_{th(ext) \text{ fall}}$ are the external rising threshold voltage and the external falling threshold voltages on pin PORADJ that switch the device on and off. By knowing these values and using the formula:

$$V_{DD} \text{ UVLO threshold (falling)} = (R_1 + R_2)/R_2 \times V_{th(ext) \text{ fall}}$$

$$V_{DD} \text{ UVLO threshold (rising)} = (R_1 + R_2)/R_2 \times V_{th(ext) \text{ rise}}$$

it is possible to set R_1 and R_2 in order to get suitable values for V_{DD} undervoltage (UVLO) thresholds, in order to turn the device on and off ($R_1 + R_2 = 100 \text{ k}\Omega$ typ.).

In particular, R_1 and R_2 must be set so that, when V_{DD} is getting low, before turning the microcontroller off, the smartcard must also be switched off properly. The same is true for the microcontroller startup - in such case the smartcard must be turned on after the microcontroller. The reset pulse width t_W is doubled to approximately 16 ms.

Input PORADJ is biased internally with a pull-down current source of 4 μA which is removed when the voltage on pin PORADJ exceeds 1 V.

This ensures that after detection of the external divider by the ST8024L during power-on, the input current on pin PORADJ does not cause inaccuracy of the divider voltage.

Note: The $V_{th(ext)}$ threshold of the ST8024L is slightly lower (by 80 mV typ.) than it was in the case of the ST8024 device. If, for example, the microcontroller is shut down at 2.5 V, the appropriate external resistor values must be chosen to ensure proper deactivation of the ST8024L device.

6.2.3 Application examples

The voltage supervisor is used as power-on reset and as supply dropout detection during a card session. Supply dropout detection is to ensure that a proper deactivation sequence is followed before the voltage is too low. For the internal voltage supervisor to function, the system microcontroller should operate down to 2.35 V to ensure a proper deactivation sequence. If this is not possible, external resistor values can be chosen to overcome the problem.

6.3 Clock circuitry (only on SO-28 and TSSOP-28 packages)

The card clock signal (CLK) is derived from a clock signal input to pin XTAL1 or from a crystal operating at up to 26 MHz connected between pins XTAL1 and XTAL2.

The clock frequency can be f_{XTAL} , $1/2 \times f_{XTAL}$, $1/4 \times f_{XTAL}$, or $1/8 \times f_{XTAL}$. Frequency selection is made via inputs CLKDIV1 and CLKDIV2 (see [Table 21](#)).

Table 21. Clock frequency selection⁽¹⁾

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

1. The status of pins CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10 ns minimum between changes is needed. The minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous, which means that during transition no pulse is shorter than 45% of the smallest period, and that the first and last clock pulses regarding the instant of change have the correct width.

When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command. The duty factor of f_{XTAL} depends on the signal present at pin XTAL1. In order to reach a 45 to 55% duty factor on pin CLK, the input signal on pin XTAL1 should have a duty factor of 48 to 52% and transition times of less than 5% of the input signal period.

If a crystal is used, the duty factor on pin CLK may be 45 to 55% depending on the circuit layout and on the crystal characteristics and frequency. In other cases, the duty factor on pin CLK is guaranteed between 45 and 55% of the clock period.

The crystal oscillator runs as soon as the ST8024L is powered up. If the crystal oscillator is used, or if the clock pulse on pin XTAL1 is permanent, the clock pulse is applied to the card as shown in the activation sequences in [Figure 5](#) and [Figure 6](#).

If the signal applied to XTAL1 is controlled by the system microcontroller, the clock pulse is applied to the card when it is sent by the system microcontroller (after completion of the activation sequence).

6.4 I/O transceivers

The three data lines I/O, AUX1, and AUX2 are identical. The idle state is realized by both I/O and I/OUC lines being pulled high via an 11 k Ω resistor (I/O to V_{CC} and I/OUC to V_{DD}). Pin I/O is referenced to V_{CC} , and pin I/OUC to V_{DD} , therefore allowing operation when V_{CC} is not equal to V_{DD} . The first side of the transceiver to receive a falling edge becomes the master. An anti-latch circuit disables the detection of falling edges on the line of the other side, which then becomes a slave. After a time delay $t_{d(edge)}$, an N transistor on the slave side is turned on, therefore transmitting the logic 0 present on the master side. When the master side returns to logic 1, a P transistor on the slave side is turned on during the time delay t_{PU} and then both sides return to their idle states. This active pull-up feature ensures fast low to high transitions; it is able to deliver more than 1 mA, at an output voltage of up to 0.9 V_{CC} , into an 80 pF load. At the end of the active pull-up pulse, the output voltage depends only on the internal pull-up resistor and the load current. The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.

6.5 Inactive mode

After a power-on reset, the circuit enters inactive mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive (approximately 200 Ω to GND)
- Pins I/OUC, AUX1UC, and AUX2UC are in the high impedance state (11 k Ω pull-up resistor to V_{DD}). Applies only to SO-28 and TSSOP-28 packages.
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active
- The internal oscillator is running at its low frequency.

6.6 Activation sequence

After power-on and after the internal pulse width delay, the system microcontroller can check the presence of a card using the signals $\overline{OFF}$ and $\overline{CMDVCC}$, as shown in [Table 22](#).

If the card is in the reader (this is the case if $\overline{PRES}$ or PRES is active), the system microcontroller can start a card session by pulling $\overline{CMDVCC}$ low. The following sequence then occurs (see [Figure 6](#)):

1. $\overline{CMDVCC}$ is pulled low and the internal oscillator changes to its high frequency (t_0).
2. The step-up converter is started (between t_0 and t_1).
3. V_{CC} rises from 0 to 5 V (or 1.8 V, 3 V) with a controlled slope ($t_2 = t_1 + 1.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 μ s).
4. I/O, AUX1, and AUX2 are enabled ($t_3 = t_1 + 4T$) (these were pulled low until this moment).
5. CLK is applied to the C3 contact of the card reader (t_4).
6. RST is enabled ($t_5 = t_1 + 7T$).

The clock may be applied to the card using the following sequence (see [Figure 5](#)):

- 1. Set $\overline{\text{RSTIN}}$ high.
- 2. Set $\overline{\text{CMDVCC}}$ low.
- 3. Reset RSTIN low between t_3 and t_5 ; CLK starts at this moment.
- 4. RST remains low until t_5 , when RST is enabled to be the copy of RSTIN .
- 5. After t_5 , RSTIN has no further affect on CLK ; this allows a precise count of CLK pulses before toggling RST .

If the applied clock is not needed, then $\overline{\text{CMDVCC}}$ may be set low with RSTIN low. In this case, CLK starts at t_3 (minimum 200 ns after the transition on I/O), and after t_5 , RSTIN may be set high in order to obtain an “answer to request” (ATR) from the card.

Activation should not be performed with RSTIN held permanently high.

Note: It is recommended that no control smartcard signals are to be shared with any other devices. Sharing may result in inadvertent activation or deactivation of the smartcard.

Table 22. Card presence indicator

$\overline{\text{OFF}}$	$\overline{\text{CMDVCC}}$	Indication
H	H	Card present
L	H	Card not present

Figure 5. Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$

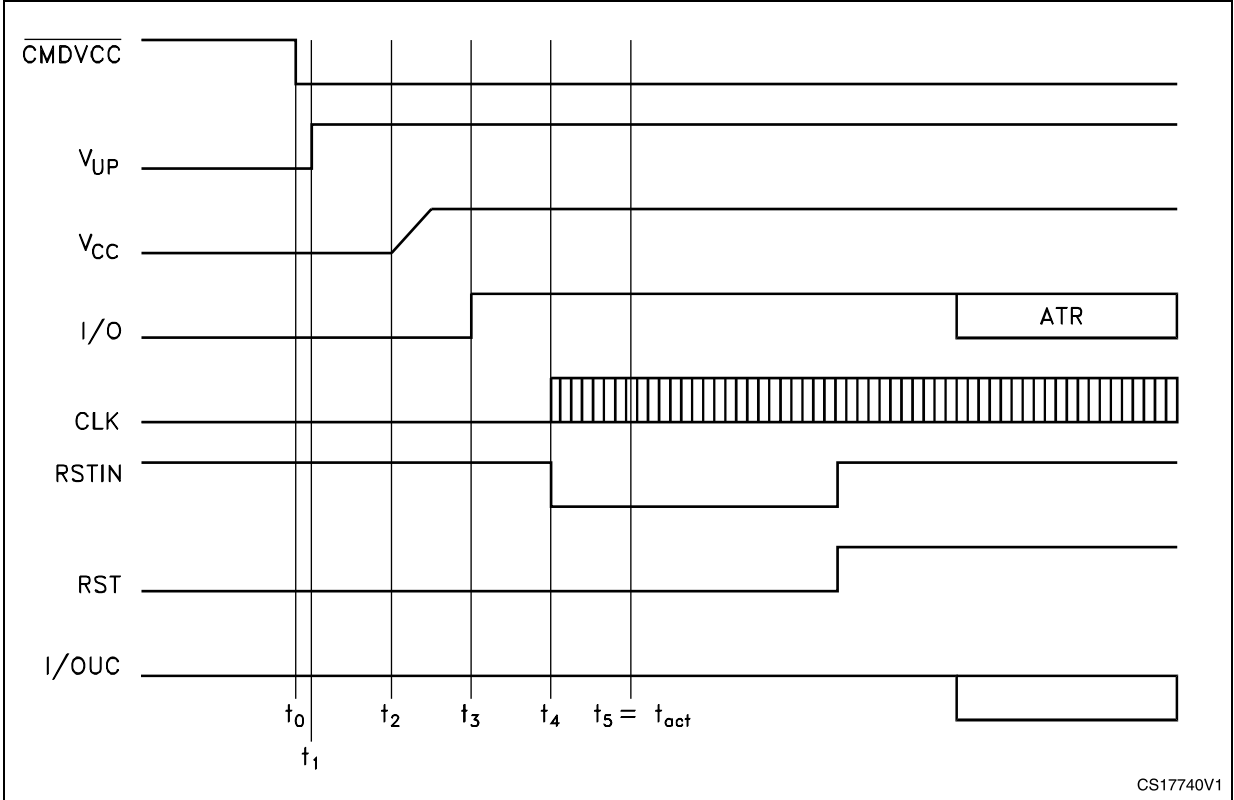
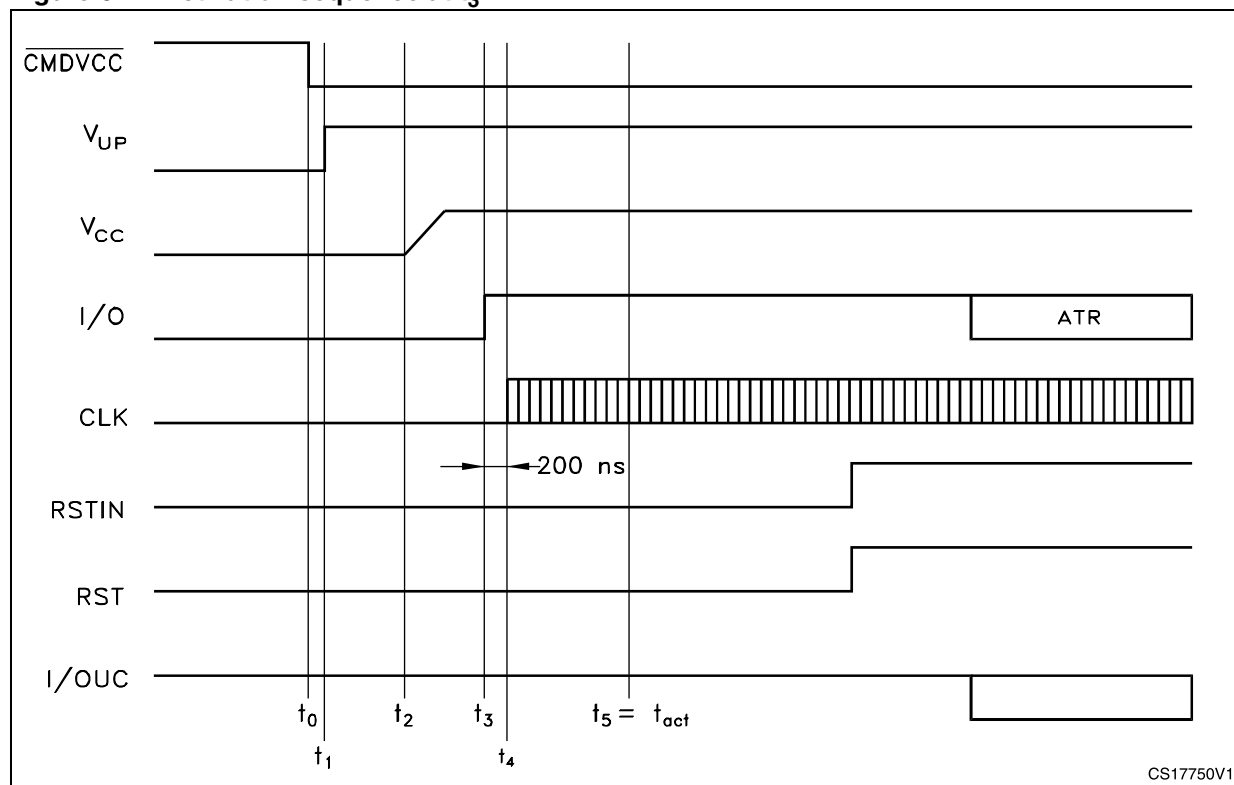


Figure 6. Activation sequence at t_3 

6.7 Active mode

When the activation sequence is completed, the ST8024L is in its active mode. Data are exchanged between the card and the microcontroller via the I/O lines.

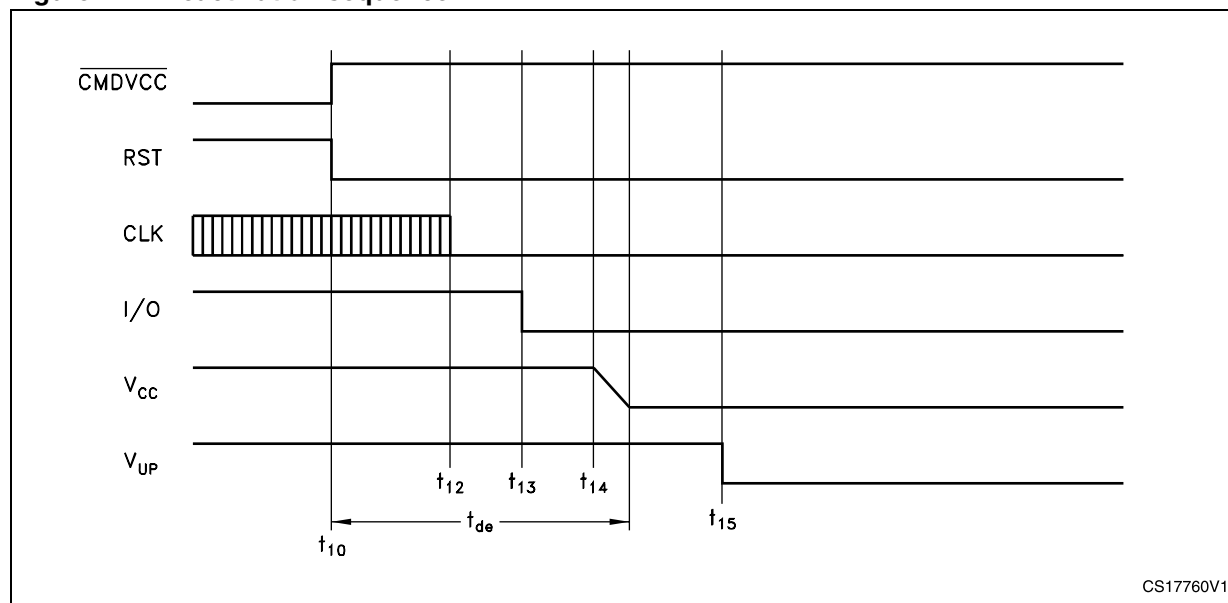
The ST8024L is designed for cards without V_{PP} (the voltage required to program or erase the internal non-volatile memory).

6.8 Deactivation sequence

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line HIGH. The circuit then executes an automatic deactivation sequence by counting the sequencer back and finishing in the inactive mode (see [Figure 7](#)):

1. RST goes low (t_{10}).
2. CLK is held low ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25 μs).
3. I/O , AUX1 , and AUX2 are pulled low ($t_{13} = t_{10} + T$).
4. V_{CC} starts to fall towards zero ($t_{14} = t_{10} + 1.5 \times T$).
5. The deactivation sequence is complete at t_{DE} , when V_{CC} reaches its inactive state.
6. All card contacts become low impedance to GND; I/OUC , AUX1UC , and AUX2UC remain at V_{DD} (pulled-up via an 11 k Ω resistor).
7. The internal oscillator returns to its lower frequency.

Figure 7. Deactivation sequence



6.9 V_{CC} generator

The V_{CC} generator has a capacity to supply up to 80 mA (max.) continuously at 5 V, 65 mA (max.) at 3 V, and 45 mA (max.) at 1.8 V. An internal overload detector operates at approximately 120 mA. Current samples to the detector are internally filtered, allowing spurious current pulses up to 200 mA with a duration in the order of μ s to be drawn by the card without causing deactivation. The average current must stay below the specified maximum current value. For reasons of V_{CC} voltage accuracy, a 100 nF capacitor with an ESR < 350 m Ω should be tied to CGND near to pin V_{CC}, and a 100 nF capacitor with the same ESR should be tied to CGND near card reader contact C1.

6.10 Fault detection

The following fault conditions are monitored:

- Short-circuit or high current on V_{CC}
- Removal of a card during a transaction
- V_{DD} dropping
- Step-up converter operating out of the specified values (V_{DDP} too low or current from V_{UP} too high)
- Overheating
- There are two different cases (see [Figure 8](#)):
 - $\overline{CMDVCC}$ high outside a card session. Output $\overline{OFF}$ is low if a card is not in the card reader, and high if a card is in the reader. A voltage drop on the V_{DD} supply is detected by the supply supervisor, this generates an internal power-on reset pulse but does not act upon $\overline{OFF}$. No short-circuit or overheating is detected because the card is not powered-up.
 - $\overline{CMDVCC}$ low within a card session. Output $\overline{OFF}$ goes low when a fault condition is detected. As soon as this occurs, an emergency deactivation is performed automatically (see [Figure 9](#)). When the system controller resets $\overline{CMDVCC}$ to high, it may sense the $\overline{OFF}$ level again after completing the deactivation sequence. This distinguishes between a hardware problem or a card extraction ($\overline{OFF}$ goes high again if a card is present).

Depending on the type of card-present switch within the connector (normally closed or normally open) and on the mechanical characteristics of the switch, bouncing may occur on the PRES signals at card insertion or withdrawal.

There is a debounce feature in the device with an 8 ms typical duration (see [Figure 8](#)). When a card is inserted, output $\overline{OFF}$ goes high only at the end of the debounce time.

When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES or $\overline{PRES}$ and output $\overline{OFF}$ goes low.

Figure 8. Behavior of $\overline{OFF}$, $\overline{CMDVCC}$, PRES, and V_{CC}

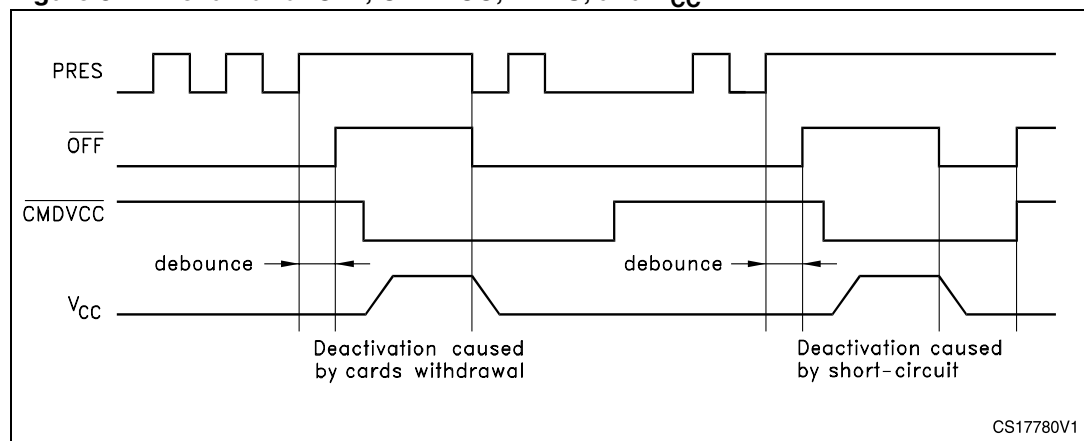
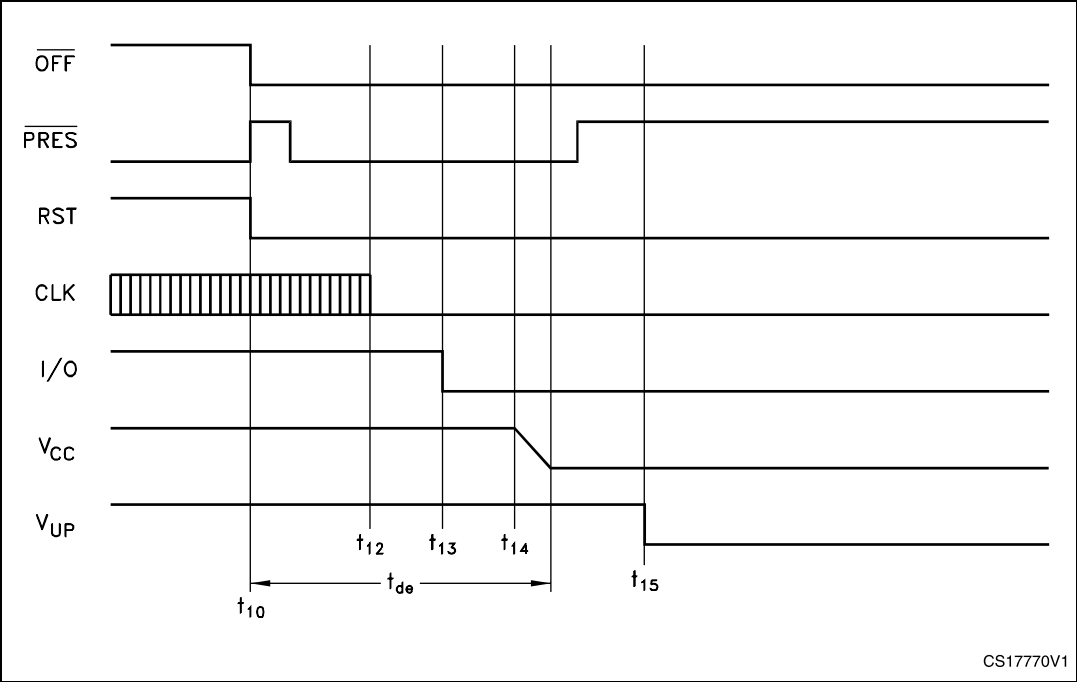


Figure 9. Emergency deactivation sequence (card extraction)



CS17770V1

6.11 V_{CC} selection settings

The ST8024L supports three smartcard V_{CC} voltages: 1.8 V, 3 V, and 5 V. The V_{CC} selection is controlled by the 1.8V and 5V/ $\overline{3V}$ signals as shown in [Table 23](#). The 1.8V signal has priority over the 5V/ $\overline{3V}$. When the 1.8 V pin is taken high, V_{CC} is 1.8 V and it overrides any setting on the 5V/ $\overline{3V}$ pin.

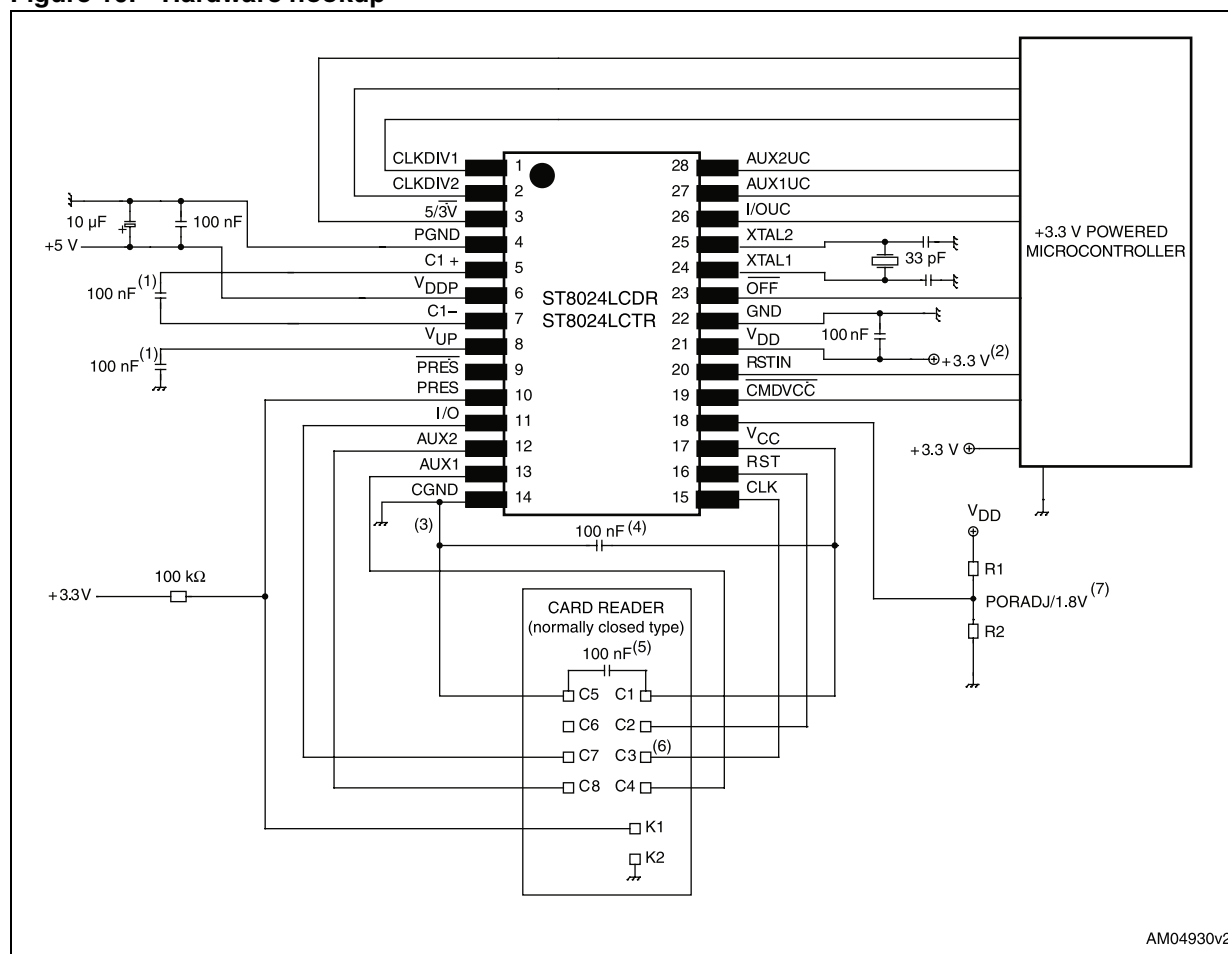
When the 1.8V pin is taken low, the 5V/ $\overline{3V}$ pin selects the 5 V or 3 V V_{CC} . If the 5V/ $\overline{3V}$ pin is taken high, then V_{CC} is 5 V, and if the 5V/ $\overline{3V}$ pin is taken low then V_{CC} is 3 V.

Table 23. V_{CC} selection settings

5V/ $\overline{3V}$ pin	1.8V pin	V_{CC} output
0	0	3 V
1	0	5 V
x	1	1.8 V

7 Applications

Figure 10. Hardware hookup



1. These capacitors must be $< 350\text{ m}\Omega$ ESR and be placed near the IC (within 10 mm).
2. ST8024L and the microcontroller must use the same V_{DD} supply.
3. Make short, straight connections between CGND, C5, and the ground connection to the capacitor.
4. Mount one ESR-type ($< 350\text{ m}\Omega$) 100 nF capacitor close to pin V_{CC} .
5. Mount one ESR-type ($< 350\text{ m}\Omega$) 100 nF capacitor close to C1 contact.
6. The connection to C3 should be routed as far as possible from C2, C7, C4, and C8 and, if possible, surrounded by grounded tracks.
7. This is the optional resistor divider for changing the threshold of V_{DD} when using the PORADJ function. If this divider is not required, pin 18 should be connected to ground.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 11. SO-28 small outline, package mechanical drawing

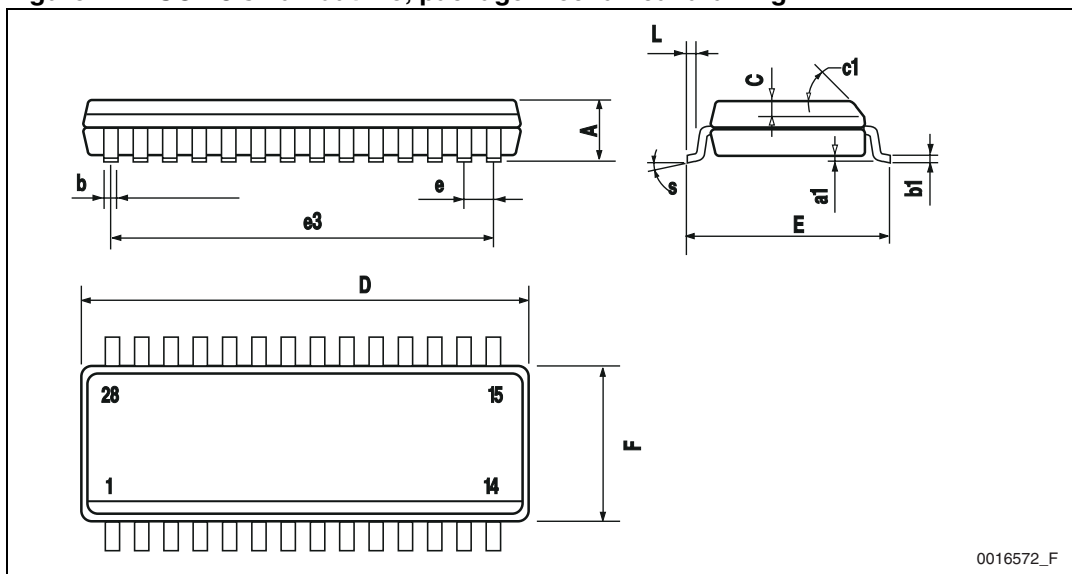


Table 24. SO-28 small outline, package mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	17.70		18.10	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					

Figure 12. TSSOP-20 package mechanical drawing

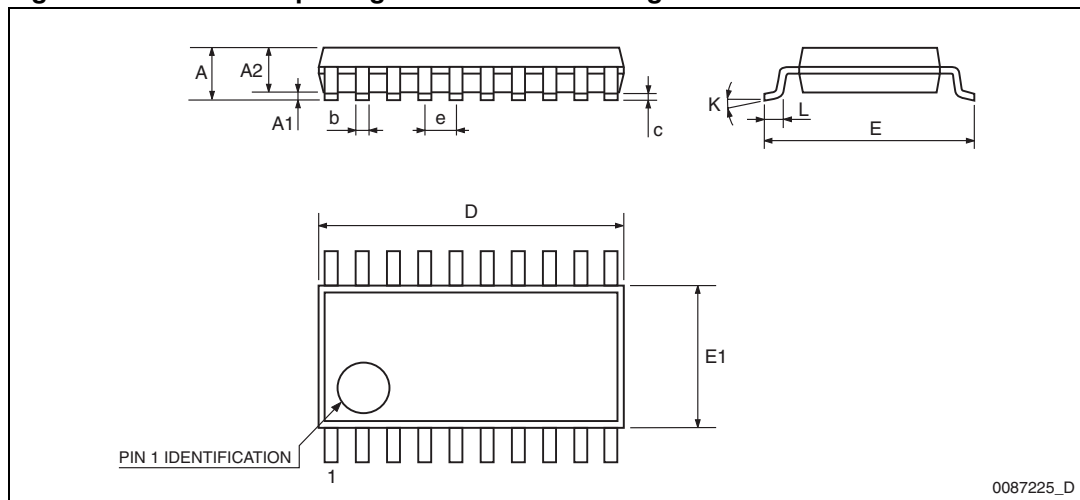


Table 25. TSSOP-20 package mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 13. TSSOP-28 package mechanical drawing

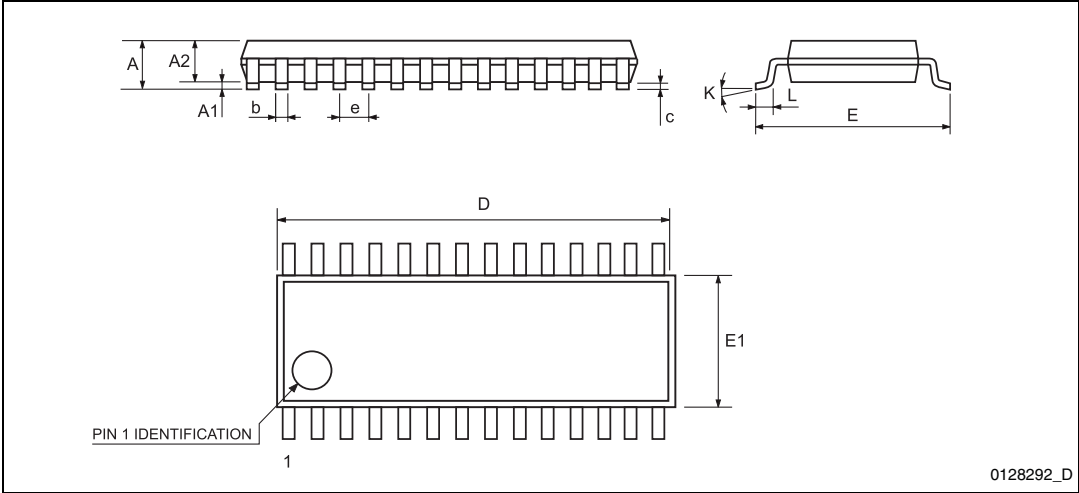


Table 26. TSSOP-28 package mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	9.6	9.7	9.8	0.378	0.382	0.386
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 14. SO-28 tape and reel schematic

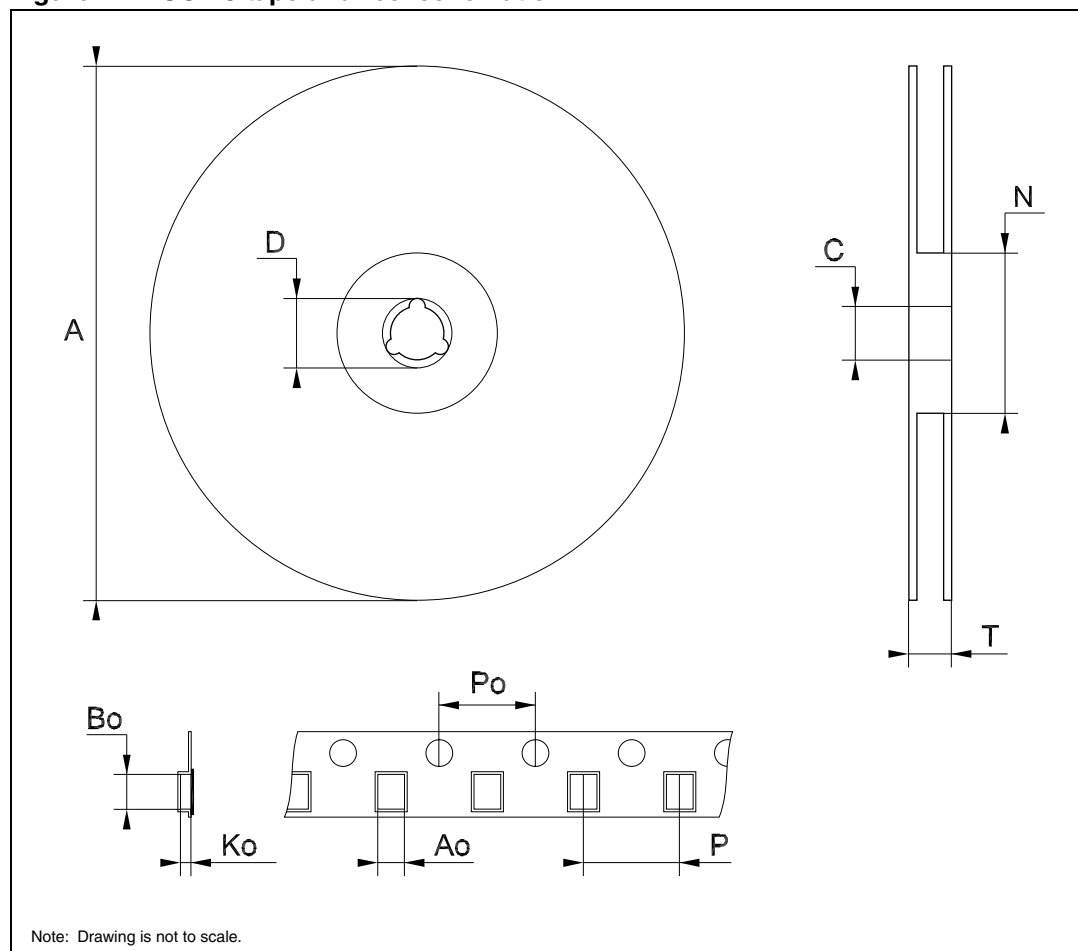


Table 27. SO-28 tape and reel mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
A _O	10.8		11.0	0.425		0.433
B _O	18.2		18.4	0.716		0.724
K _O	2.9		3.1	0.114		0.122
P _O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 15. TSSOP-20 tape and reel schematic

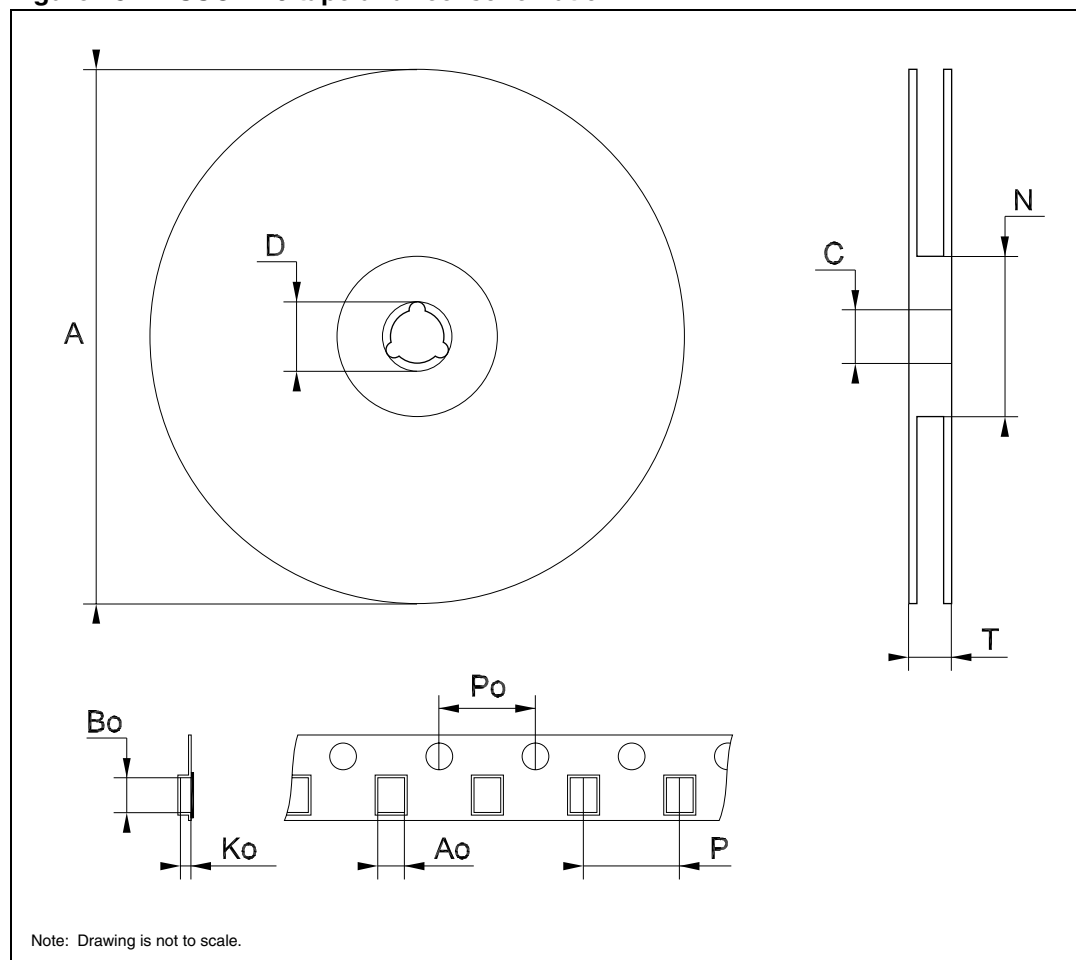


Table 28. TSSOP-20 tape and reel mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
A _O	6.8		7	0.268		0.276
B _O	6.9		7.1	0.272		0.280
K _O	1.7		1.9	0.067		0.075
P _O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 16. TSSOP-28 tape and reel schematic

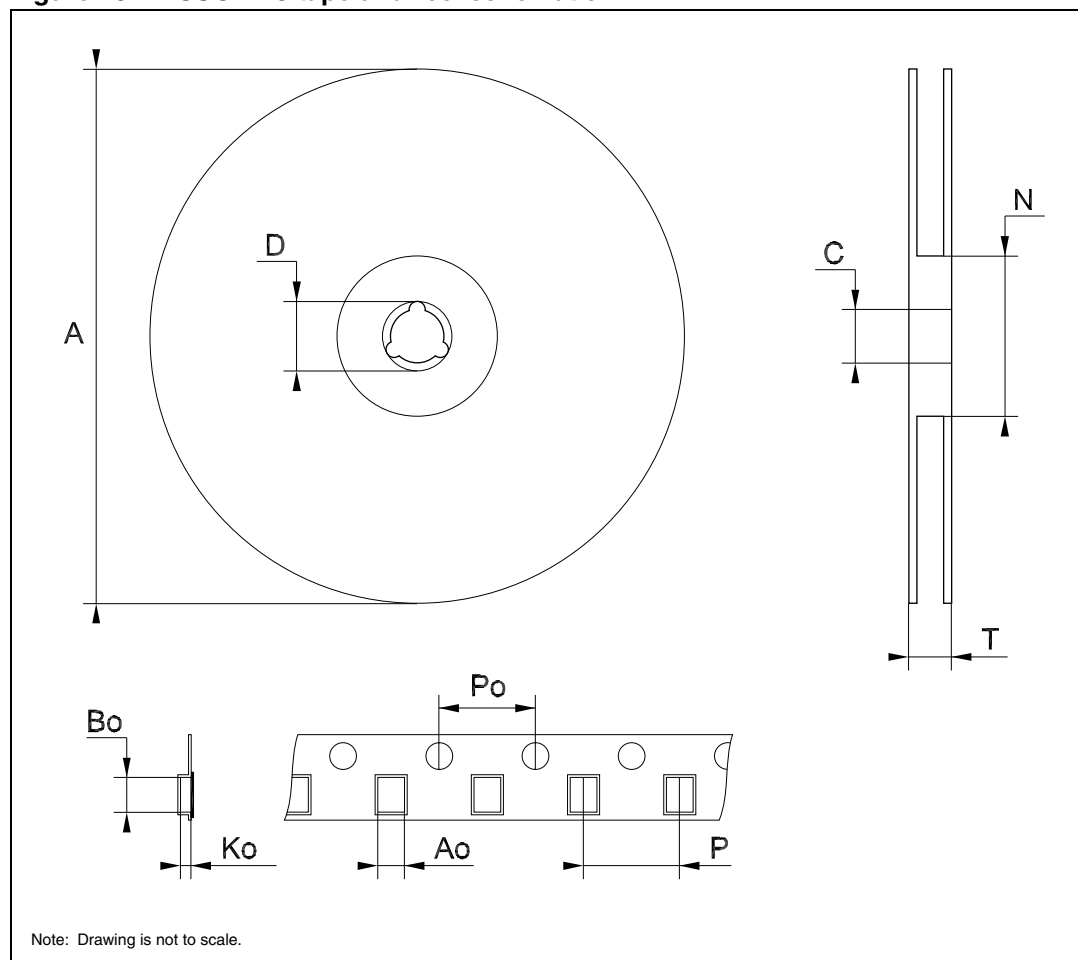


Table 29. TSSOP-28 tape and reel mechanical data

Symbol	Dimensions					
	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
A _O	6.8		7	0.268		0.276
B _O	10.1		10.3	0.398		0.406
K _O	1.7		1.9	0.067		0.075
P _O	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

9 Revision history

Table 30. Document revision history

Date	Revision	Changes
19-Jul-2010	1	Initial release.
30-Jul-2010	2	Updated Description , Table 6 .
27-Sep-2010	3	Updated Features , Table 1 , 6 , 8 , 19 , 20 , Section 6.1 , Section 6.2.2 , Section 6.6 , Section 6.9 , footnotes of Figure 10 .
09-Feb-2012	4	Added ST8024LACTR device, updated Features , Table 1 , Section 1: Description (moved to page 5), Figure 1 , Figure 2 , Table 2 , Table 6 , Table 8 , Section 6.1 to Section 6.3 , Figure 10 and Disclaimer, minor text corrections throughout document.
04-May-2012	5	Updated Figure 1 , Table 2 , Table 3 , Table 6 , Table 8 , Table 14 , Table 16 , Table 17 , Section 6.1 , moved notes from Section 5 below Table 3 , Table 8 , Table 15 , Table 16 , Table 17 , minor text corrections throughout document.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

