National Semiconductor

CLC401
Fast Settling, Wideband High-Gain Monolithic Op Amp

General Description

The CLC401 is a wideband, fast-settling op amp designed for applications requiring gains greater than ±7. Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high-speed monolithic op amps. For example, at a gain of +20, the −3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2° deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high-frequency amplification – requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ±7 to ±50 gain range precludes the need for external compensation. And, unlike many other high-speed op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is based on National's proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figures 1 and 2, page 4). How-

(Continued on page 4)

The CLC401 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC401AJP	-40°C to +85°C	8-pin plastic DIP
CLC401AJE	-40°C to +85°C	8-pin plastic SOIC
CLC401A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-833, Level B

DESC SMD number: 5962-89973

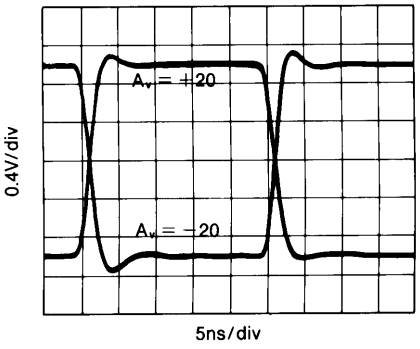
Features

- -3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- Low power, 150mW
- Overload and short circuit protected
- Stable without compensation
- Recommended gain range, ±7 to ±50

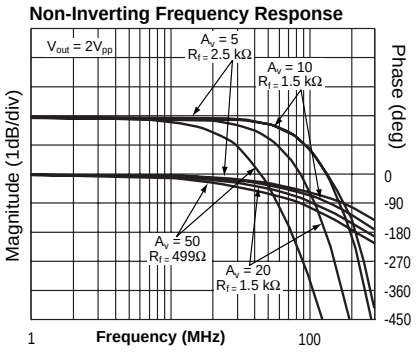
Applications

- Flash, precision A/D conversion
- Photodiode, CCD preamps
- IF processors
- High-speed modems, radios
- Line drivers
- DC-coupled log amplifiers
- High-speed communications

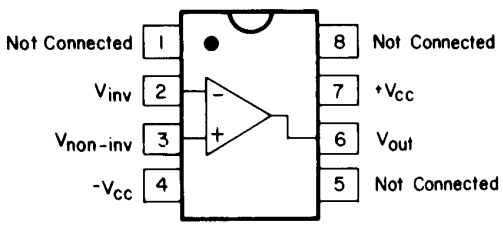
Pulse Response



Non-Inverting Frequency Response



Pinout
DIP & SOIC



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CLC401 Electrical Characteristics (A_V = +20, V_{CC} = ±5V, R_L = 100Ω, R_f = 1.5kΩ; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC401AJ	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
−3dB bandwidth	V_{out}<2V_{pp}	150	>100	>100	>70	MHz	SSBW
	V_{out}<5V_{pp}	100	>65	>65	>55	MHz	LSBW
gain flatness	V_{out}<2V_{pp}						
peaking	<25MHz	0	<0.1	<0.1	<0.1	dB	GFPL
peaking	>25MHz	0	<0.2	<0.2	<0.2	dB	GFPH
rolloff	<50MHz	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 50MHz	0.2	<1.0	<1.0	<1.5	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.5	<3.5	<3.5	<5.0	ns	TRS
	5V step	5	<7.0	<7.0	<8.0	ns	TRL
settling time to ±0.1%	2V step	10	<15	<15	<15	ns	TS
overshoot	2V step	0	<10	<10	<10	%	OS
slew rate		1200	>800	>800	>700	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 20MHz	−45	<−35	<−35	<−35	dBc	HD2
3rd harmonic distortion	2V_{pp}, 20MHz	−60	<−50	<−50	<−45	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−158	<−155	<−155	<−154	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz	35	<50	<50	<55	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		3	±10.0	±6.0	±11.0	mV	VIO
average temperature coefficient		20	±50	—	±50	μV/°C	DVIO
*input bias current	non-inverting	10	±36	±20	±20	μA	IBN
average temperature coefficient		100	±200	—	±100	nA/°C	DIBN
*input bias current	inverting	10	46	30	40	μA	IBI
average temperature coefficient		100	±200	—	±100	nA/°C	DIBI
power supply rejection ratio		55	50	50	50	dB	PSRR
common mode rejection ratio		55	50	50	50	dB	CMRR
*supply current	no load	15	21	21	21	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	200	>50	>100	>100	kΩ	RIN
	capacitance	0.5	<2.5	<2.5	<2.5	pF	CIN
output impedance	at DC	0.2	<0.3	<0.3	<0.3	Ω	RO
output voltage range	no load	3.5	>3.0	>3.2	>3.2	V	VO
common mode input range	for rated performance	2.8	>2.0	>2.5	>2.5	V	CMIR
output current		60	>35	>50	>50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	60mA
common mode input voltage	±V_{CC}
differential input voltage	5V
junction temperature range	+150°C
operating temperature range	
AJ:	− 40°C to + 85°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+300°C)	10 sec

Miscellaneous Ratings

recommended gain range: +7 to +50, -1 to -50

NOTES: * AJ 100% tested at +25°C.

Package Thermal Resistance

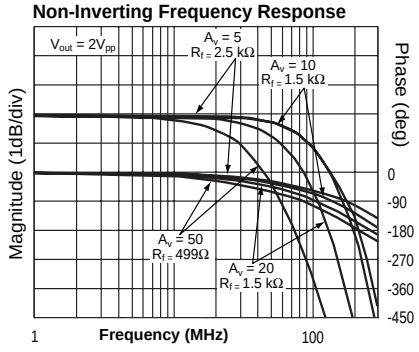
Package	θ_{JC}	θ_{JA}
AJP	70°C/W	125°C/W
AJE	65°C/W	145°C/W

Reliability Information

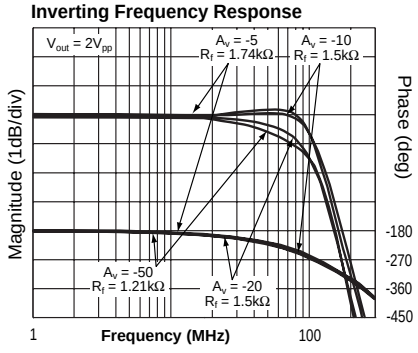
Transistor count	28

CLC401 Typical Performance Characteristics (T_A = 25°, A_V = +20, V_{CC} = ±5V, R_L = 100Ω; unless specified)

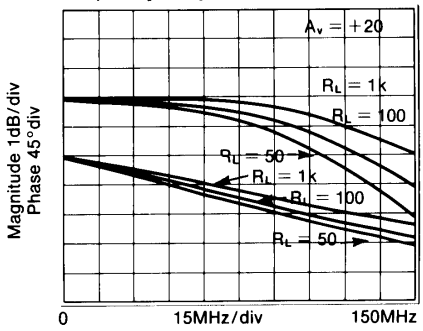
Non-Inverting Frequency Response



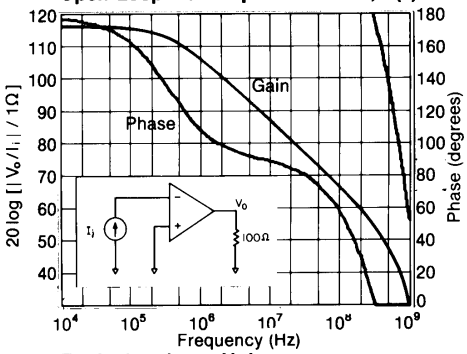
Inverting Frequency Response



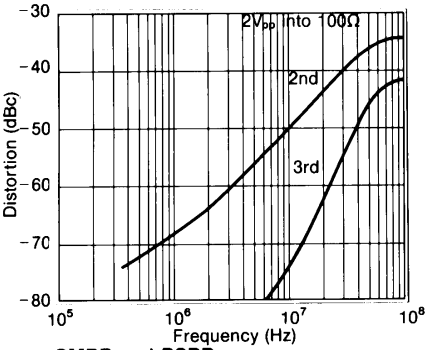
Frequency Response for Various R_Ls



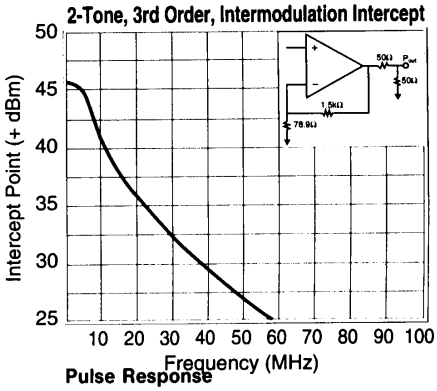
Open-Loop Transimpedance Gain, Z(s)



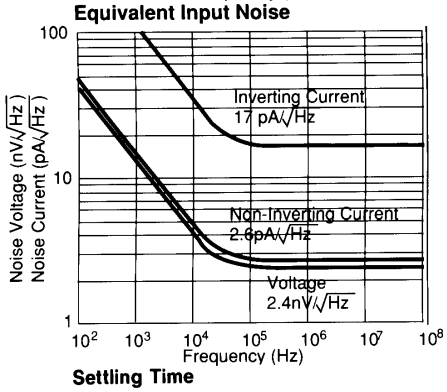
2nd and 3rd Harmonic Distortion



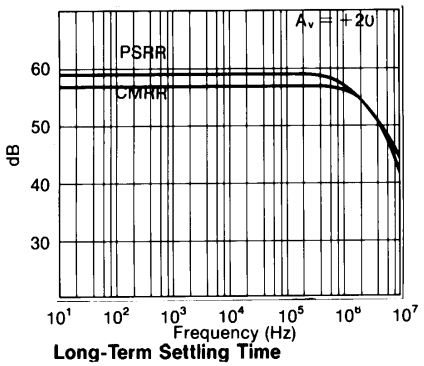
2-Tone, 3rd Order, Intermodulation Intercept



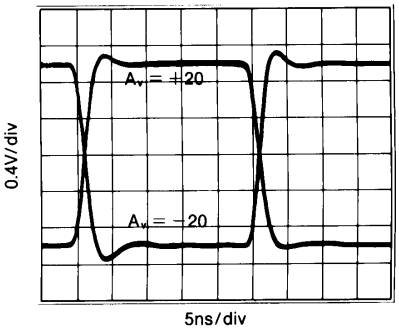
Equivalent Input Noise



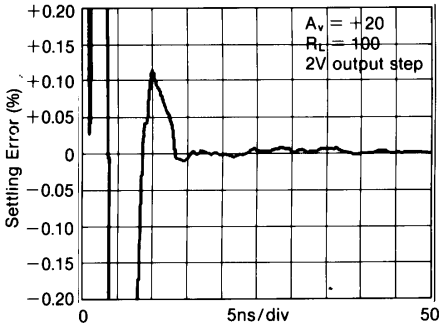
CMRR and PSRR



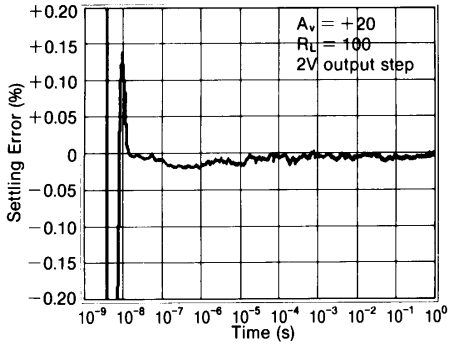
Pulse Response



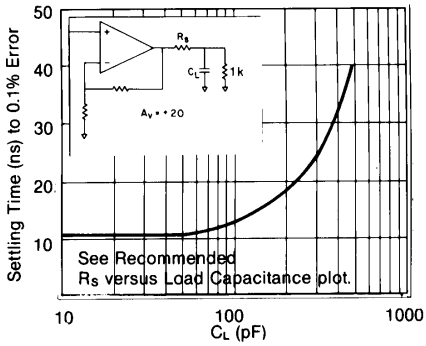
Settling Time



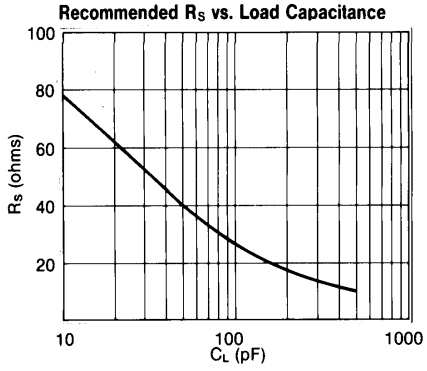
Long-Term Settling Time



Settling Time vs. Load Capacitance



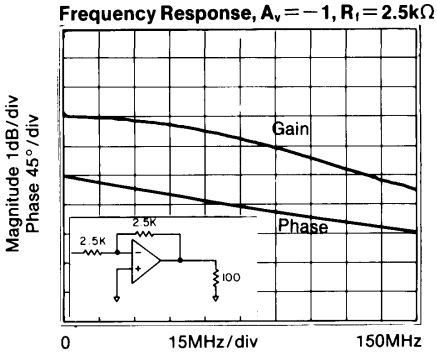
Recommended R_S vs. Load Capacitance

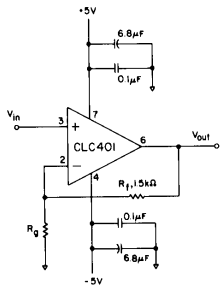


Low Gain & Transimpedance Applications

The CLC401 may be used at gains down to unity ($A_v = \pm 1$) by choosing R_f according to Equation (4) on the following page. The curves to the right show performance at inverting unity gain with R_f = 2500Ω, a configuration appropriate for D/A converter buffering and other transimpedance applications.

Frequency Response, $A_v = -1$, $R_f = 2.5k\Omega$



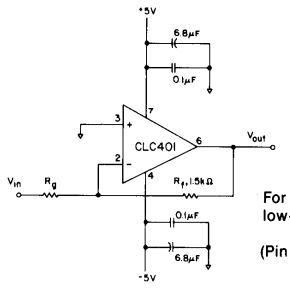


$$A_v = 1 + \frac{R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 1: recommended non-inverting gain circuit



$$A_v = \frac{-R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 2: recommended inverting gain circuit

ever, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Understanding the Loop Gain

Referring to the equivalent circuit of Figure 3, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plot on page 3. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

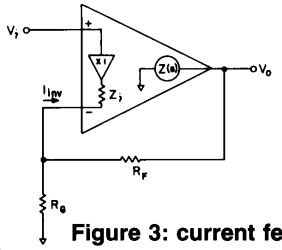


Figure 3: current feedback topology

Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f/R_g}{1 - 1/LG} \qquad \text{eq. (1)}$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i/(R_f \,||\, R_g)} \qquad \text{eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$. (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1.) Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 1.5k\Omega$, yields a large loop gain at DC. As a result, equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 1.5k\Omega$.** Increasing R_f from 1.5kΩ will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC401 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC401, $Z_i \cong 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by equation 2. The second term in equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \,||\, R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC401 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm \text{IBN} \times R_s (1 + R_f/R_g) \pm \text{VIO} (1 + R_f/R_g) \pm \text{IBI} \times R_f \qquad \text{eq. (3)}$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5kΩ with the CLC401—this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 1.5k\Omega$ and $R_g = 79\Omega$). For the CLC401 this gives,

$$R_f = 2500 - 50A_v \text{ and } R_g = \frac{2500 - 50A_v}{A_v - 1} \qquad \text{eq. (4)}$$

where A_v is the desired non-inverting gain. Note that with $A_v = +20$ we get the specified $R_f = 1.5k\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC401 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC401.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. CLC730013 for through-hole and CLC730027 for SOIC) for the CLC401 are available.

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