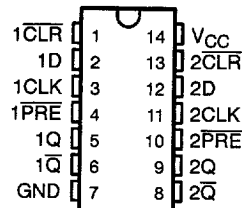


SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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- **EPIC™** (Enhanced-Performance Implanted CMOS) 2- μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LV74 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV74 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

† This configuration is nonstable; that is, it will not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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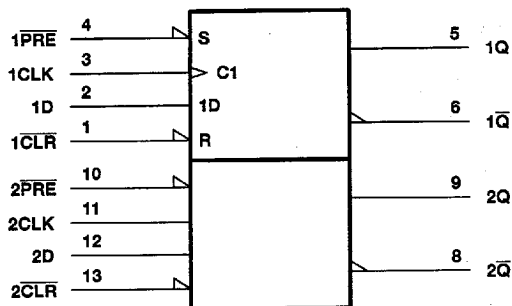
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SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

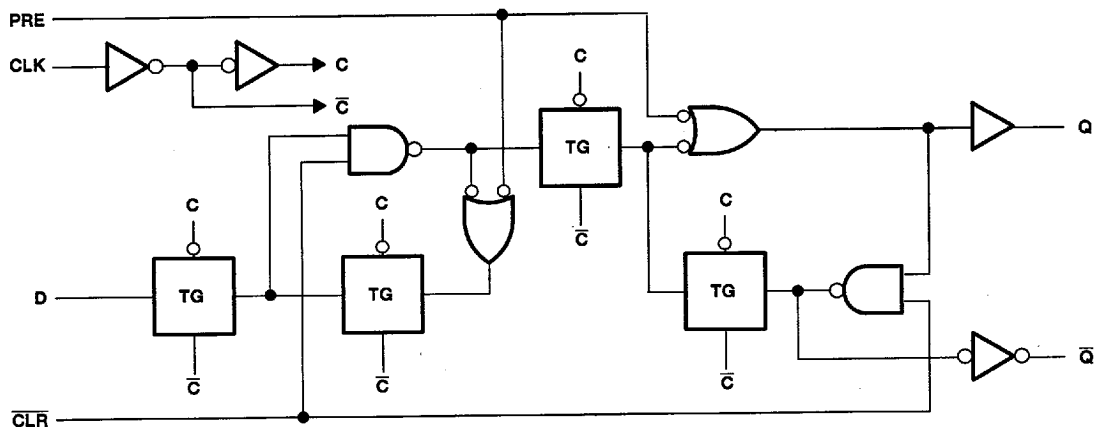
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			–6	mA
I_{OL}	Low-level output current			6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC} [†]	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2			V
	I _{OH} = -6 mA		3 V	2.4			
V _{OL}	I _{OL} = 100 μA		MIN to MAX			0.2	V
	I _{OL} = 6 mA		3 V			0.4	
I _I	V _I = V _{CC} or GND		3.6 V			±1	μA
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	3.6 V			20	μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND		One input at V _{CC} - 0.6 V,			500	μA
C _I	V _I = V _{CC} or GND		3.3 V	2.5			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	PRE or CLR low	20		25		ns
		CLK high or low	20		25		
t_{su}	Setup time before CLK↑	Data	13		16		ns
		PRE or CLR inactive	8		10		
t_h	Hold time, data after CLK↑		3		3		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	100		19		MHz
t_{pd}	PRE or CLR	Q or $\bar{Q}$	16	34		43		ns
	CLK		15	28		35		

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	32	pF

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