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1 Introduction

Motorola's DragonBall™ family of microprocessors has demonstrated leadership in the portable handheld market. Continuing this legacy, the DragonBall MX (Media Extensions) series offers a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. DragonBall MX products specifically address the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The new DragonBall MC9328MXL features the advanced and power-efficient ARM920T™ core that operates at speeds up to 200 MHz. Integrated modules, which include an LCD controller, USB support, and an MMC/SD host controller, support a suite of peripherals to enhance any product seeking to provide a rich multimedia experience. It is packaged in either a 256-pin Mold Array Process-Ball Grid Array (MAPBGA) or 225-pin PBGA package. Figure 1 shows the functional block diagram of the MC9328MXL.

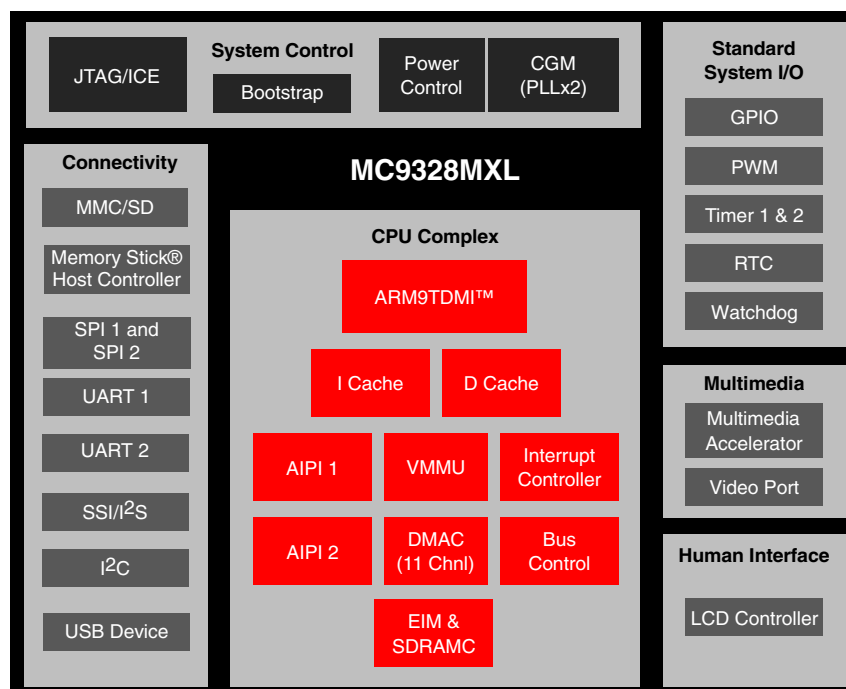


Figure 1. MC9328MXL Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
 - *Active low* signals change from logic level one to logic level zero.
 - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
 - *Active low* signals change from logic level zero to logic level one.
 - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign (\$) or 0x are hexadecimal.

1.2 Features

To support a wide variety of applications, the MC9328MXL offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Two Serial Peripheral Interfaces (SPI1 and SPI2)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)

- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and Inter-IC Sound (SSI/I²S) Module
- Inter-IC (I²C) Bus Module
- Video Port
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Multimedia Accelerator (MMA)
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.98 V core, 1.7 V to 3.3V I/O
- 256-pin MAPBGA Package
- 225-pin MAPBGA Package

1.3 Target Applications

The MC9328MXL is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers, and messaging applications.

1.4 Product Documentation

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous DragonBall products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP/D)

MC9328MXL Reference Manual (order number MC9328MXLRM/D)

The Motorola manuals are available on the Motorola Semiconductors Web site at <http://www.motorola.com/semiconductors>. These documents may be downloaded directly from the Motorola Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from <http://www.arm.com>.

1.5 Ordering Information

Table 1 provides ordering information for both the 256-lead mold array process ball grid array (MAPBGA) package and the 225-lead BGA package.

Table 1. MC9328MXL Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
256-lead MAPBGA	150 MHz	0°C to 70°C		MC9328MXLVH15
			Pb-free	MC9328MXLVM15
		-30°C to 70°C		MC9328MXLDVH15
			Pb-free	MC9328MXLDVM15
		-40°C to 85°C		MC9328MXLCVH15
			Pb-free	MC9328MXLCVM15
	200 MHz	0°C to 70°C		MC9328MXLVH20
			Pb-free	MC9328MXLVM20
-30°C to 70°C			MC9328MXLDVH20	
		Pb-free	MC9328MXLDVM20	
225-lead MAPBGA	150 MHz	0°C to 70°C		MC9328MXLVF15
			Pb-free	MC9328MXLVP15
		-30°C to 70°C		MC9328MXLDVF15
			Pb-free	MC9328MXLDVP15
		-40°C to 85°C		MC9328MXLCVF15
			Pb-free	MC9328MXLCVP15
	200 MHz	0°C to 70°C		MC9328MXLVF20
			Pb-free	MC9328MXLVP20
-30°C to 70°C			MC9328MXLDVF20	
		Pb-free	MC9328MXLDVP20	

2 Signals and Connections

Table 2 identifies and describes the MC9328MXL signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. MC9328MXL Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
\overline{OE}	Memory Output Enable—Active low output enables external data bus.
\overline{CS} [5:0]	Chip-Select—The chip-select signals \overline{CS} [3:2] are multiplexed with \overline{CSD} [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default \overline{CSD} [1:0] is selected.
\overline{ECB}	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
\overline{LBA}	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
\overline{RW}	\overline{RW} signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a \overline{WE} input signal by external DRAM.
\overline{DTACK}	\overline{DTACK} signal— The external input data acknowledge signal. When using the external \overline{DTACK} signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external \overline{DTACK} signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the MC9328MXL upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM/SyncFlash non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM/SyncFlash cycles.
SDIBA [3:0]	SDRAM/SyncFlash interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM/SyncFlash cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM/SyncFlash cycles.
DQM [3:0]	SDRAM data enable
$\overline{CSD0}$	SDRAM/SyncFlash Chip-select signal which is multiplexed with the $\overline{CS2}$ signal. These two signals are selectable by programming the system control register.
$\overline{CSD1}$	SDRAM/SyncFlash Chip-select signal which is multiplexed with $\overline{CS3}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{CSD1}$ is selected, so it can be used as SyncFlash boot chip-select by properly configuring BOOT [3:0] input pins.
\overline{RAS}	SDRAM/SyncFlash Row Address Select signal

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{CAS}}$	SDRAM/SyncFlash Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM/SyncFlash Write Enable signal
SDCKE0	SDRAM/SyncFlash Clock Enable 0
SDCKE1	SDRAM/SyncFlash Clock Enable 1
SDCLK	SDRAM/SyncFlash Clock
$\overline{\text{RESET_SF}}$	SyncFlash Reset
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to little endian. If it is driven logic-low at reset, the external chip-select space will be configured to big endian.
$\overline{\text{DMA_REQ}}$	External DMA request pin.

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with \overline{ECB} , \overline{LBA} , BCLK, PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SPI 1 and 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_ \overline{SS}	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_ $\overline{SPI_RDY}$	Serial Data Ready

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MXL Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MXL Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_SS	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MXL Reference Manual for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the MC9328MXL Reference Manual for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
USBD_OE	USB OE
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
UART1_RTS	Request to Send
UART1_CTS	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
UART2_RTS	Request to Send
UART2_CTS	Clear to Send
UART2_DSR	Data Set Ready
UART2_RI	Ring Indicator
UART2_DCD	Data Carrier Detect
UART2_DTR	Data Terminal Ready
Serial Audio Port – SSI (configurable to I²S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I²C	
I2C_SCL	I ² C Clock
I2C_SDA	I ² C Data
PWM	
PWMO	PWM Output
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins

Table 2. MC9328MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
AVSS	Quiet ground for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry
Substrate Supply Pins	
SVDD	Supply routed through substrate of package; not to be bonded
SGND	Ground routed through substrate of package; not to be bonded

3 Specifications

This section contains the electrical specifications and timing diagrams for the MC9328MXL processor.

3.1 Maximum Ratings

Table 3 provides information on maximum ratings.

Table 3. Maximum Ratings

Rating	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{dd}	-0.3	3.3	V
Maximum operating temperature range	T_A	0	70	°C
Storage temperature	Test	-55	150	°C
Power Consumption	P_{max}	800 ¹	1300 ²	mW

1. A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core—that is, 7x GPIO, 15x Data bus, and 8x Address bus.
2. A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core—that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 200MHz, and where the whole image is running out of SDRAM. QVDD at 2.0V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges for the supply voltages. The MC9328MXL has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 4. Recommended Operating Range

Rating	Symbol	Minimum	Maximum	Unit
I/O supply voltage (if using MSHC, SPI, BTA, USBd, LCD and CSI which are only 3 V interfaces)	NVDD	2.70	3.30	V
I/O supply voltage (if not using the peripherals listed above)	NVDD	1.70	3.30	V
Internal supply voltage (Core = 150 MHz)	QVDD	1.70	1.90	V
Internal supply voltage (Core = 200 MHz)	QVDD	1.80	2.00	V
Analog supply voltage	AVDD	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains both maximum and minimum DC characteristics of the MC9328MXL.

Table 5. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Minimum	Typical	Maximum	Unit
I _{op}	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	—	QVDD at 1.8v = 120mA; NVDD+AVDD at 3.0v = 30mA	—	mA
Sidd ₁	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	—	25	—	μA
Sidd ₂	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	—	45	—	μA
Sidd ₃	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	—	35	—	μA
Sidd ₄	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 55°C)	—	60	—	μA
V _{IH}	Input high voltage	0.7V _{DD}	—	V _{dd} +0.2	V
V _{IL}	Input low voltage	—	—	0.4	V

Table 5. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OH}	Output high voltage ($I_{OH} = 2.0\text{ mA}$)	$0.7V_{DD}$	—	V_{DD}	V
V_{OL}	Output low voltage ($I_{OL} = -2.5\text{ mA}$)	—	—	0.4	V
V_{it+}	Positive input threshold voltage, $V_i = V_{ih}$	—	—	1.126	V
V_{it-}	Negative input threshold voltage, $V_i = V_{il}$	0.640	—	—	V
V_{hys}	Hysteresis ($V_{it+} - V_{it-} = V_{ih}$)	—	0.3	—	V
I_{IL}	Input low leakage current ($V_{IN} = \text{GND}$, no pull-up or pull-down)	—	—	± 1	μA
I_{IH}	Input high leakage current ($V_{IN} = V_{DD}$, no pull-up or pull-down)	—	—	± 1	μA
I_{OH}	Output high current ($V_{OH} = 0.8V_{DD}$, $V_{DD} = 1.8\text{V}$)	—	—	4.0	mA
I_{OL}	Output low current ($V_{OL} = 0.4\text{V}$, $V_{DD} = 1.8\text{V}$)	-4.0	—	—	mA
I_{OZ}	Output leakage current ($V_{out} = V_{DD}$, output is tri-stated)	—	—	± 5	μA
C_i	Input capacitance	—	—	5	pF
C_o	Output capacitance	—	—	5	pF

3.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\text{ min}}$ to $V_{DD\text{ max}}$ under an operating temperature from T_L to T_H . All timing is measured at 30 pF loading.

Table 6. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	—	20.8	ns

Table 7. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter(peak to peak)	—	5	20	ns
EXTAL32k startup time	800	—	—	ms

Table 7. 32k/16M Oscillator Signal Timing (Continued)

Parameter	Minimum	RMS	Maximum	Unit
EXTAL16M input jitter(peak to peak)	—	TBD	TBD	—
EXTAL16M startup time	TBD	—	—	—

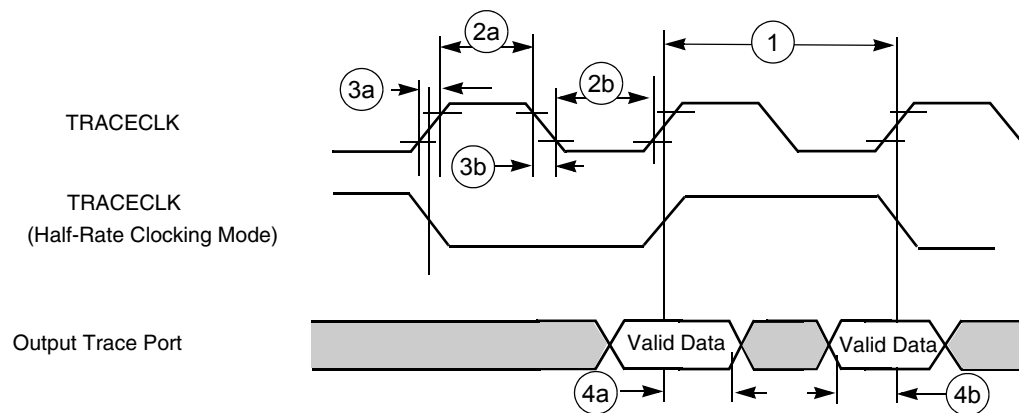
3.5 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 8 on page 13 for the ETM9 timing parameters used in Figure 2.

**Figure 2. Trace Port Timing Diagram****Table 8. Trace Port Timing Diagram Parameter Table**

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	—	2	—	ns
2b	Clock low time	3	—	2	—	ns
3a	Clock rise time	—	4	—	3	ns

Table 8. Trace Port Timing Diagram Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
3b	Clock fall time	—	3	—	3	ns
4a	Output hold time	2.28	—	2	—	ns
4b	Output setup time	3.42	—	3	—	ns

3.6 DPLL Timing Specifications

Parameters of the DPLL are given in Table 9. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 9. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock freq range	Vcc = 1.8V	5	—	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	—	30	MHz
Double clock freq range	Vcc = 1.8V	80	—	220	MHz
Pre-divider factor (PD)	—	1	—	16	—
Total multiplication factor (MF)	Includes both integer and fractional parts	5	—	15	—
MF integer part	—	5	—	15	—
MF numerator	Should be less than the denominator	0	—	1022	—
MF denominator	—	1	—	1023	—
Pre-multiplier lock-in time	—	—	—	312.5	μsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 μs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 μs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 μs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 μs)	370	T_{ref}
Freq jitter (p-p)	—	—	0.005 (0.01%)	0.01	$2 \cdot T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.8V	—	1.0 (10%)	1.5	ns
Power supply voltage	—	1.7	—	2.5	V
Power dissipation	FOL mode, integer MF, $f_{dck} = 200$ MHz, Vcc = 1.8V	—	—	4	mW

3.7 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4. Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

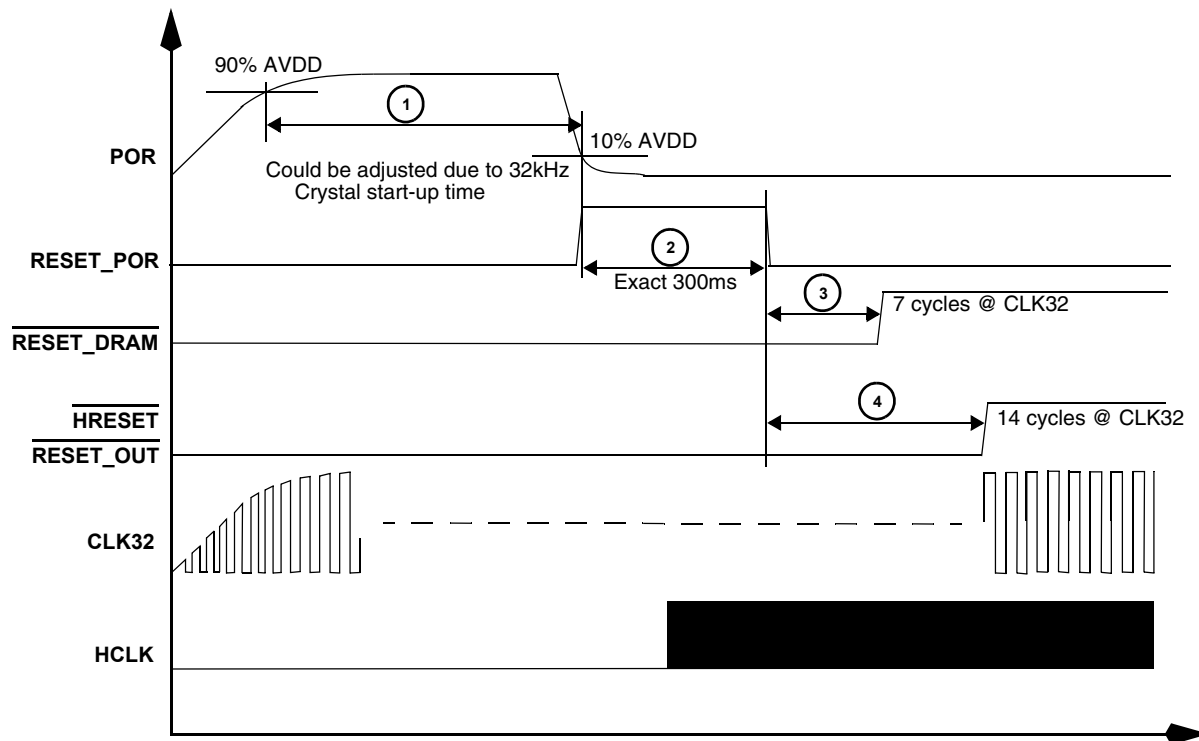


Figure 3. Timing Relationship with POR

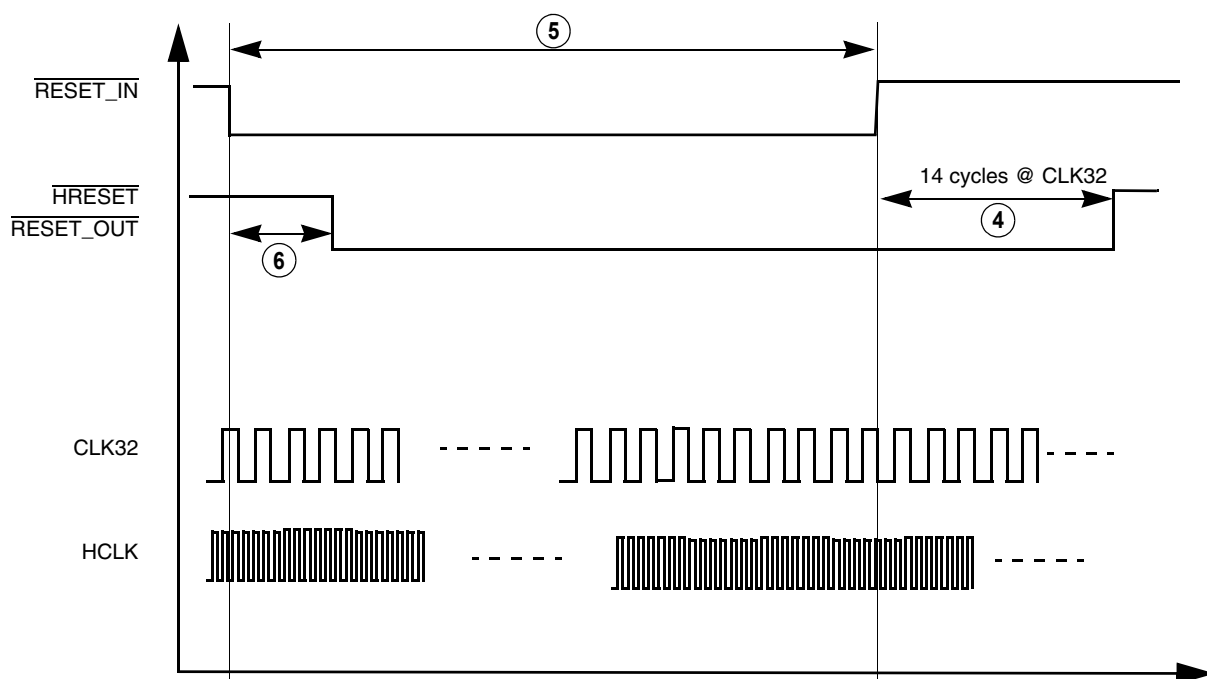
Figure 4. Timing Relationship with $\overline{\text{RESET_IN}}$

Table 10. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	800	—	800	—	ms
2	Width of internal $\overline{\text{POWER_ON_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESET}}$ and output reset at pin $\overline{\text{RESET_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET_IN}}$	4	—	4	—	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

3.8 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the MC9328MXL, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 11 on page 19 defines the parameters of signals.

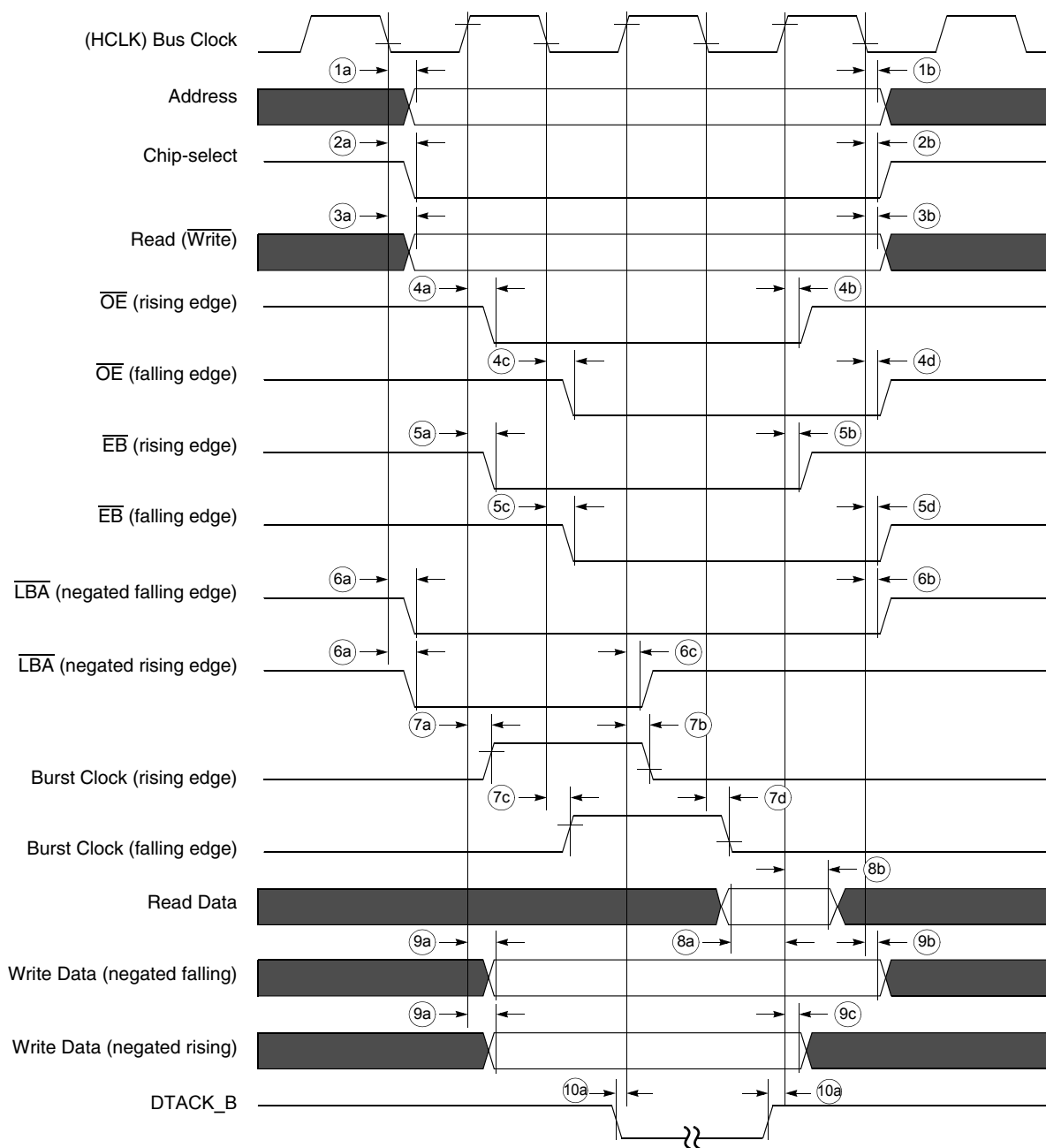


Figure 5. EIM Bus Timing Diagram

Table 11. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V			3.0V \pm 0.30V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read ($\overline{\text{Write}}$) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read ($\overline{\text{Write}}$) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns
4a	Clock ¹ rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock ¹ rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock ¹ fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock ¹ fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock ¹ rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock ¹ rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock ¹ fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock ¹ fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock ¹ fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock ¹ fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock ¹ rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock ¹ rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock ¹ rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock ¹ fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock ¹ fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	—	—	5.5	—	—	ns
8b	Read Data hold time	0	—	—	0	—	—	ns
9a	Clock ¹ rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock ¹ fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock ¹ rise to Write Data Invalid	1.63	—	—	1.62	—	—	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	—	—	2.5	—	—	ns

1. Clock refers to the system clock signal, HCLK, generated from the System PLL

3.8.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only CS5 group is designed to support DTACK signal function when using the external DTACK signal for data acknowledgement.

3.8.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 shows the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in Table 12.

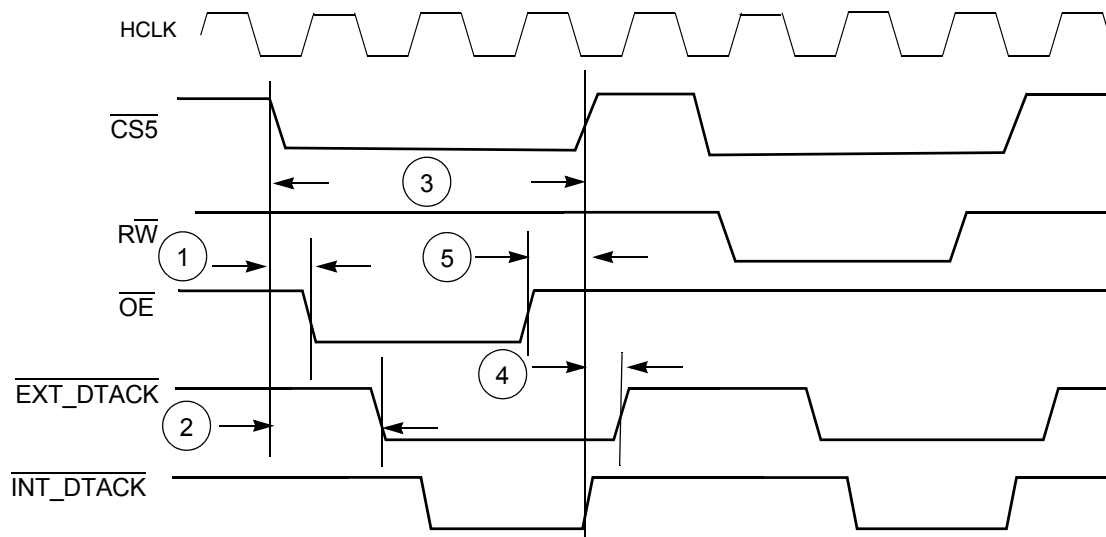


Figure 6. $\overline{\text{DTACK}}$ Timing, WSC=111111, $\text{DTACK_sel}=0$

Table 12. Access Cycle Timing Parameters

Ref No.	Characteristic	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Min	Max	Min	Max	
1	$\overline{\text{CS5}}$ asserted to $\overline{\text{OE}}$ asserted	—	T	—	T	ns
2	External $\overline{\text{DTACK}}$ input setup from $\overline{\text{CS5}}$ asserted	0	—	0	—	ns
3	$\overline{\text{CS5}}$ pulse width	3T	—	3T	—	ns
4	External $\overline{\text{DTACK}}$ input hold after $\overline{\text{CS5}}$ is negated	0	1.5T	0	1.5T	ns
5	$\overline{\text{OE}}$ negated after $\overline{\text{CS5}}$ is negated	0	4.5	0	4	ns
Note: <ol style="list-style-type: none"> 1. n is the number of wait states in the current memory access cycle. The max n is 1022. 2. T is the system clock period (system clock is 96 MHz). 3. The external $\overline{\text{DTACK}}$ input requirement is eliminated when $\overline{\text{CS5}}$ is programmed to use internal wait state. 						

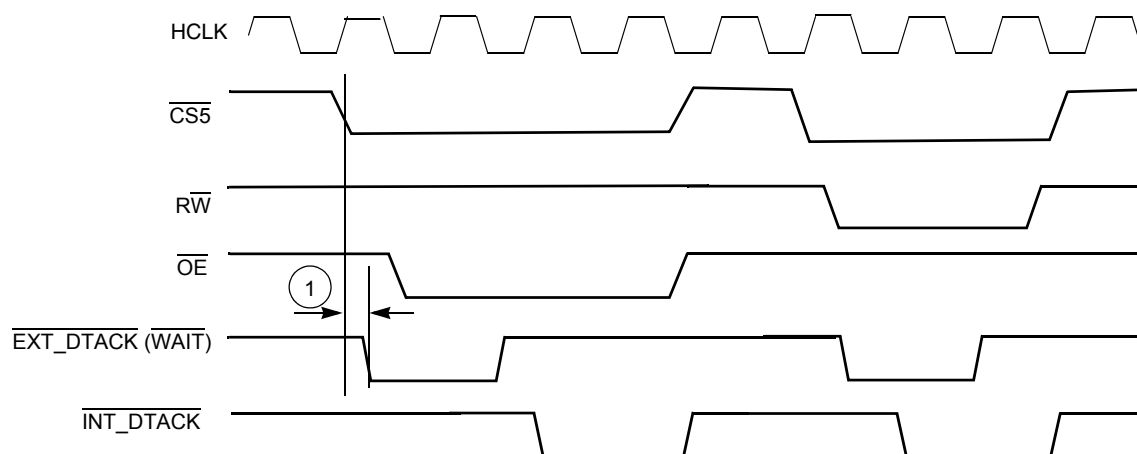


Figure 7. DTACK Timing, WSC=111111, DTACK_sel=1

Table 13. Access Cycle Timing Parameters

Ref No.	Characteristic	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Min	Max	Min	Max	
1	External $\overline{\text{DTACK}}$ input setup from $\overline{\text{CS5}}$ asserted	0	—	0	—	ns
Note: 1. n is the number of wait states in the current memory access cycle. The max n is 1022. 2. T is the system clock period (system clock is 96 MHz). 3. The external $\overline{\text{DTACK}}$ input requirement is eliminated when $\overline{\text{CS5}}$ is programmed to use internal wait state.						

3.8.3 EIM External Bus Timing

The timing diagrams in this section show the timing of accesses to memory or a peripheral.

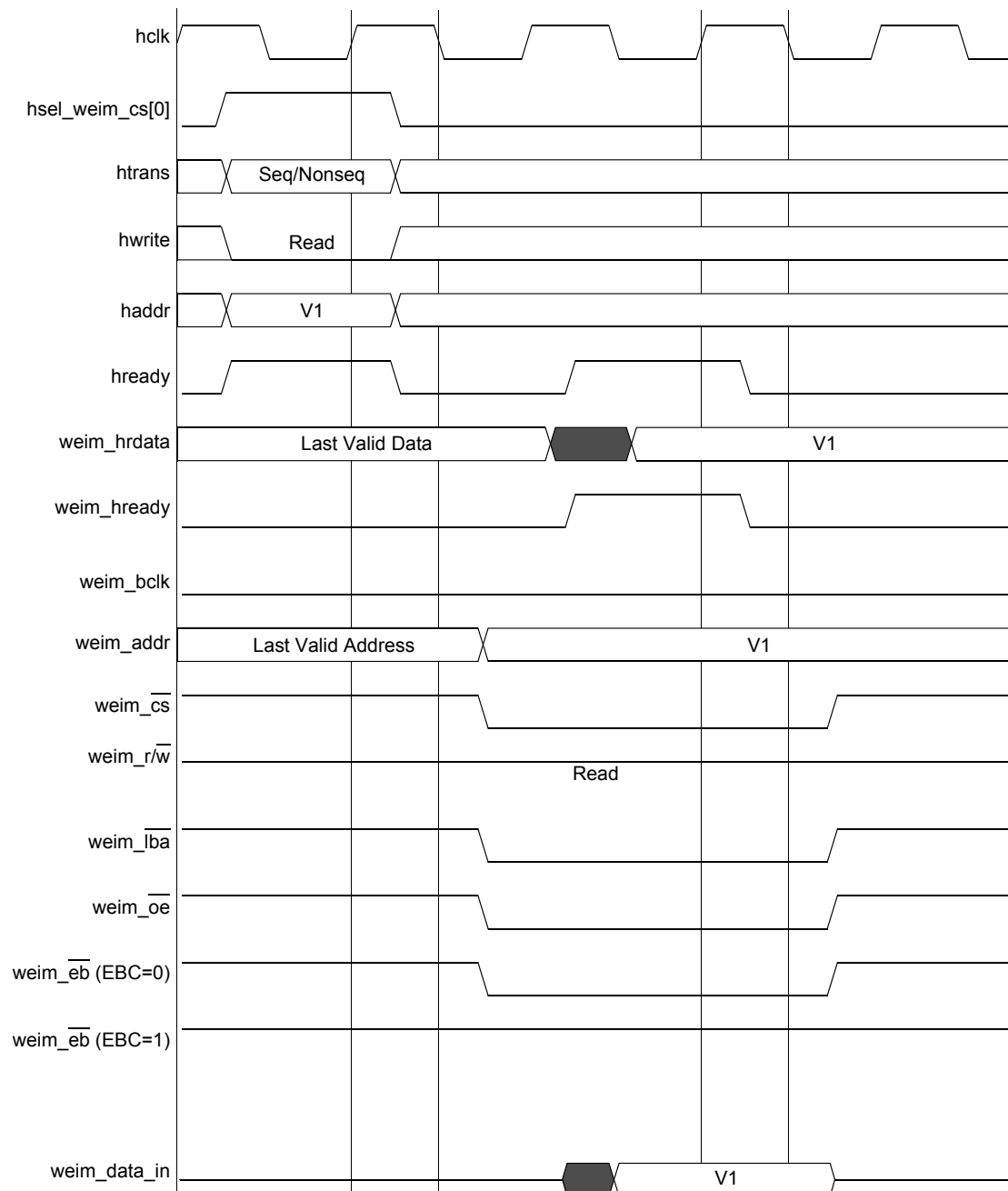


Figure 8. WSC = 1, A.HALF/E.HALF

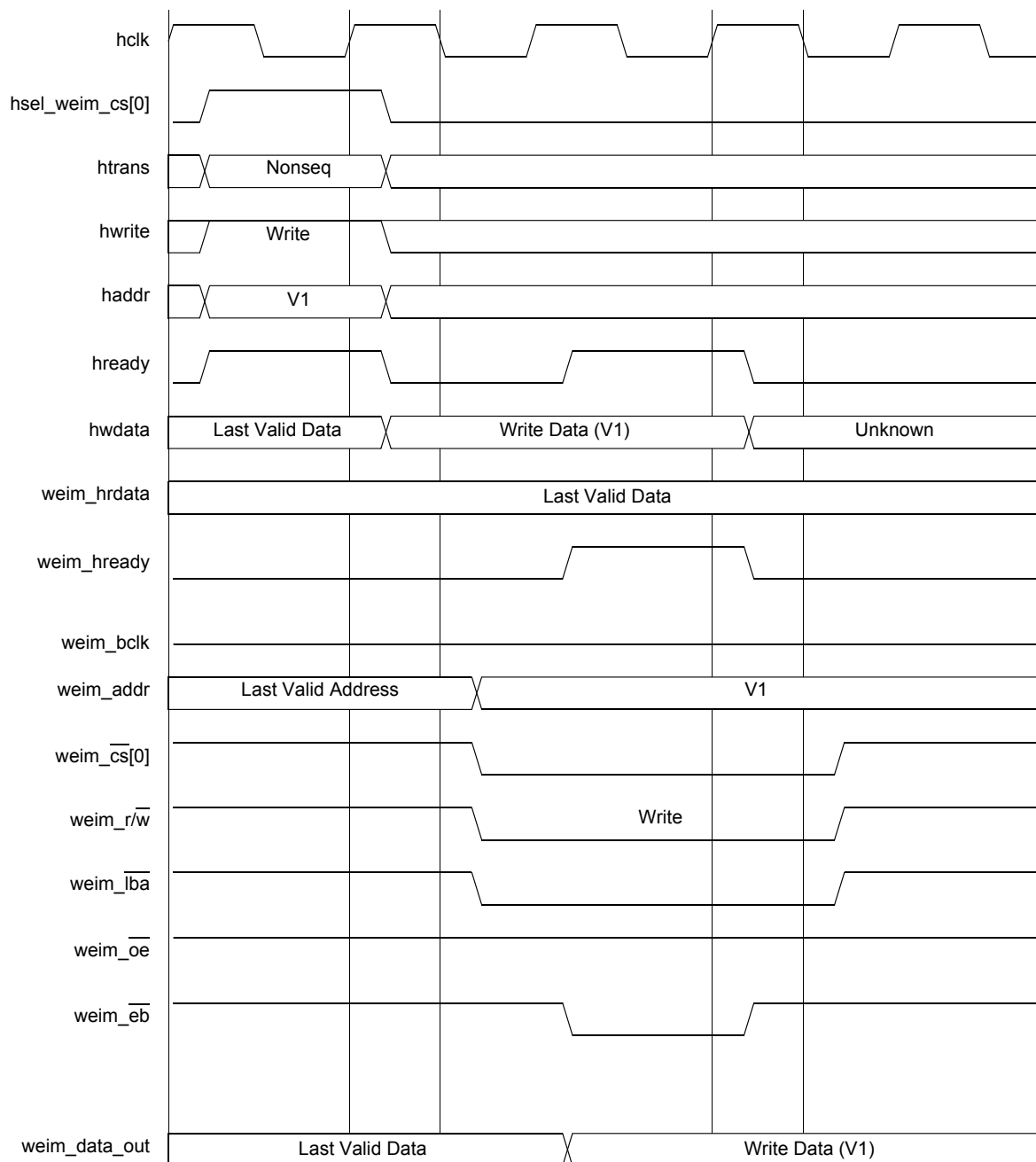


Figure 9. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Specifications

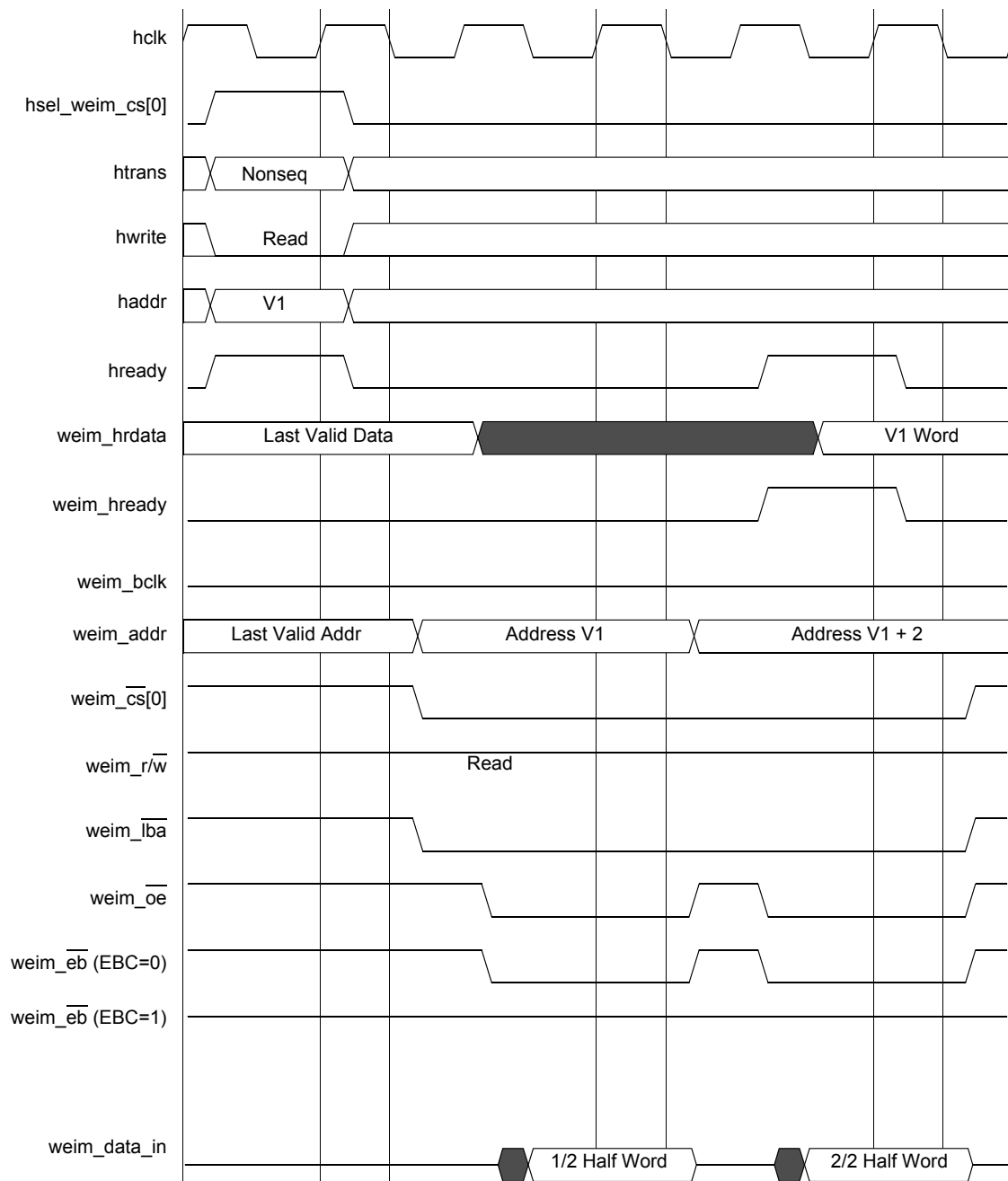


Figure 10. WSC = 1, OEA = 1, A.WORD/E.HALF

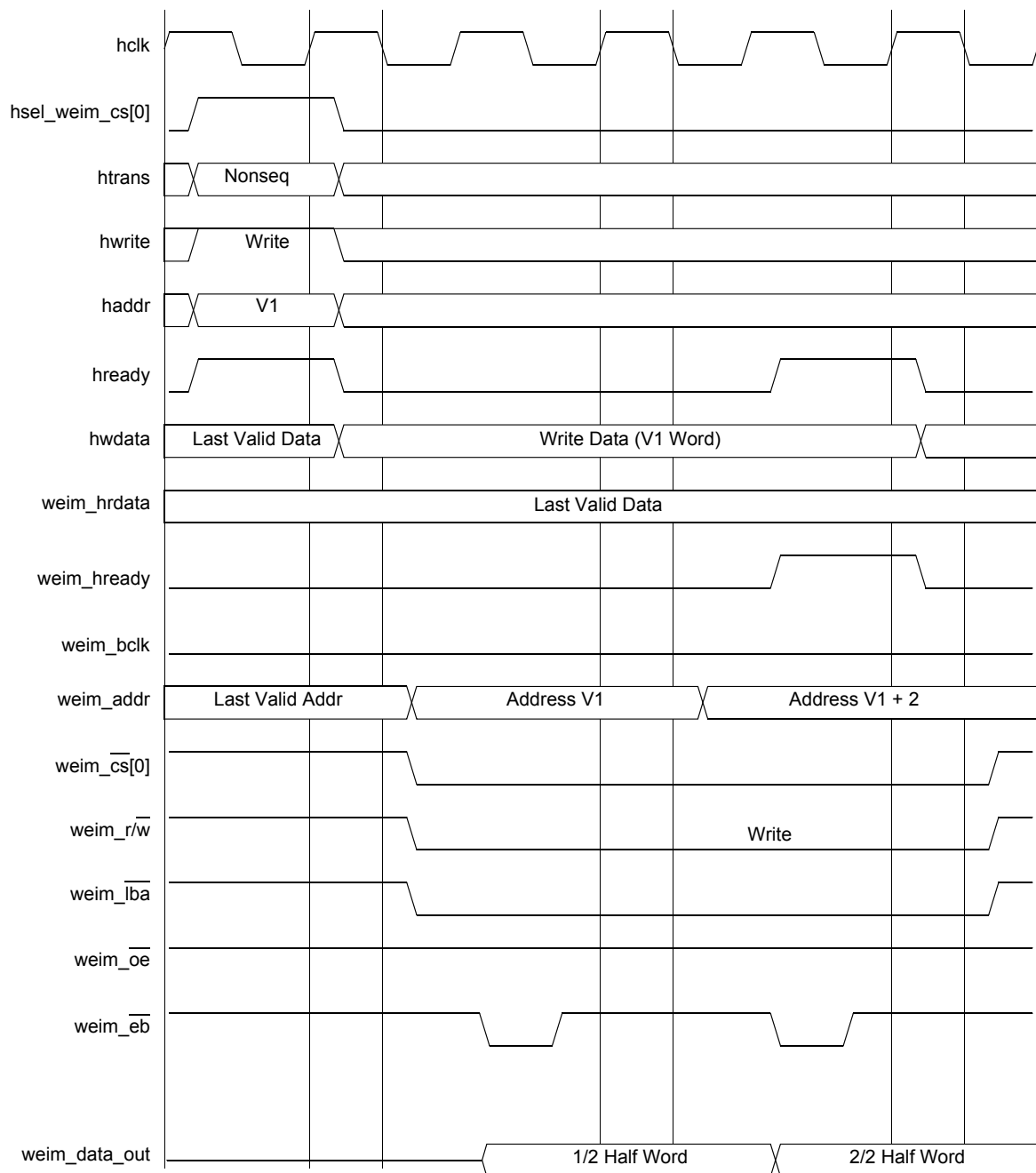


Figure 11. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

Specifications

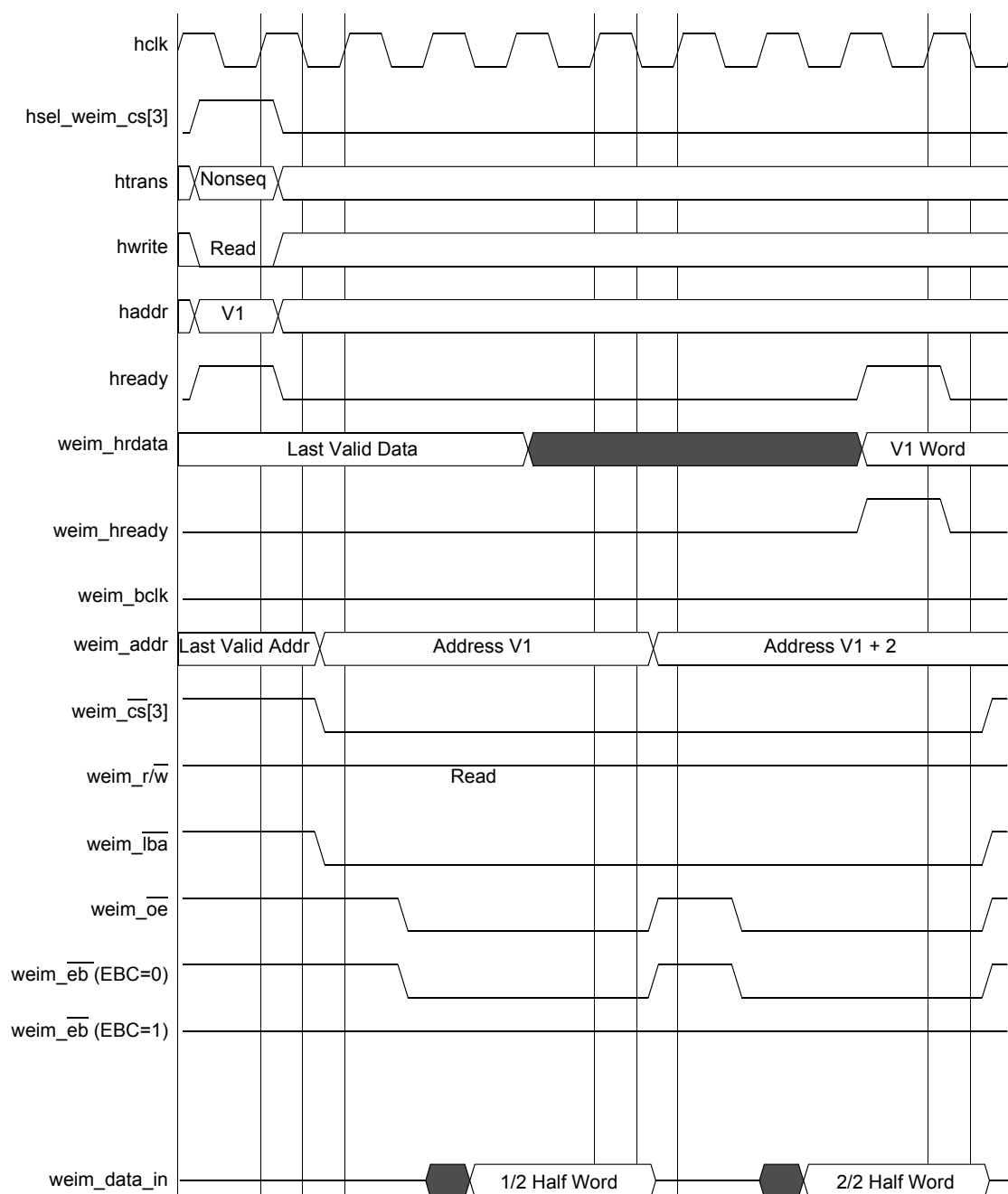


Figure 12. WSC = 3, OEA = 2, A.WORD/E.HALF

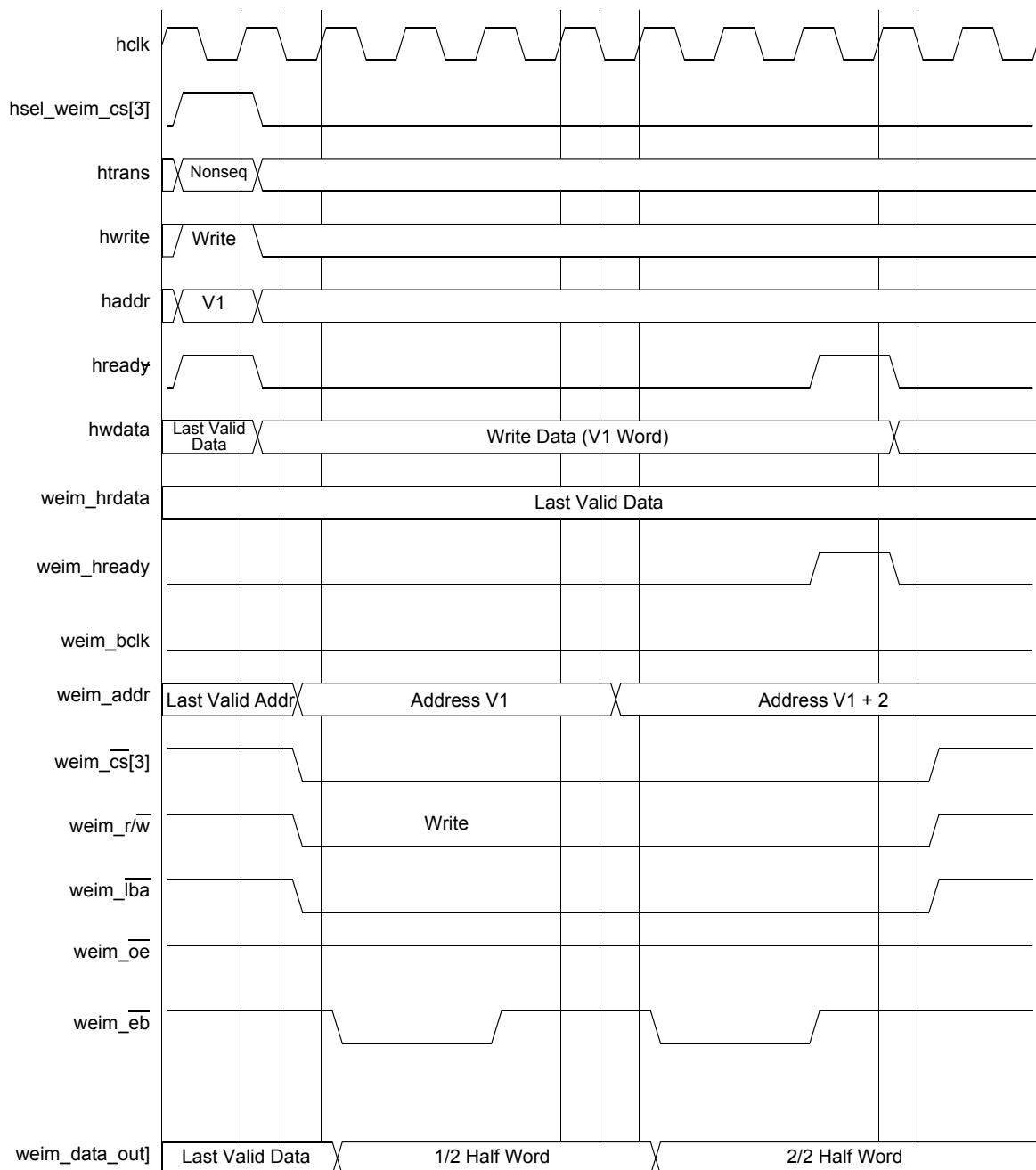


Figure 13. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF

Specifications

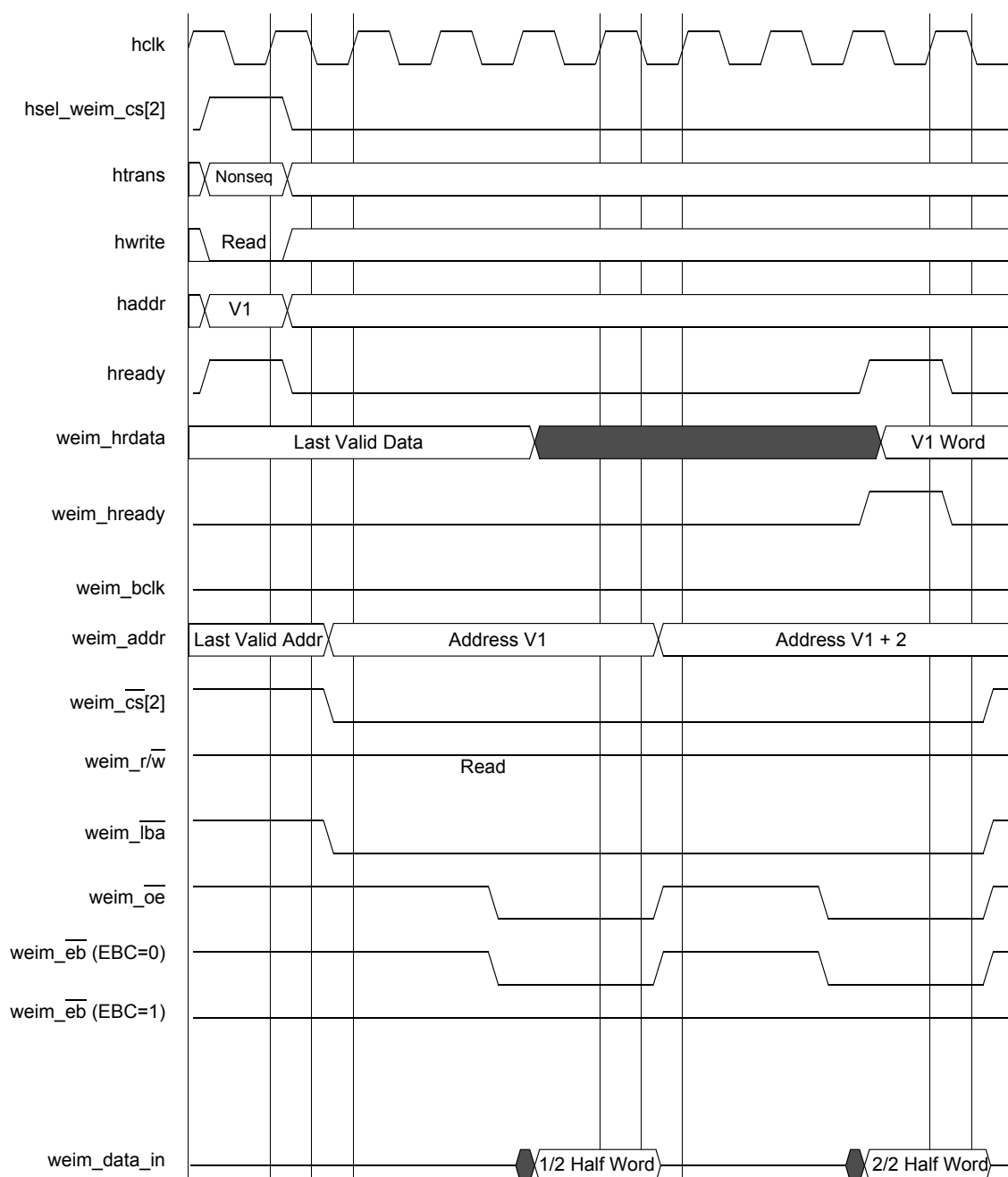


Figure 14. WSC = 3, OEA = 4, A.WORD/E.HALF

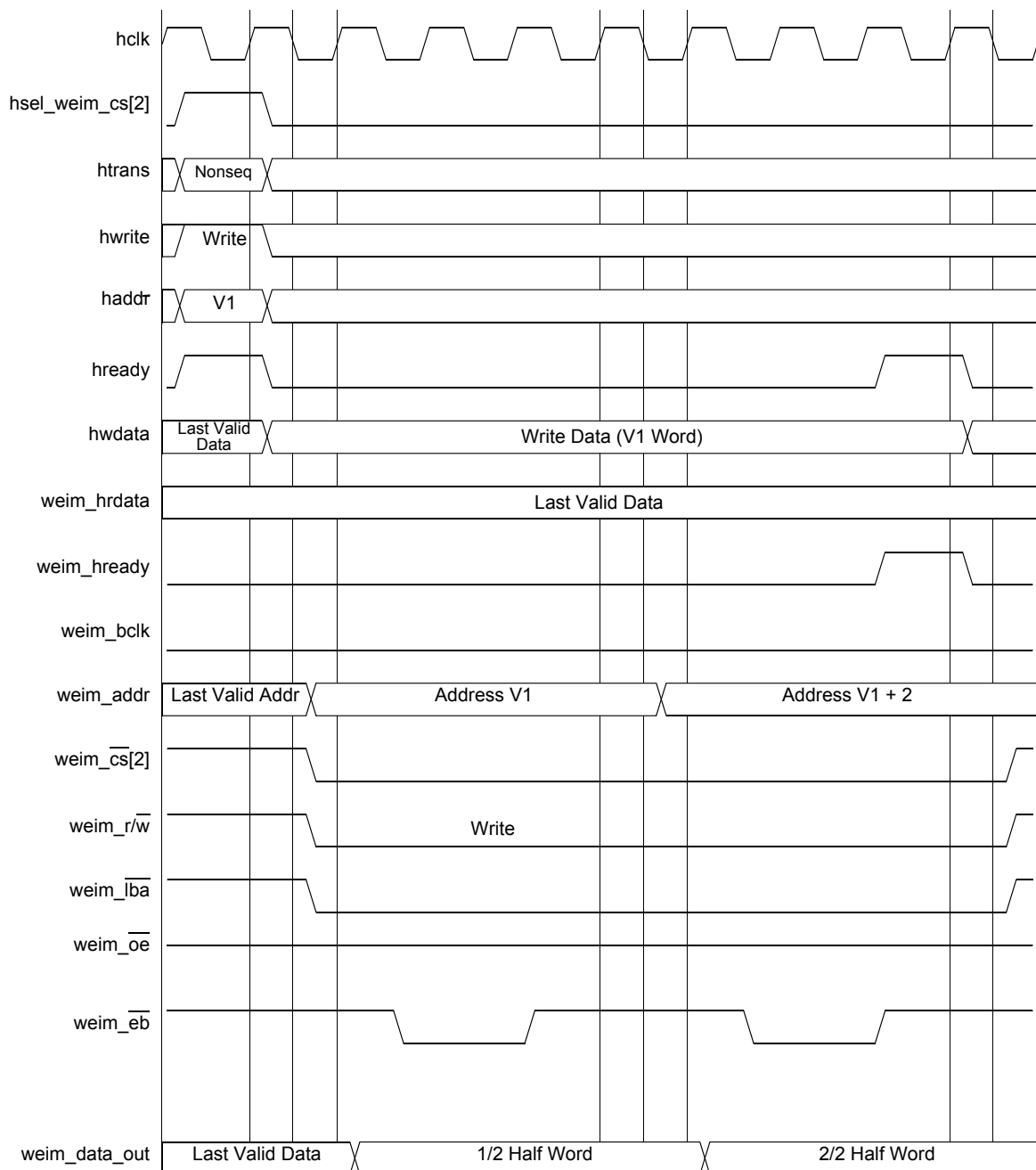


Figure 15. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF

Specifications

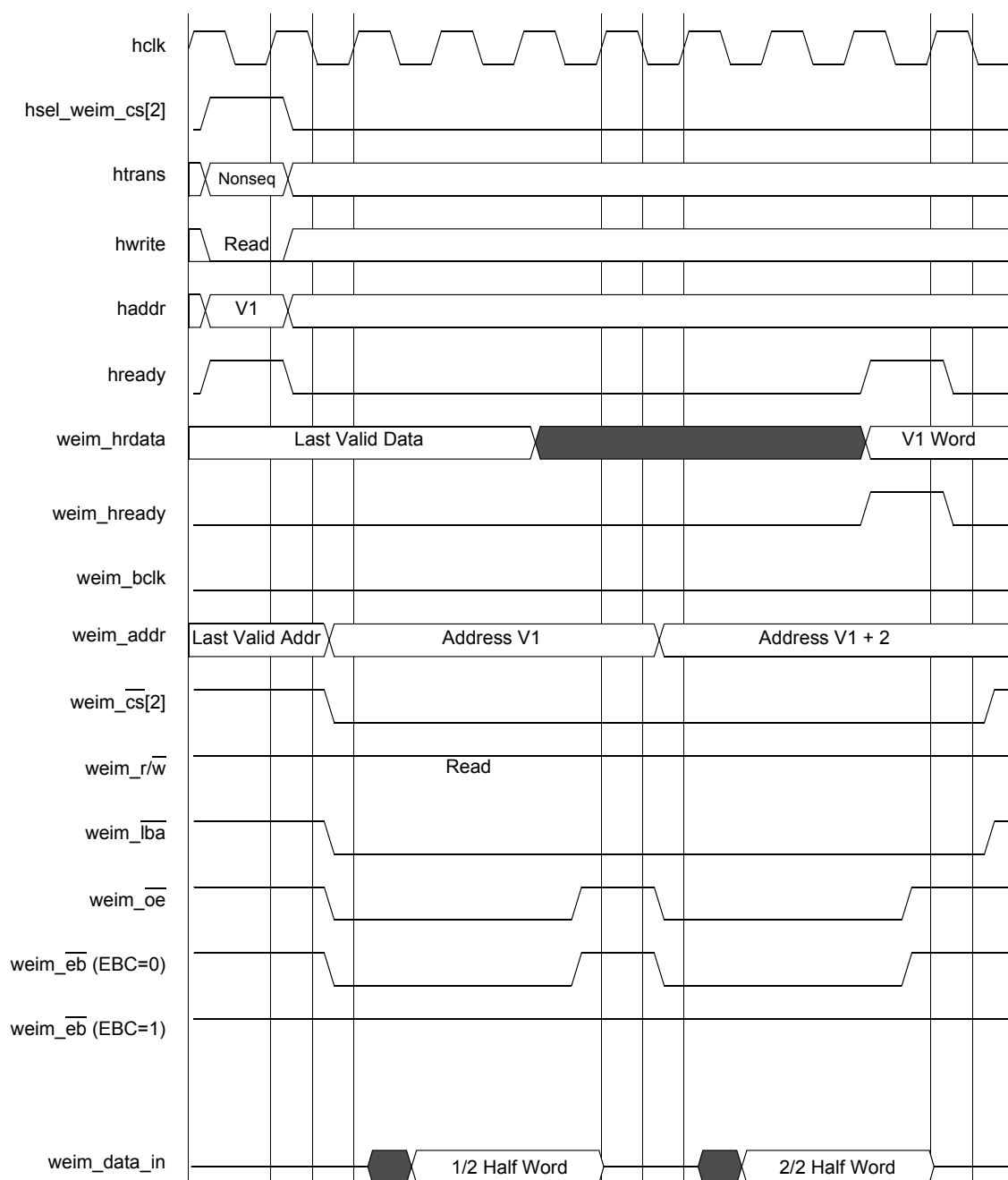


Figure 16. WSC = 3, OEN = 2, A.WORD/E.HALF

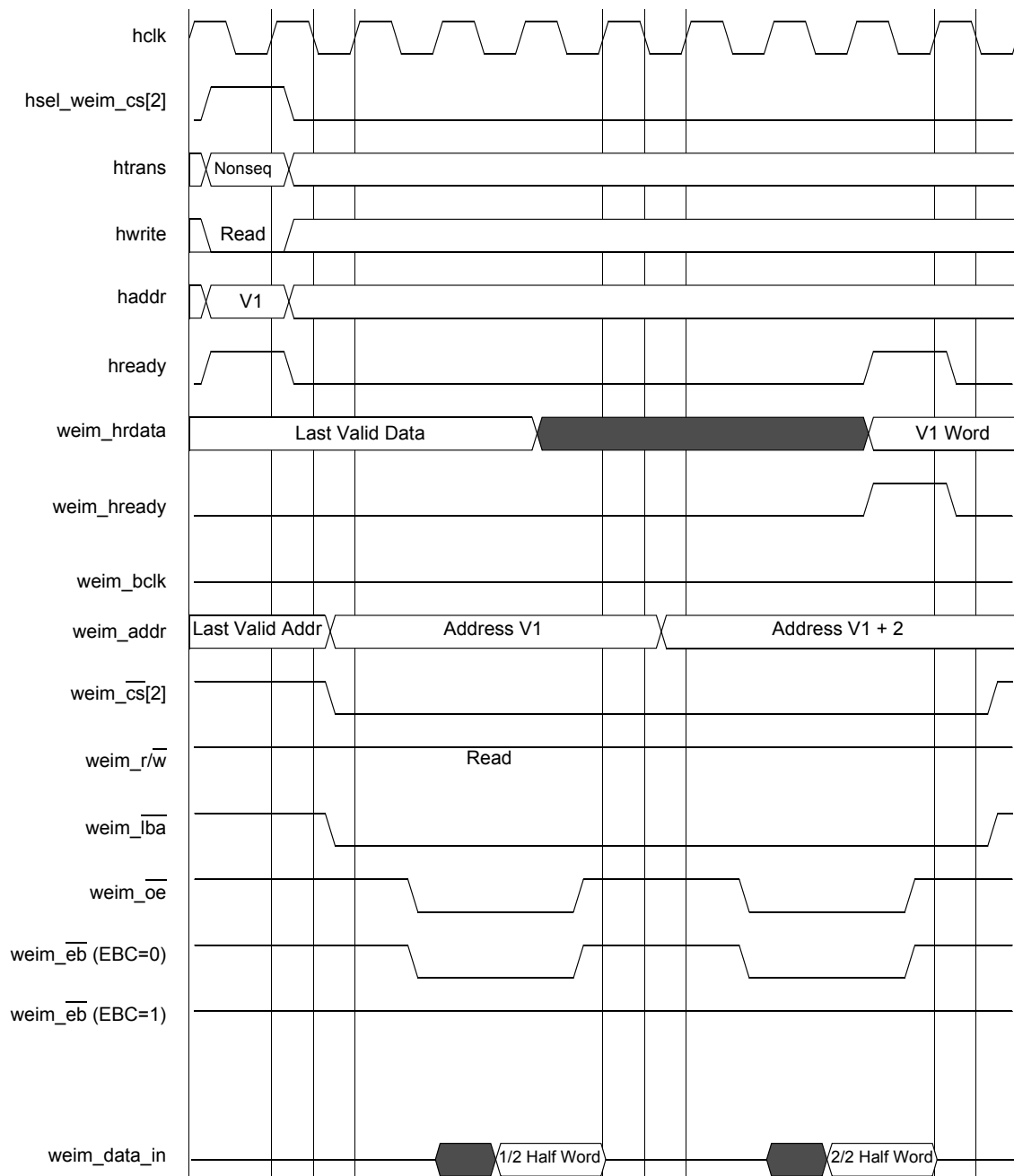


Figure 17. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

Specifications

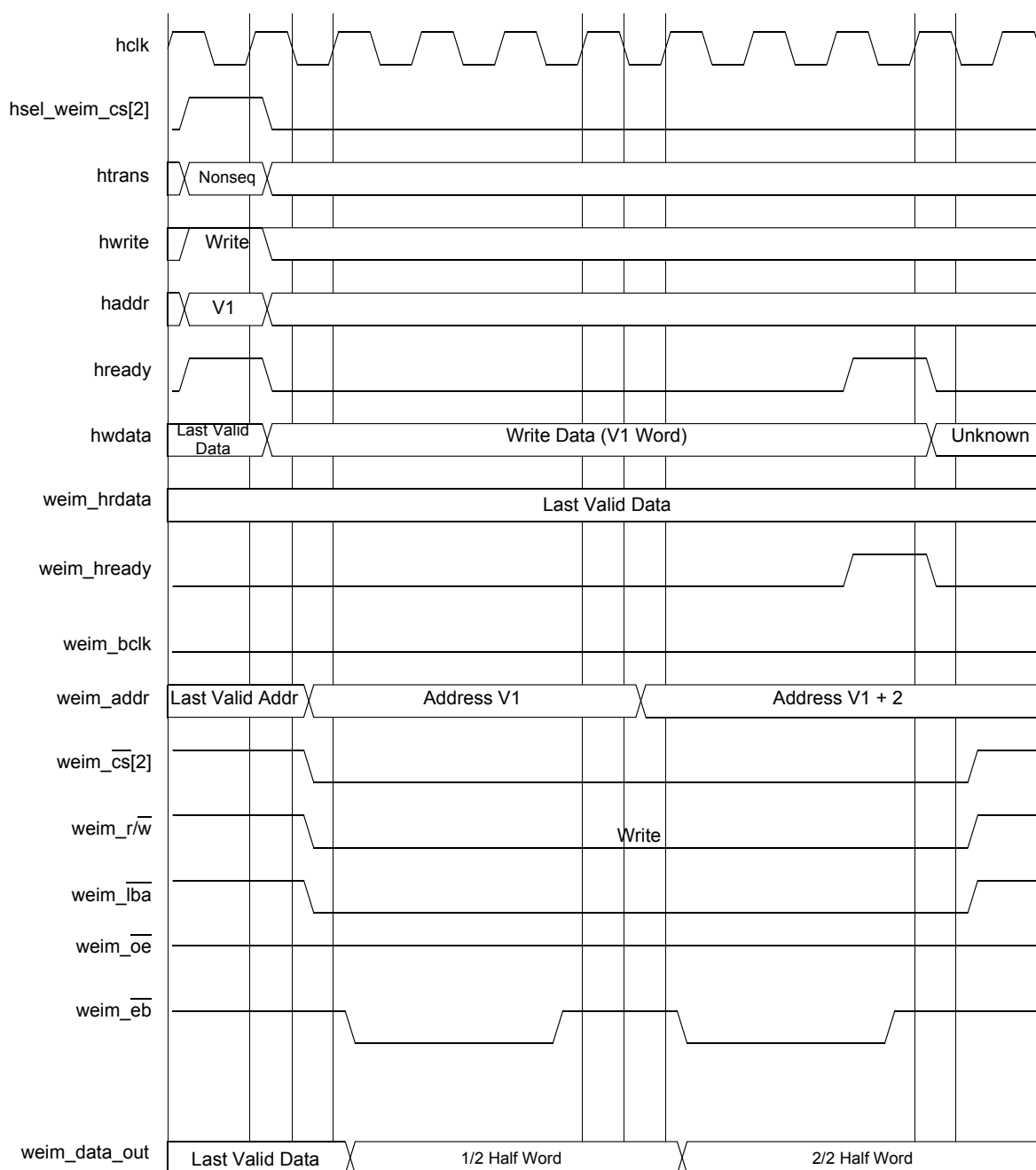


Figure 18. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

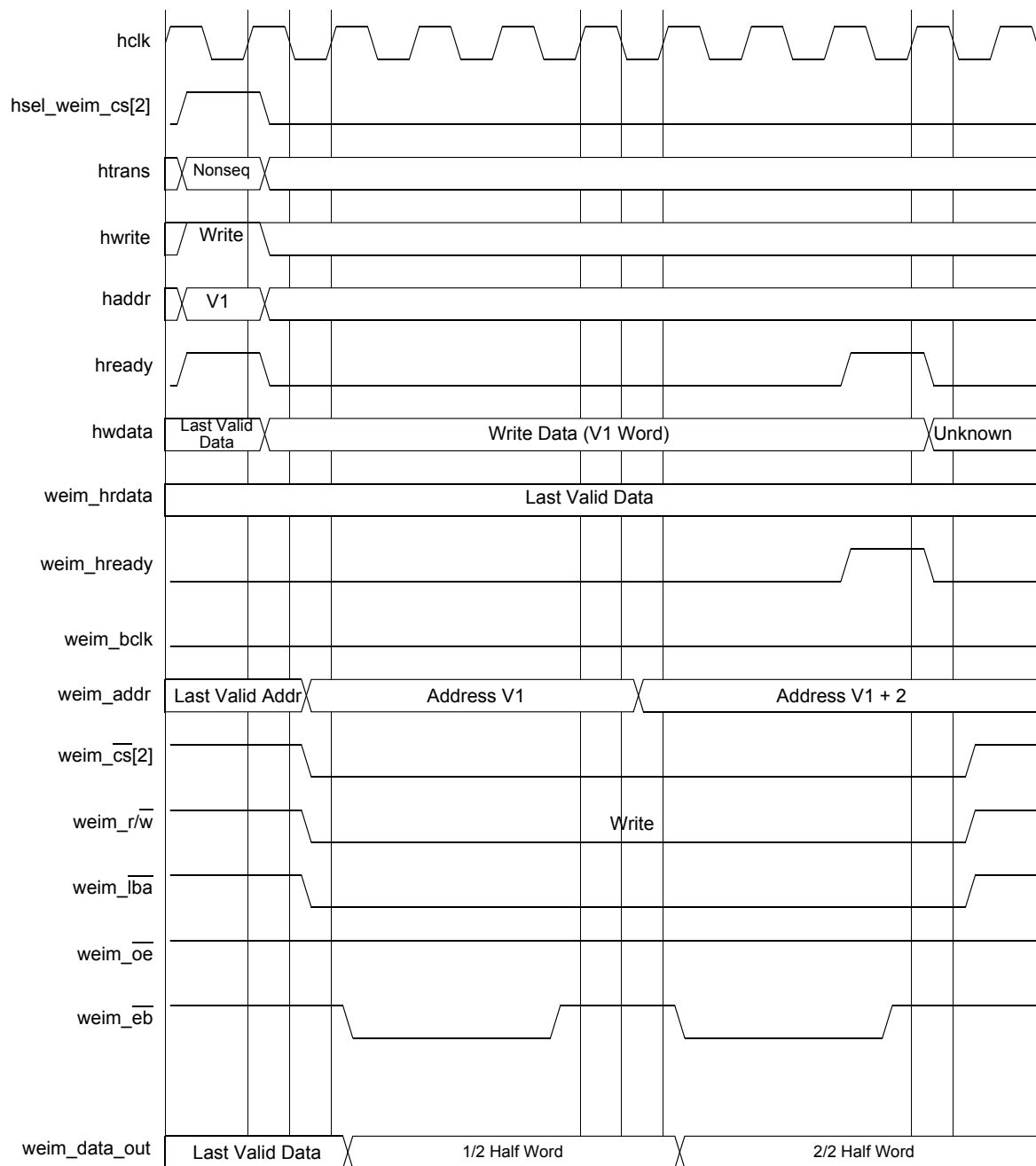


Figure 19. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

Specifications

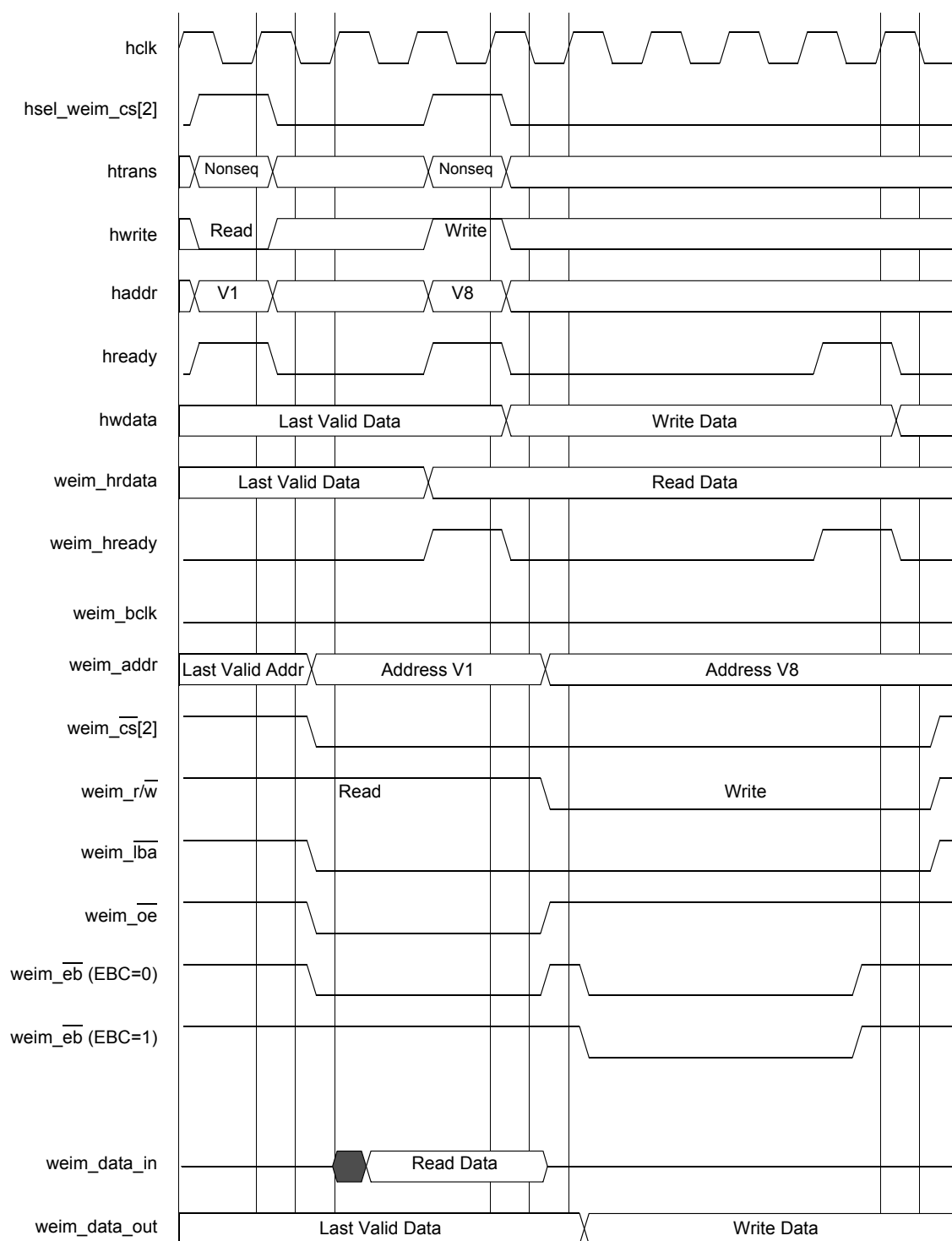


Figure 20. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

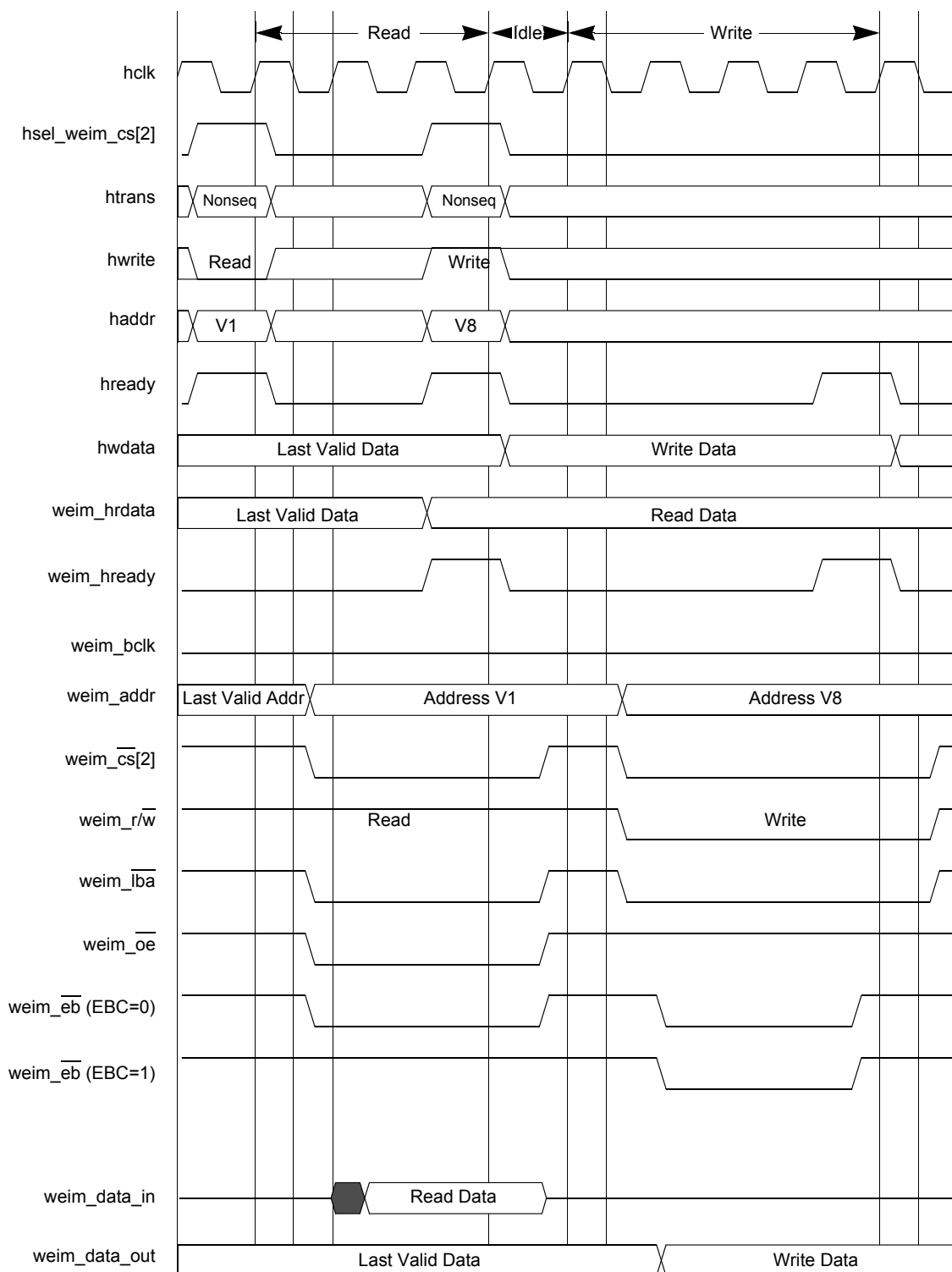


Figure 21. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF

Specifications

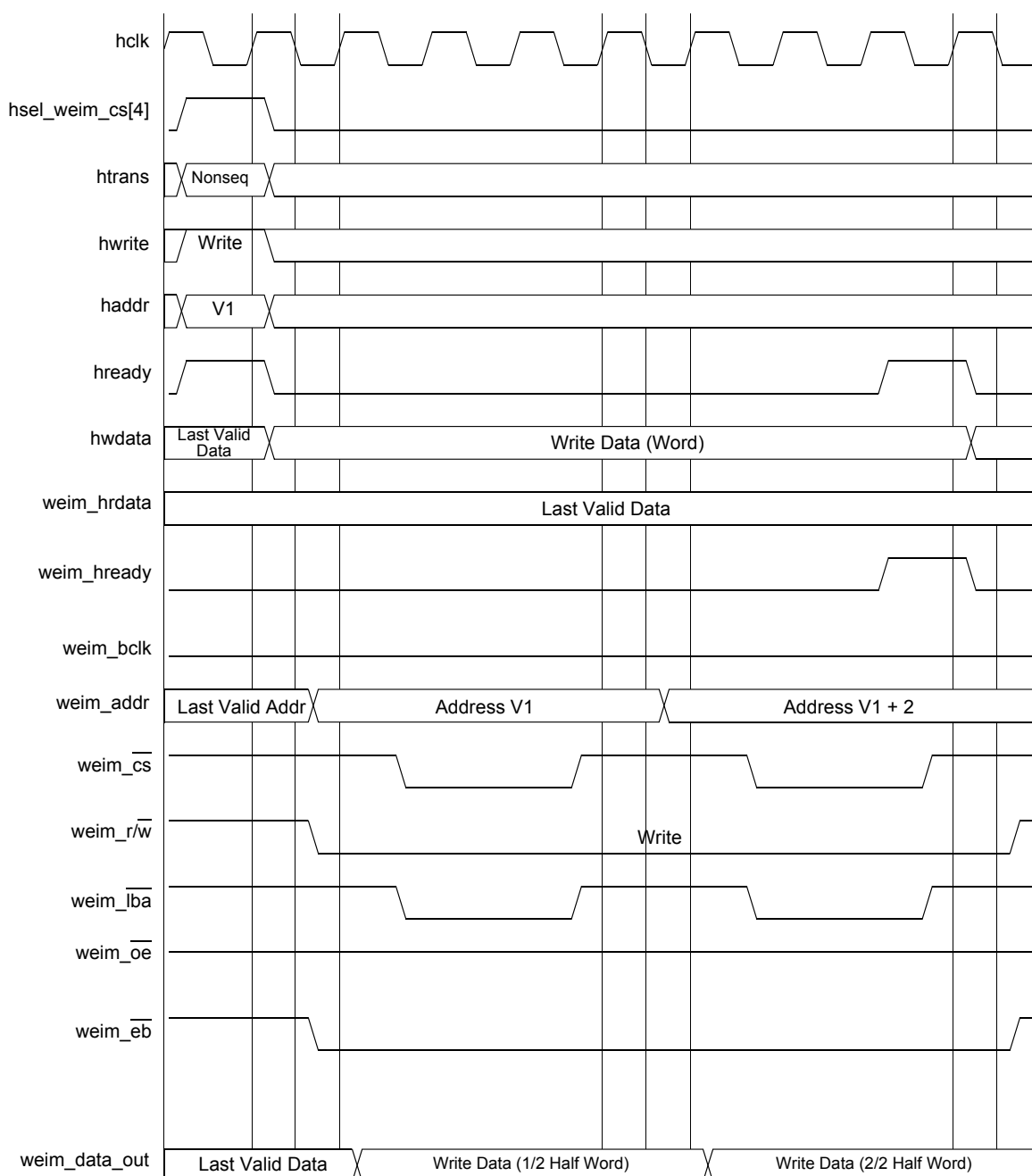


Figure 22. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF

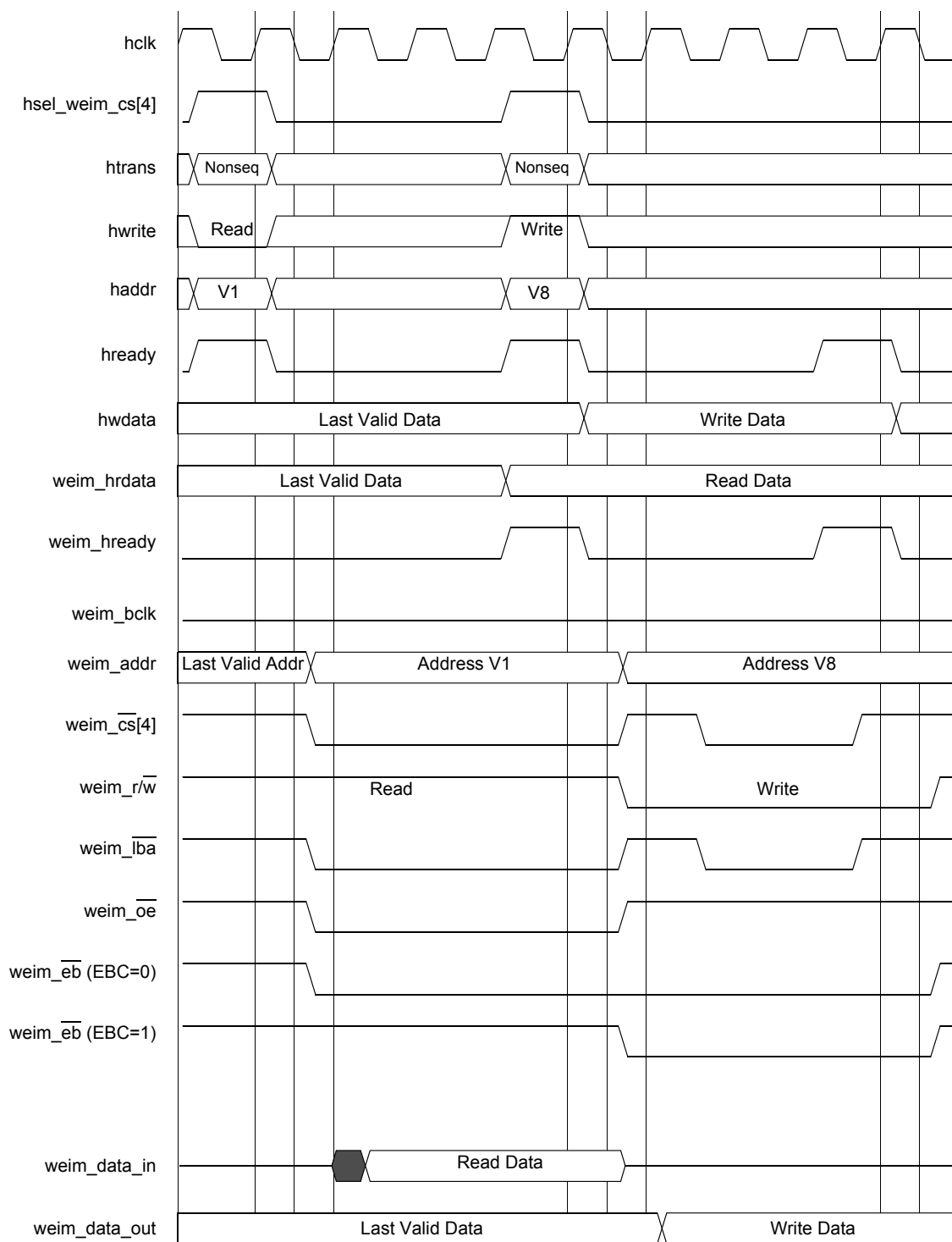


Figure 23. WSC = 3, CSA = 1, A.HALF/E.HALF

Specifications

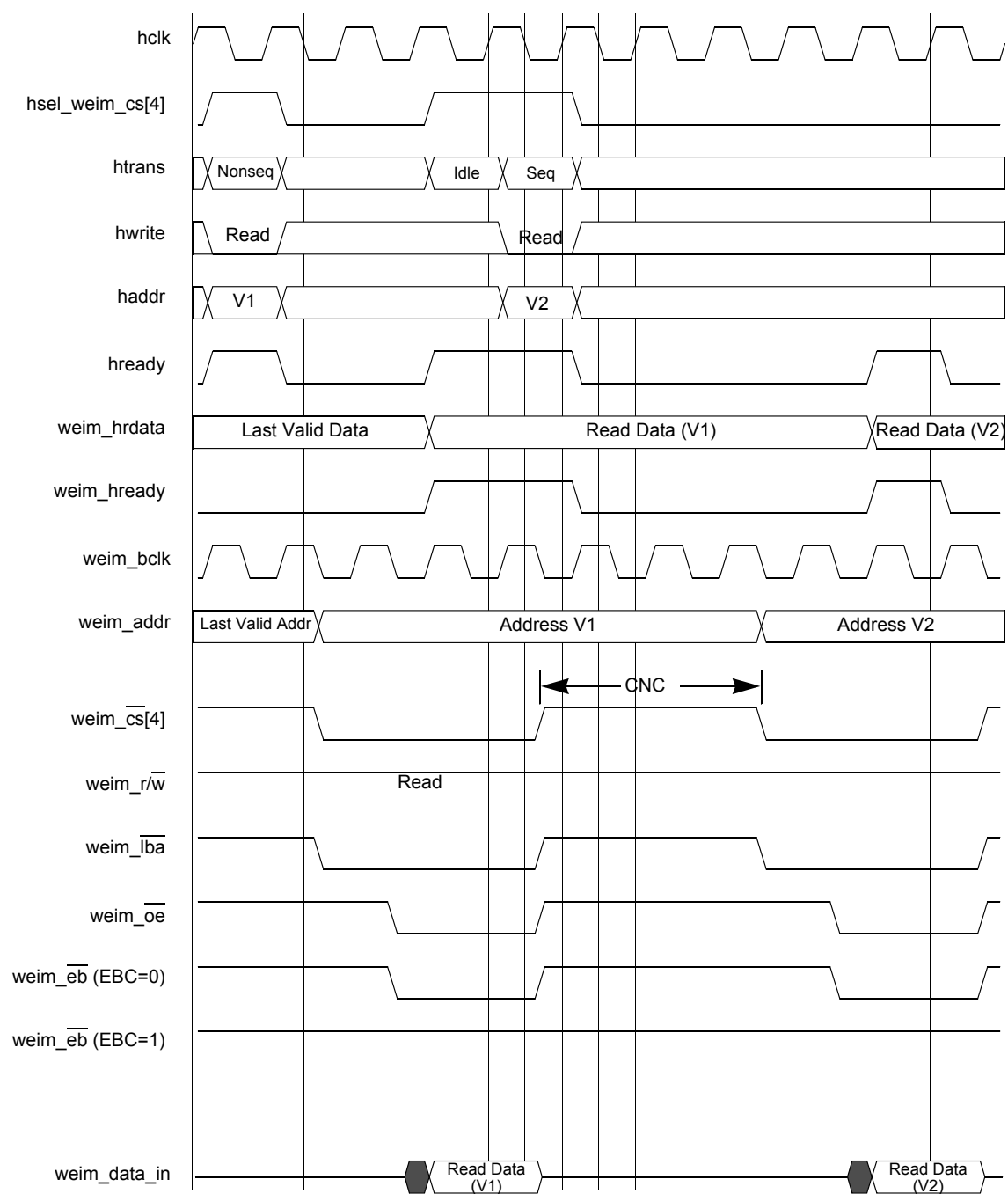


Figure 24. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

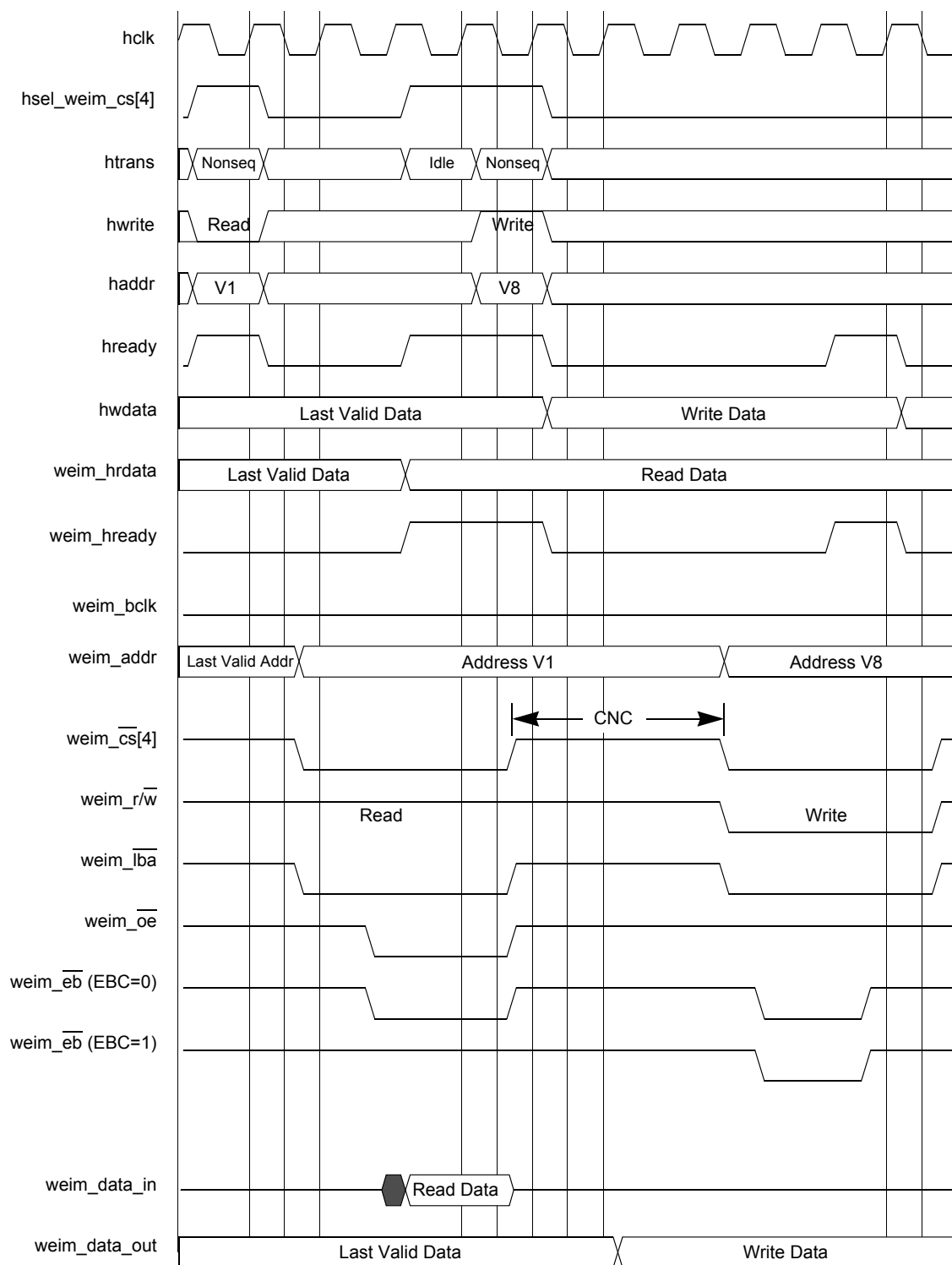


Figure 25. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF

Specifications

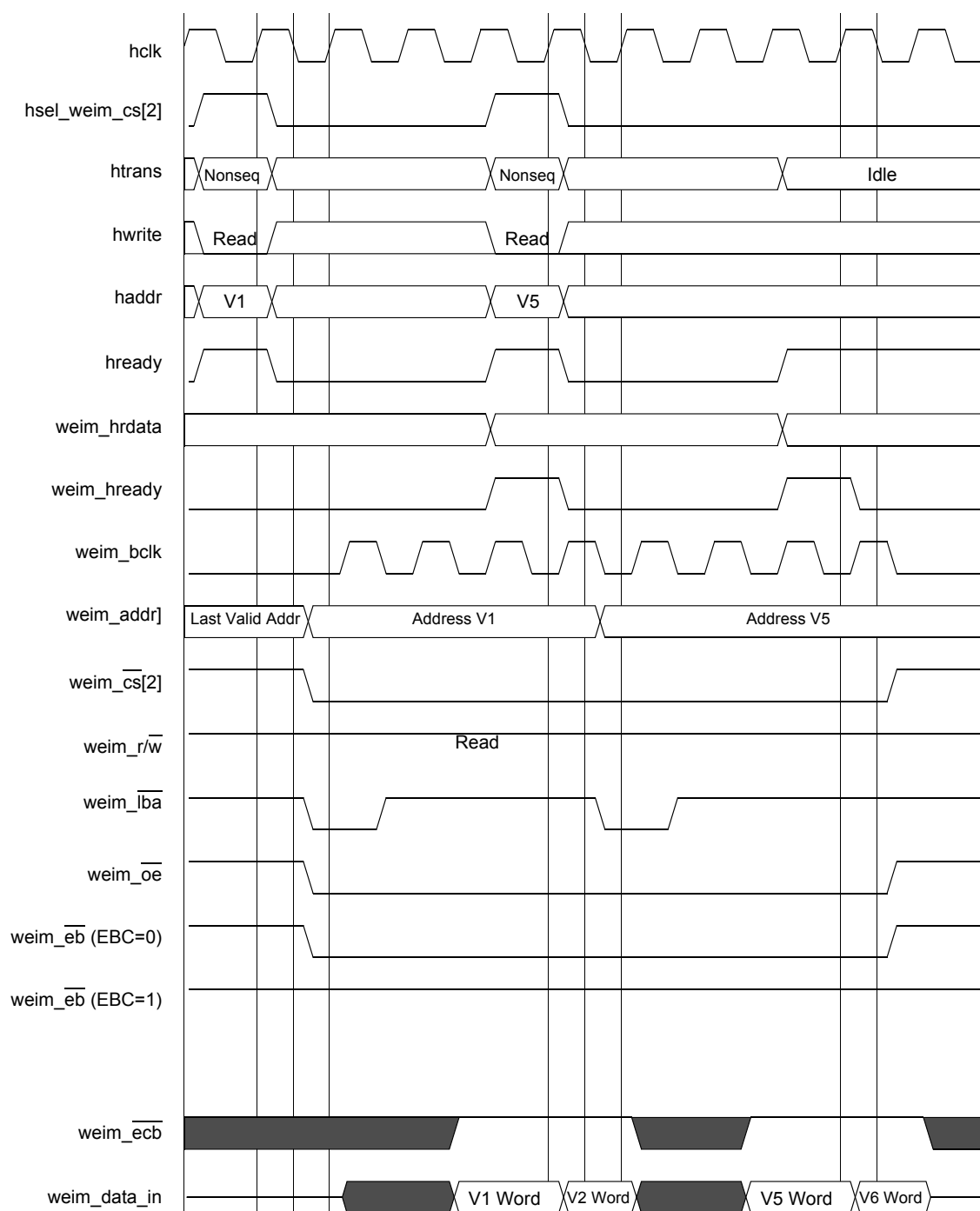


Figure 26. WSC = 3, SYNC = 1, A.HALF/E.HALF

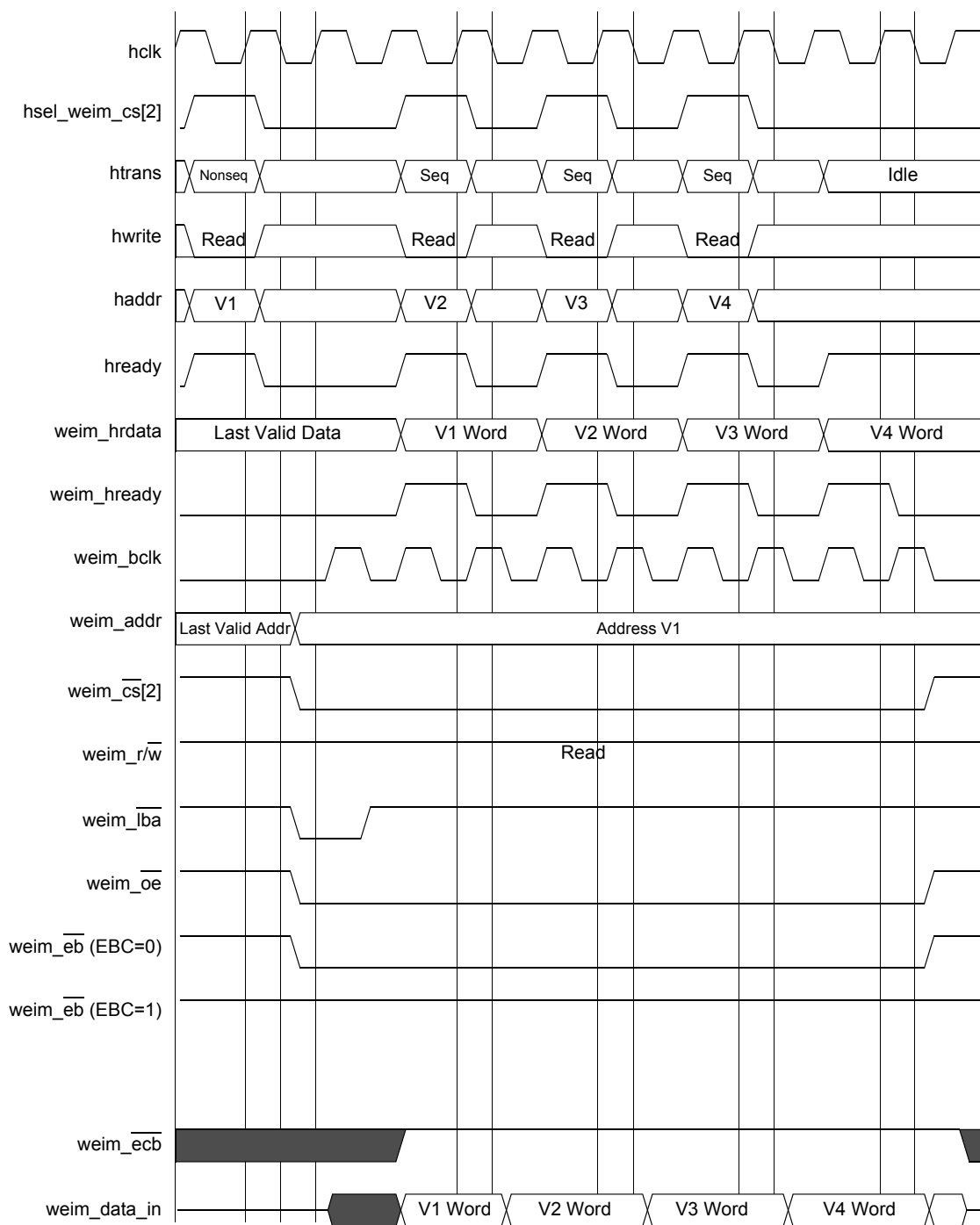


Figure 27. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD

Specifications

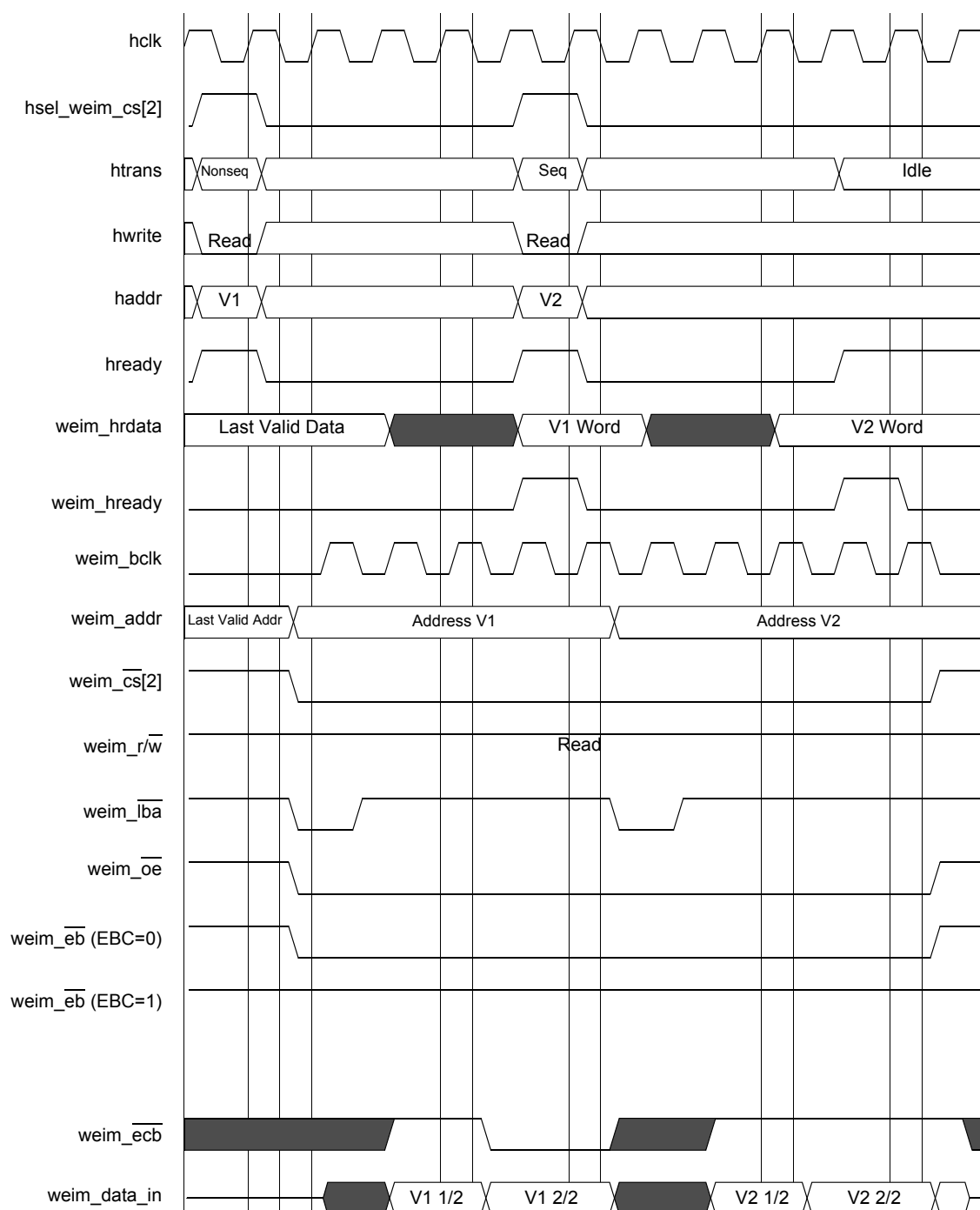


Figure 28. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

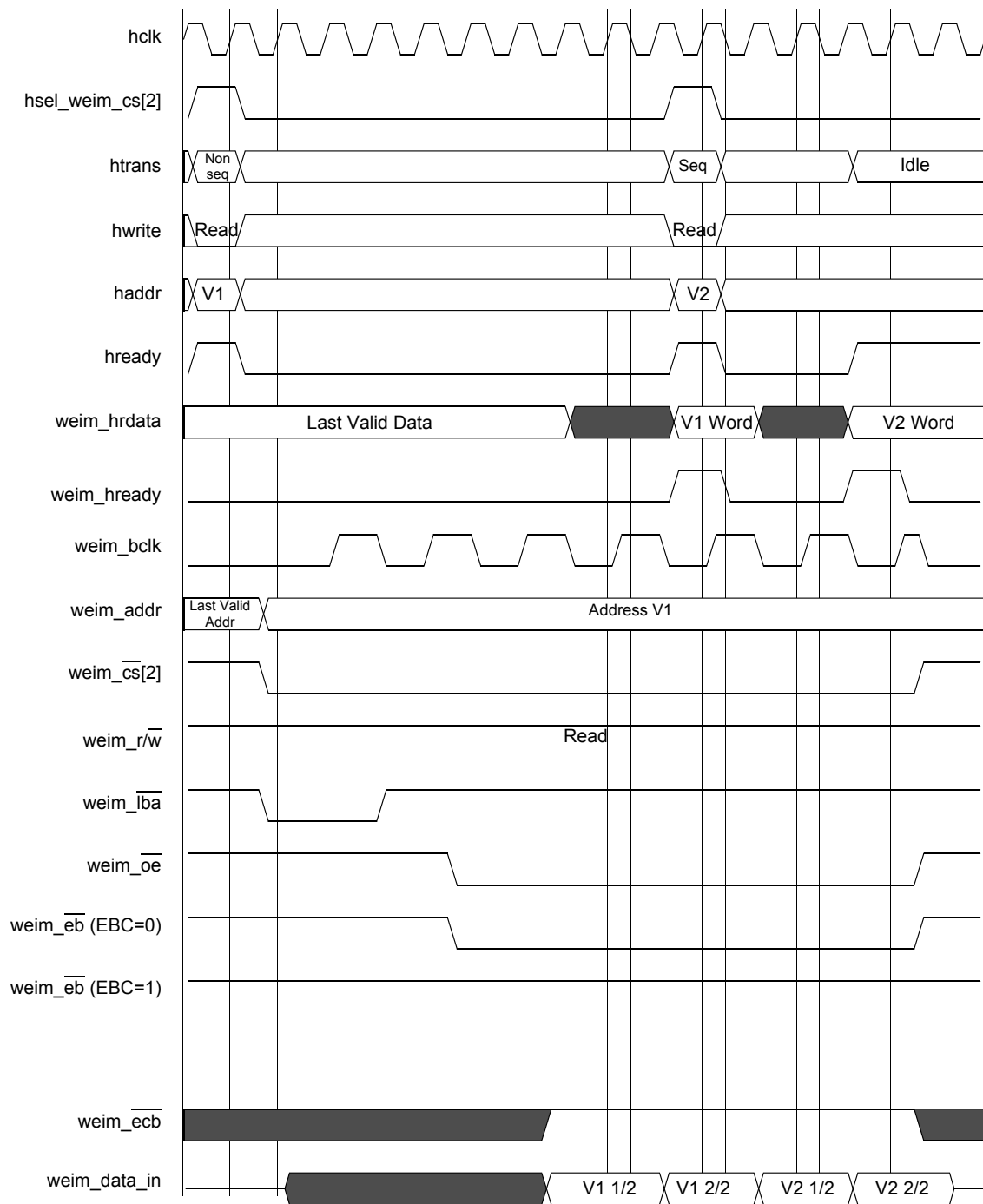


Figure 29. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF

Specifications

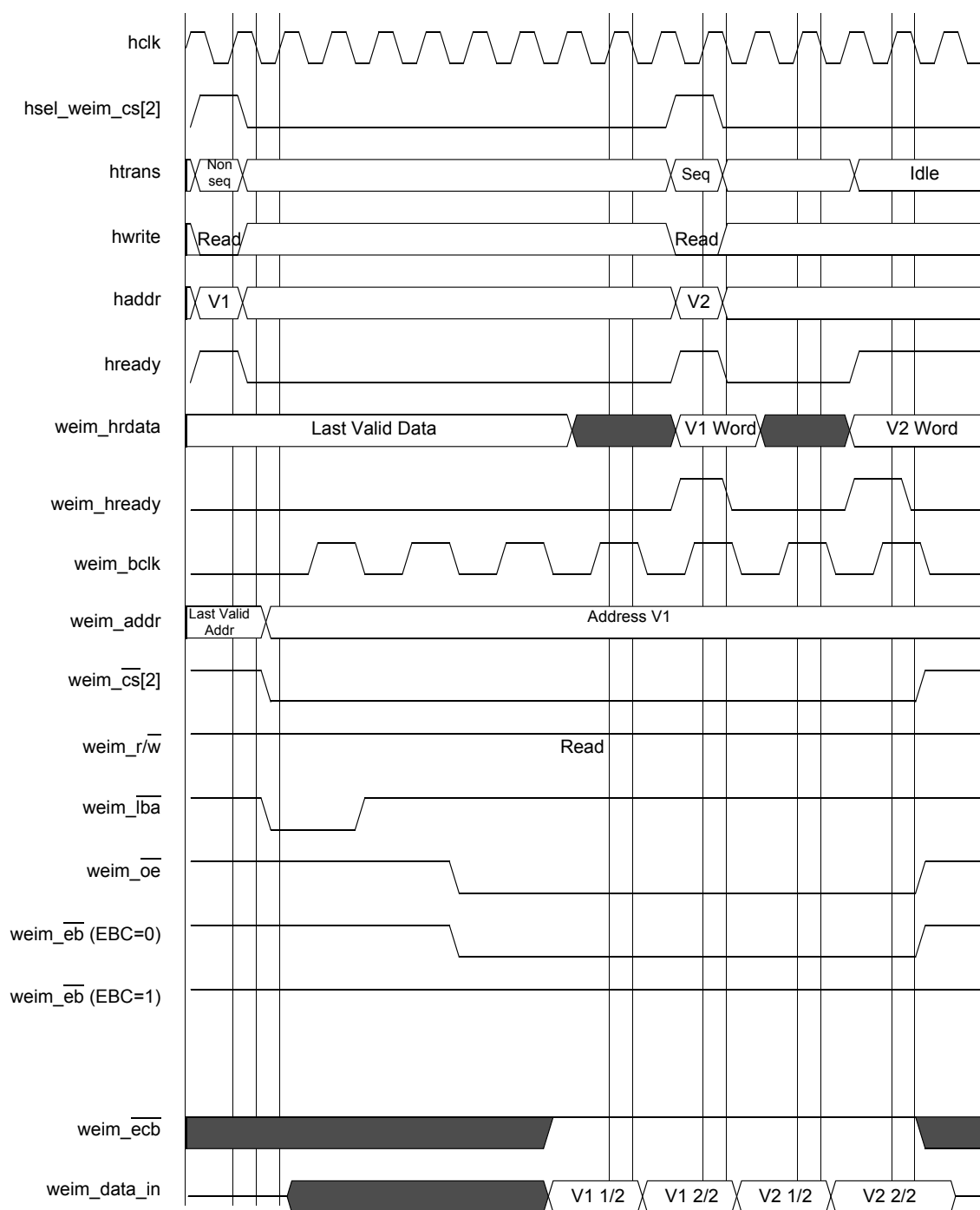


Figure 30. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

3.9 SPI Timing Diagrams

To utilize the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the \overline{SS} signal (output) and the $\overline{SPI_RDY}$ signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, \overline{SS} becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 31 through Figure 35 show the timing relationship of the master SPI using different triggering mechanisms.

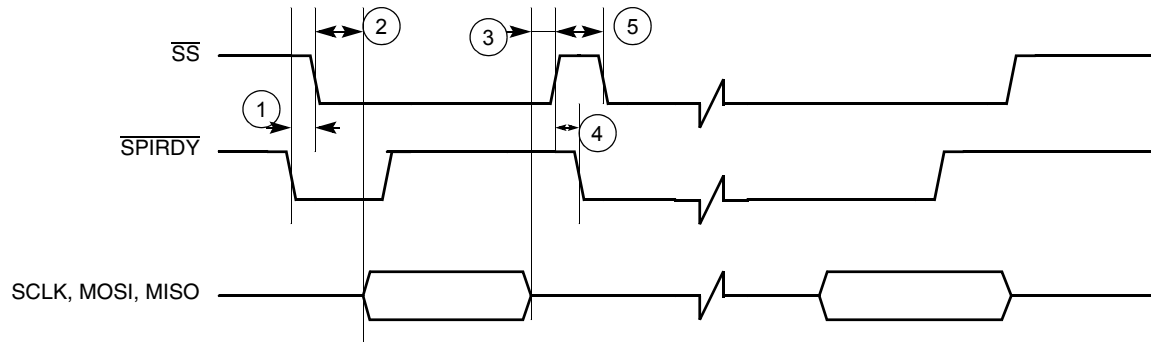


Figure 31. Master SPI Timing Diagram Using $\overline{SPI_RDY}$ Edge Trigger

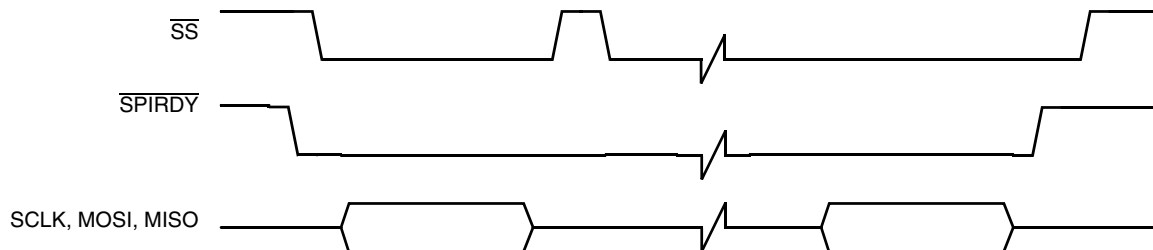


Figure 32. Master SPI Timing Diagram Using $\overline{SPI_RDY}$ Level Trigger

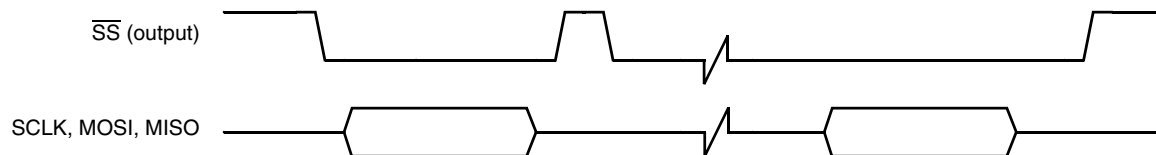


Figure 33. Master SPI Timing Diagram Ignore $\overline{SPI_RDY}$ Level Trigger

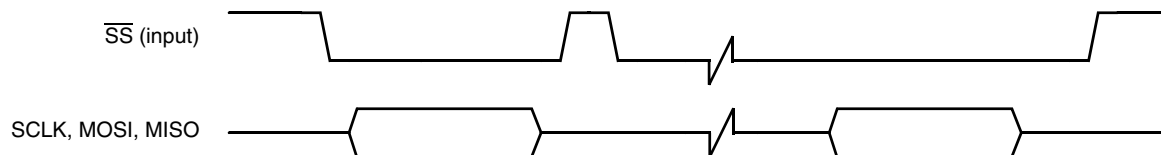


Figure 34. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

Specifications

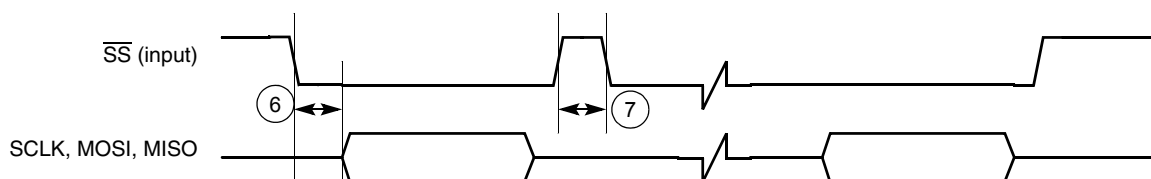


Figure 35. Slave SPI Timing Diagram FIFO Advanced by \overline{SS} Rising Edge

Table 14. Timing Parameter Table for Figure 31 through Figure 35

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	$\overline{SPI_RDY}$ to \overline{SS} output low	$2T^1$	—	$2T^1$	—	ns
2	\overline{SS} output low to first SCLK edge	$3 \cdot T_{sclk}^2$	—	$3 \cdot T_{sclk}^2$	—	ns
3	Last SCLK edge to \overline{SS} output high	$2 \cdot T_{sclk}$	—	$2 \cdot T_{sclk}$	—	ns
4	\overline{SS} output high to $\overline{SPI_RDY}$ low	0	—	0	—	ns
5	\overline{SS} output pulse width	$T_{sclk} + WAIT^3$	—	$T_{sclk} + WAIT^3$	—	ns
6	\overline{SS} input low to first SCLK edge	T	—	T	—	ns
7	\overline{SS} input pulse width	T	—	T	—	ns

1. T = CSPI system clock period (PERCLK2).
2. T_{sclk} = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

3.10 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MXL Reference Manual*.

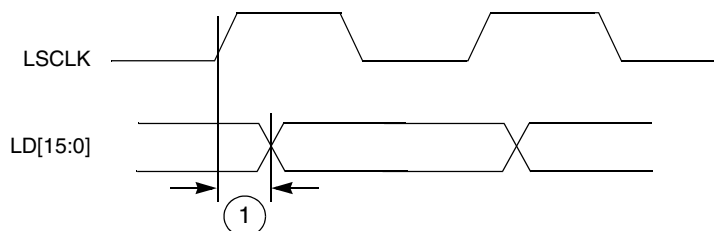


Figure 36. SCLK to LD Timing Diagram

Table 15. LCDC SCLK Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SCLK to LD valid	—	2	—	2	ns

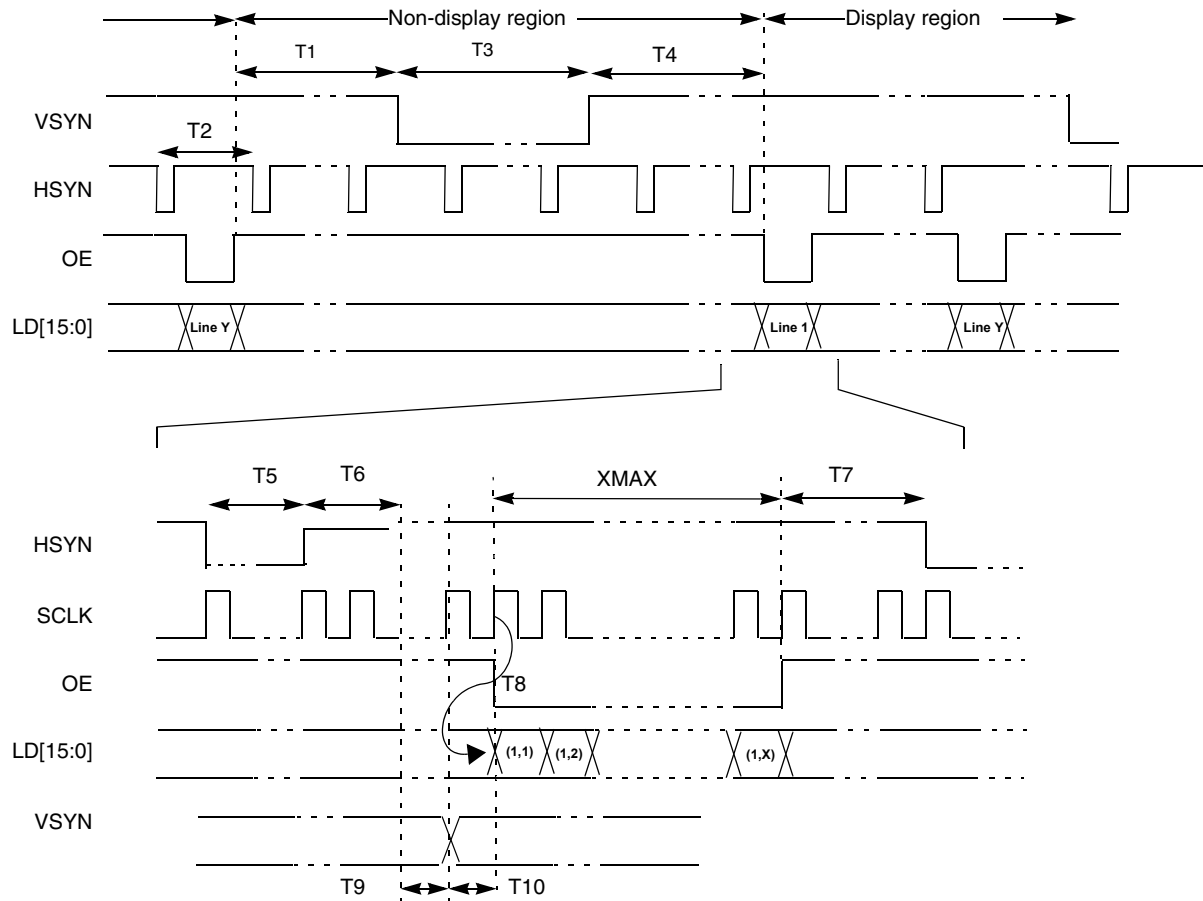


Figure 37. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Table 16. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Corresponding Register Value	Unit
T1	End of OE to beginning of VSYN	$T5+T6+T7+T9$	$(VWAIT1 \cdot T2)+T5+T6+T7+T9$	Ts
T2	HSYN period	$XMAX+5$	$XMAX+T5+T6+T7+T9+T10$	Ts
T3	VSYN pulse width	T2	$VWIDTH \cdot (T2)$	Ts
T4	End of VSYN to beginning of OE	2	$VWAIT2 \cdot (T2)$	Ts
T5	HSYN pulse width	1	$HWIDTH+1$	Ts
T6	End of HSYN to beginning to T9	1	$HWAIT2+1$	Ts

Table 16. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing (Continued)

Symbol	Description	Minimum	Corresponding Register Value	Unit
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts
T8	SCLK to valid LD data	-3	3	ns
T9	End of HSYN idle2 to VSYN edge (for non-display region)	2	2	Ts
T9	End of HSYN idle2 to VSYN edge (for Display region)	1	1	Ts
T10	VSYN to OE active (Sharp = 0) when VWAIT2 = 0	1	1	Ts
T10	VSYN to OE active (Sharp = 1) when VWAIT2 = 0	2	2	Ts
Note: <ul style="list-style-type: none"> Ts is the SCLK period which equals $\text{LCDC_CLK} / (\text{PCD} + 1)$. Normally $\text{LCDC_CLK} = 15\text{ns}$. VSYN, HSYN and OE can be programmed as active high or active low. In Figure 37, all 3 signals are active low. The polarity of SCLK and LD[15:0] can also be programmed. SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 37, SCLK is always active. For T9 non-display region, VSYN is non-active. It is used as an reference. XMAX is defined in pixels. 				

3.11 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

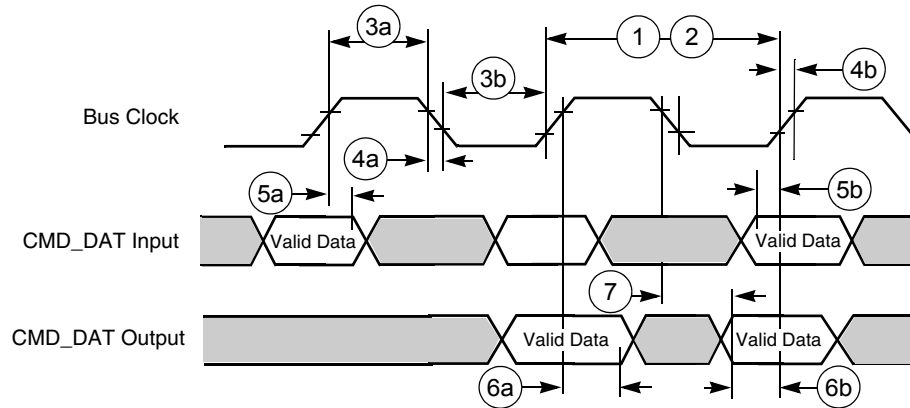


Figure 38. Chip-Select Read Cycle Timing Diagram

Table 17. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0 \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP) ¹ —10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode ²	0	400	0	400	kHz
3a	Clock high time ¹ —10/30 cards	6/33	—	10/50	—	ns
3b	Clock low time ¹ —10/30 cards	15/75	—	10/50	—	ns
4a	Clock fall time ¹ —10/30 cards	—	10/50 (5.00) ³	—	10/50	ns
4b	Clock rise time ¹ —10/30 cards	—	14/67 (6.67) ³	—	10/50	ns
5a	Input hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
5b	Input setup time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
6a	Output hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
6b	Output setup time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
7	Output delay time ³	0	16	0	14	ns

1. $C_L \leq 100$ pF / 250 pF (10/30 cards)

2. $C_L \leq 250$ pF (21 cards)

3. $C_L \leq 25$ pF (1 card)

3.11.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is N_{CR} clock cycles as illustrated in Figure 39. The symbols for Figure 39 through Figure 43 are defined in Table 18.

Table 18. State Signal Parameters for Figure 39 through Figure 43

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

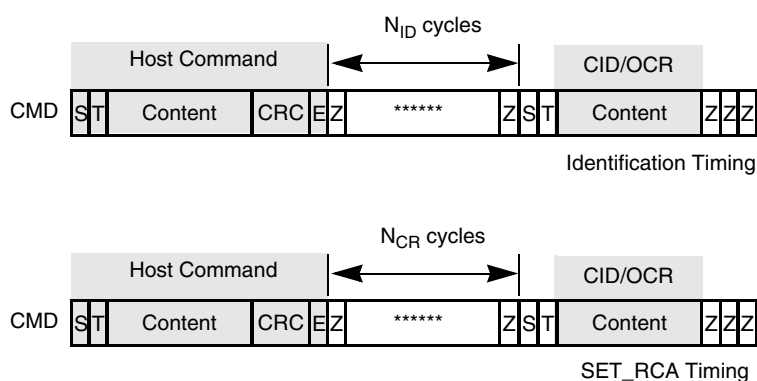


Figure 39. Timing Diagrams at Identification Mode

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 40, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods N_{RC} and N_{CC} .

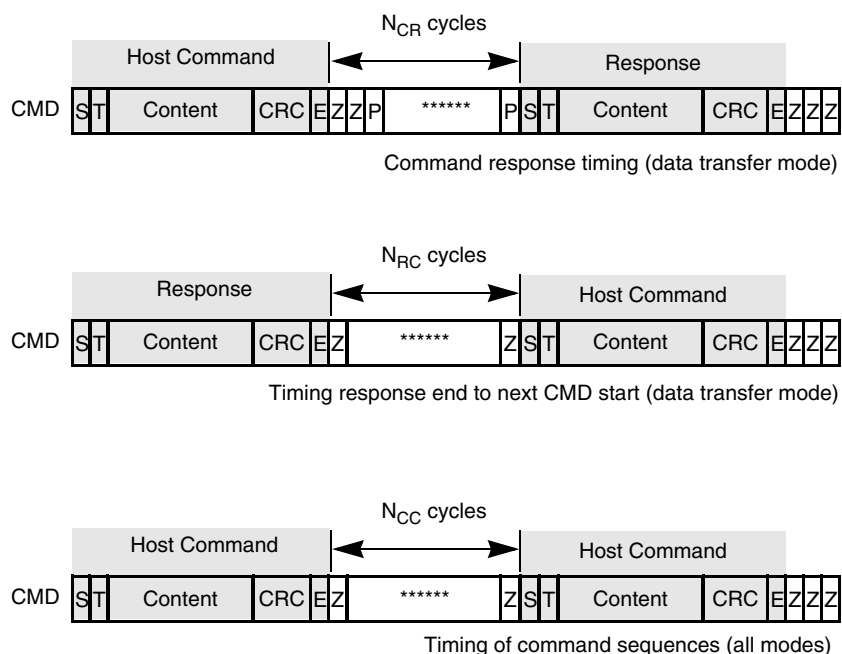


Figure 40. Timing Diagrams at Data Transfer Mode

Figure 41 on page 52 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay N_{AC} , beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance N_{AC} until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

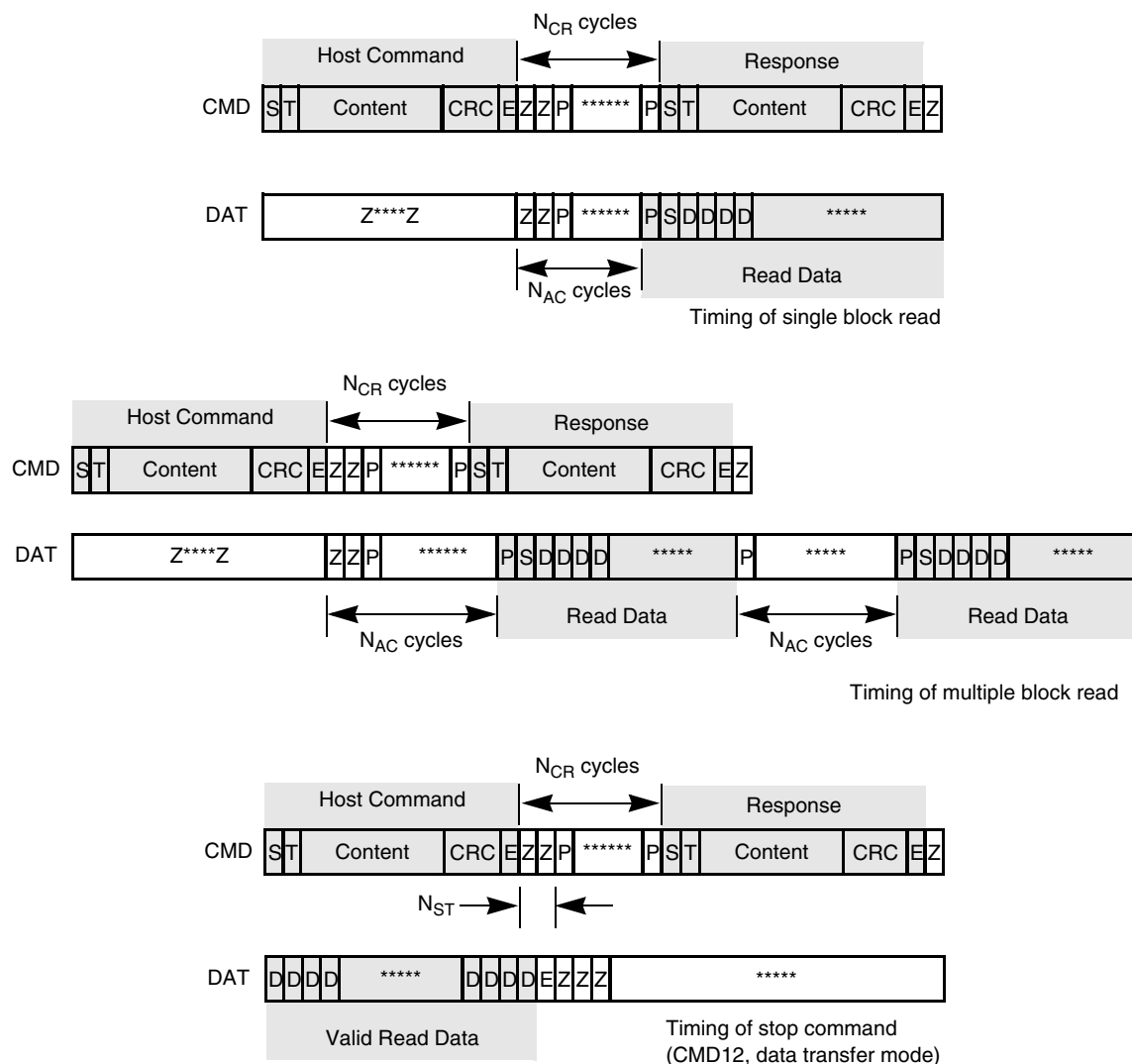


Figure 41. Timing Diagrams at Data Read

Figure 42 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

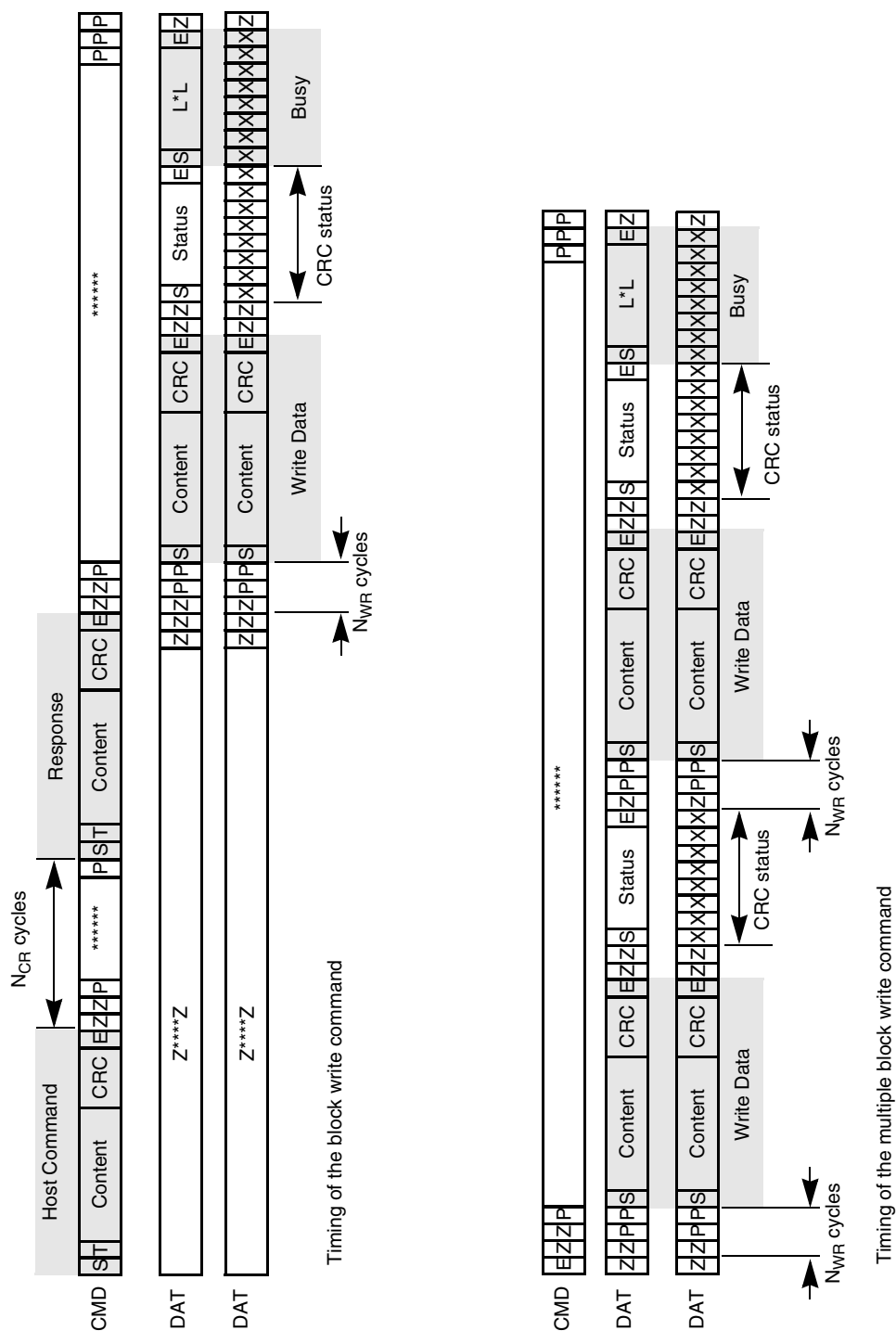


Figure 42. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 43 shows the different scenarios on the bus.

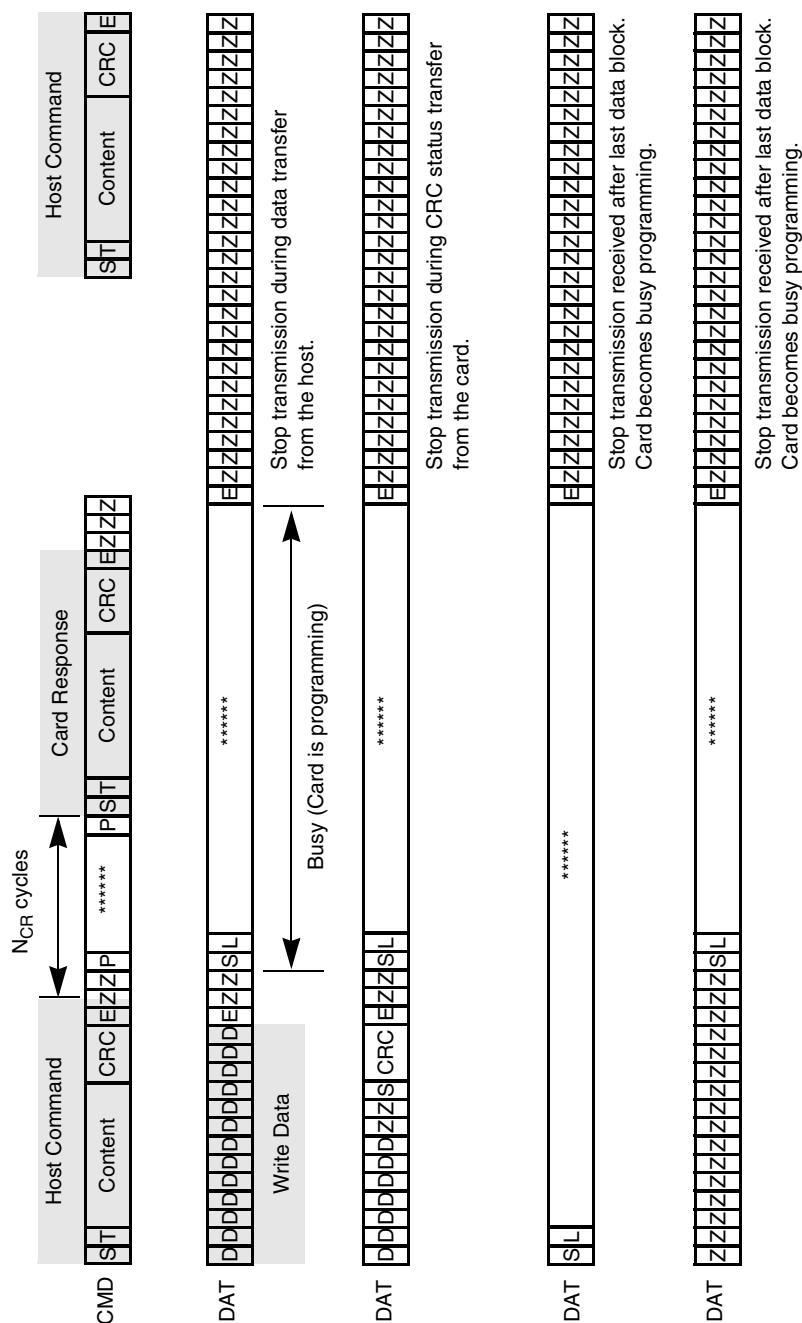


Figure 43. Stop Transmission During Different Scenarios

Table 19. Timing Values for Figure 39 through Figure 43

Parameter	Symbol	Minimum	Maximum	Unit	Parameter
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL))					MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL))
Command response cycle	NCR	2	64	Clock cycles	Command response cycle
Identification response cycle	NID	5	5	Clock cycles	Identification response cycle
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles	Access time delay cycle
Command read cycle	NRC	8	—	Clock cycles	Command read cycle
Command-command cycle	NCC	8	—	Clock cycles	Command-command cycle
Command write cycle	NWR	2	—	Clock cycles	Command write cycle
Stop transmission cycle	NST	2	2	Clock cycles	Stop transmission cycle
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]					TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]

3.11.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the "Interrupt Period" during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

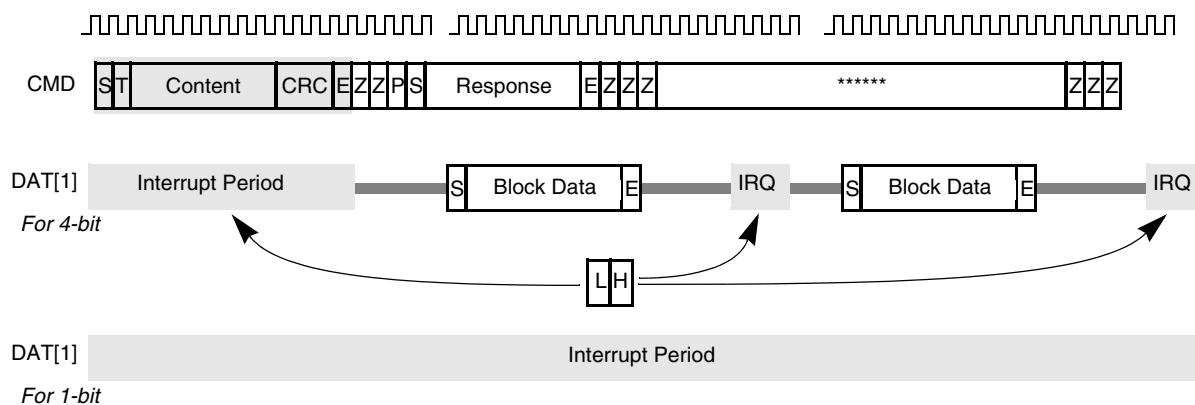


Figure 44. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

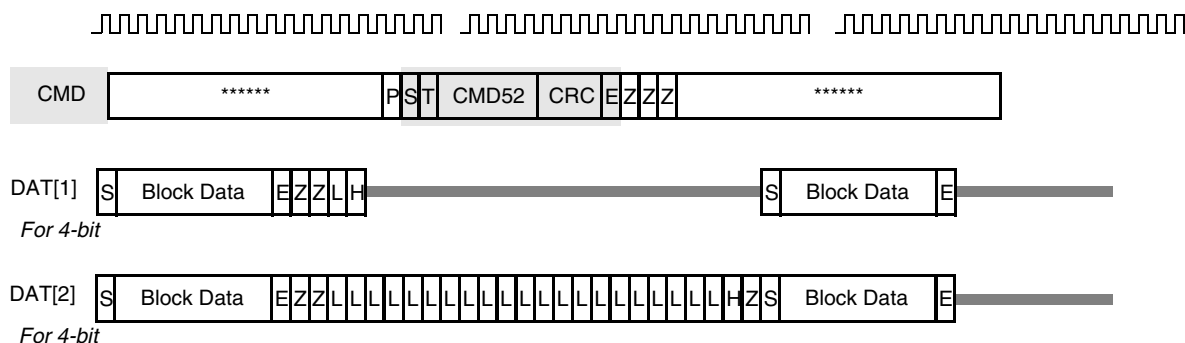


Figure 45. SDIO ReadWait Timing Diagram

3.12 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

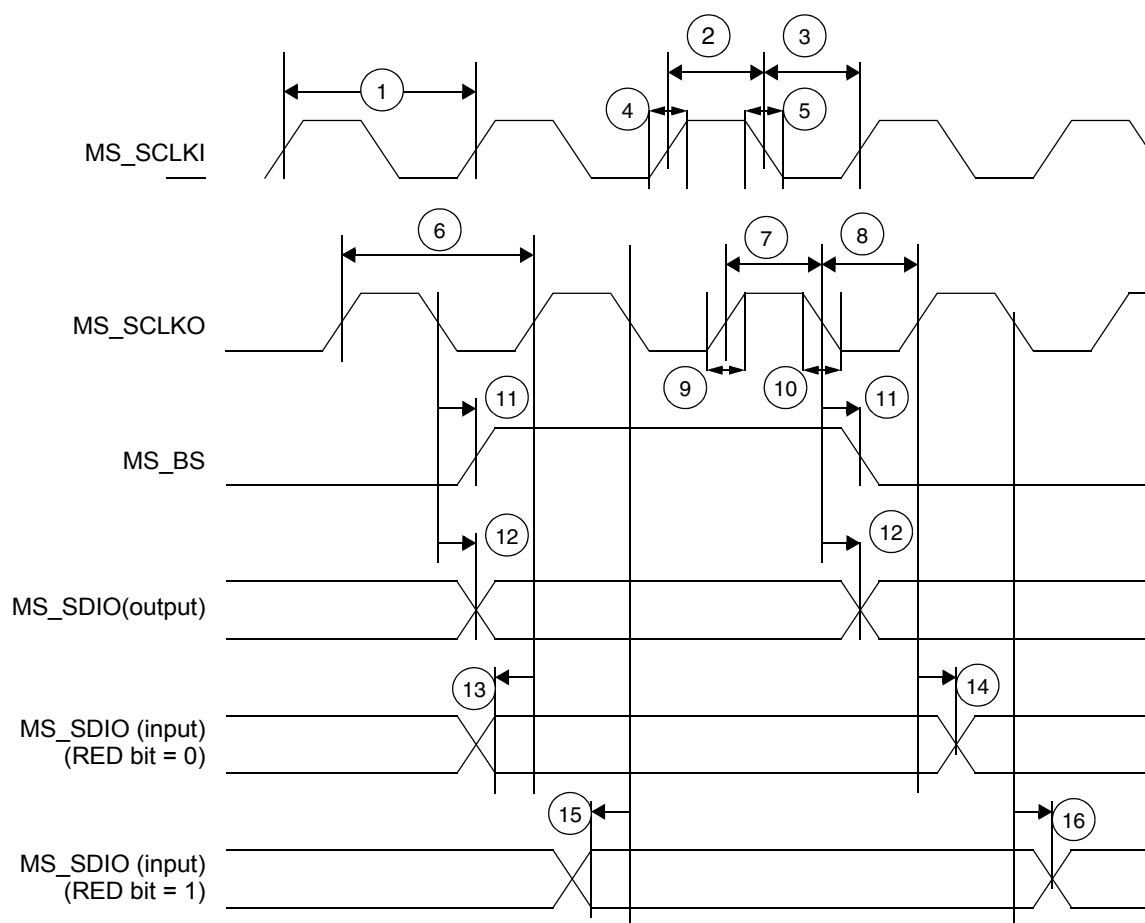


Figure 46. MSHC Signal Timing Diagram

Table 20. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	—	25	MHz
2	MS_SCLKI high pulse width	20	—	ns
3	MS_SCLKI low pulse width	20	—	ns
4	MS_SCLKI rise time	—	3	ns
5	MS_SCLKI fall time	—	3	ns
6	MS_SCLKO frequency ¹	—	25	MHz
7	MS_SCLKO high pulse width ¹	20	—	ns
8	MS_SCLKO low pulse width ¹	15	—	ns
9	MS_SCLKO rise time ¹	—	5	ns

Table 20. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3V		Unit
		Minimum	Maximum	
10	MS_SCLKO fall time ¹	—	5	ns
11	MS_BS delay time ¹	—	3	ns
12	MS_SDIO output delay time ^{1,2}	—	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0) ³	18	—	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0) ³	0	—	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1) ⁴	23	—	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1) ⁴	0	—	ns

1. Loading capacitor condition is less than or equal to 30pF.
2. An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.
3. If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.
4. If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

3.13 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 47 and the parameters are listed in Table 21.

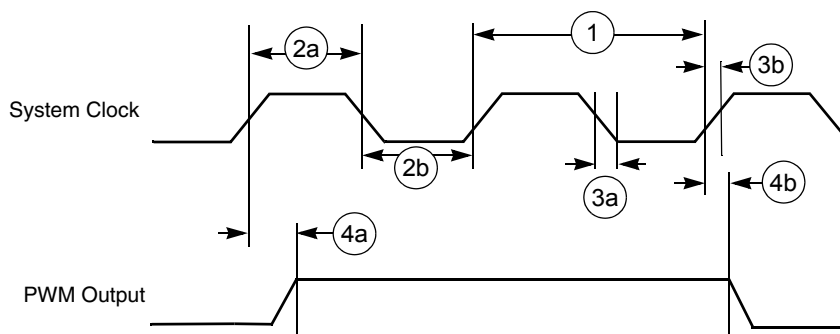


Figure 47. PWM Output Timing Diagram

Table 21. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency ¹	0	87	0	100	MHz
2a	Clock high time ¹	3.3	—	5/10	—	ns
2b	Clock low time ¹	7.5	—	5/10	—	ns
3a	Clock fall time ¹	—	5	—	5/10	ns
3b	Clock rise time ¹	—	6.67	—	5/10	ns
4a	Output delay time ¹	5.7	—	5	—	ns
4b	Output setup time ¹	5.7	—	5	—	ns

1. C_L of PWMO = 30 pF

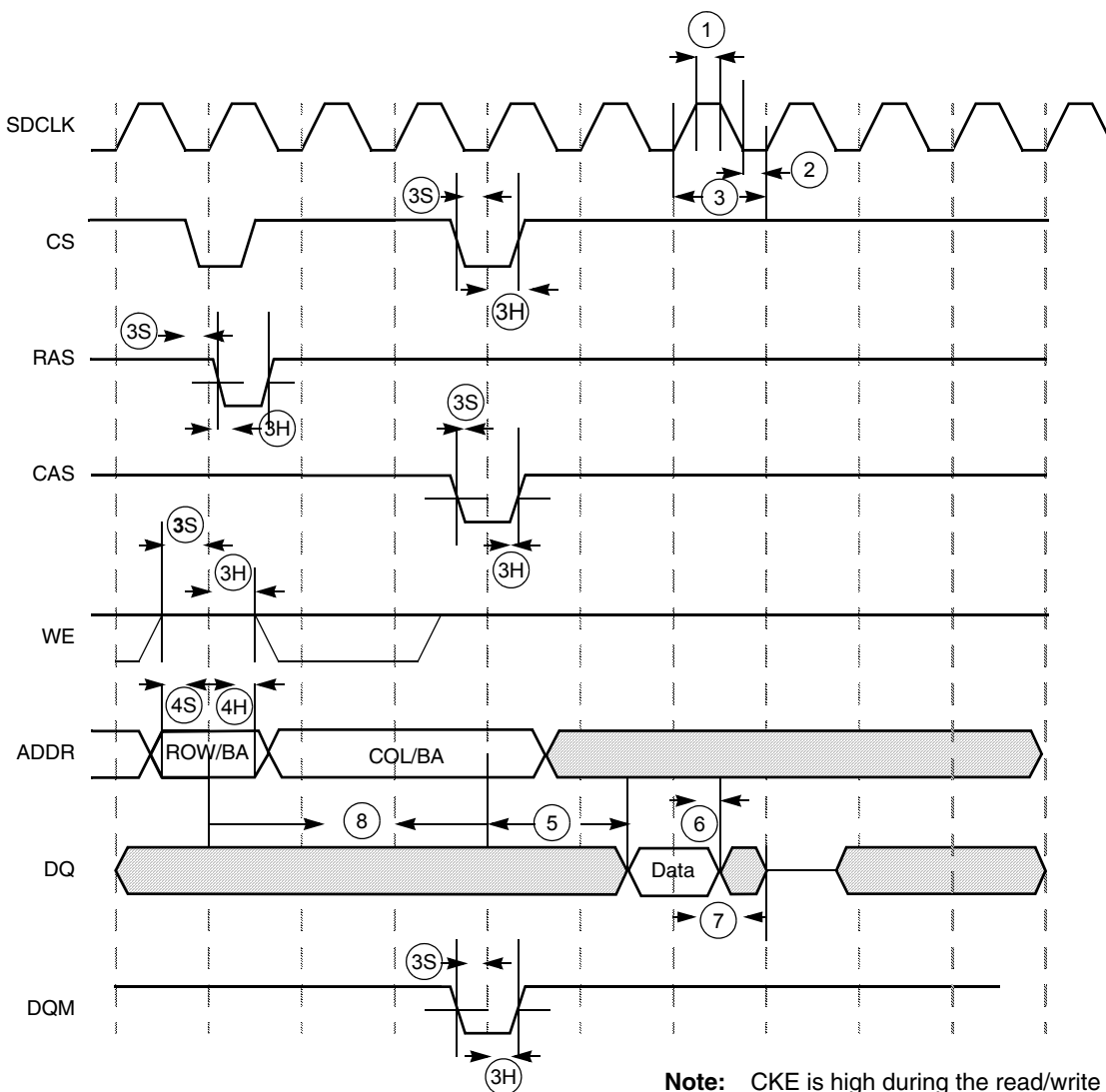
3.14 SDRAM Controller

A write to an address within the memory region initiates the program sequence. The first command issued to the SyncFlash is Load Command Register. The value in A [7:0] determines which operation the command performs. For this write setup operation, an address of 0x40 is hardware generated. The bank and other address lines are driven with the address to be programmed. The next command is Active which registers the row address and confirms the bank address. The third command supplies the column address, re-confirms the bank address, and supplies the data to be written. SyncFlash does not support burst writes, therefore a Burst Terminate command is not required.

A read to the memory region initiates the status read sequence. The first command issued to the SyncFlash is the Load Command Register with A [7:0] set to 0x70 which corresponds to the Read Status Register operation. The bank and other address lines are driven to the selected address. The second command is

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Active which sets up the status register read. The bank and row addresses are driven during this command. The third command of the triplet is Read. Bank and column addresses are driven on the address bus during this command. Data is returned from memory on the low order 8 data bits following the CAS latency.



Note: CKE is high during the read/write cycle.

Figure 48. SDRAM/SyncFlash Read Cycle Timing Diagram

Table 22. SDRAM Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	—	4	—	ns
2	SDRAM clock low-level width	6	—	4	—	ns
3	SDRAM clock cycle time	11.4	—	10	—	ns
3S	CS, RAS, CAS, WE, DQM setup time	3.42	—	3	—	ns

Table 22. SDRAM Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
3H	CS, RAS, CAS, WE, DQM hold time	2.28	—	2	—	ns
4S	Address setup time	3.42	—	3	—	ns
4H	Address hold time	2.28	—	2	—	ns
5	SDRAM access time (CL = 3)	—	6.84	—	6	ns
5	SDRAM access time (CL = 2)	—	6.84	—	6	ns
5	SDRAM access time (CL = 1)	—	22	—	22	ns
6	Data out hold time	2.85	—	2.5	—	ns
7	Data out high-impedance time (CL = 3)	—	6.84	—	6	ns
7	Data out high-impedance time (CL = 2)	—	6.84	—	6	ns
7	Data out high-impedance time (CL = 1)	—	22	—	22	ns
8	Active to read/write command period (RC = 1)	t_{RCD}^1	—	t_{RCD}^1	—	ns

1. t_{RCD} = SDRAM clock cycle time. This settings can be found in the MC9328MXL reference manual.

Specifications

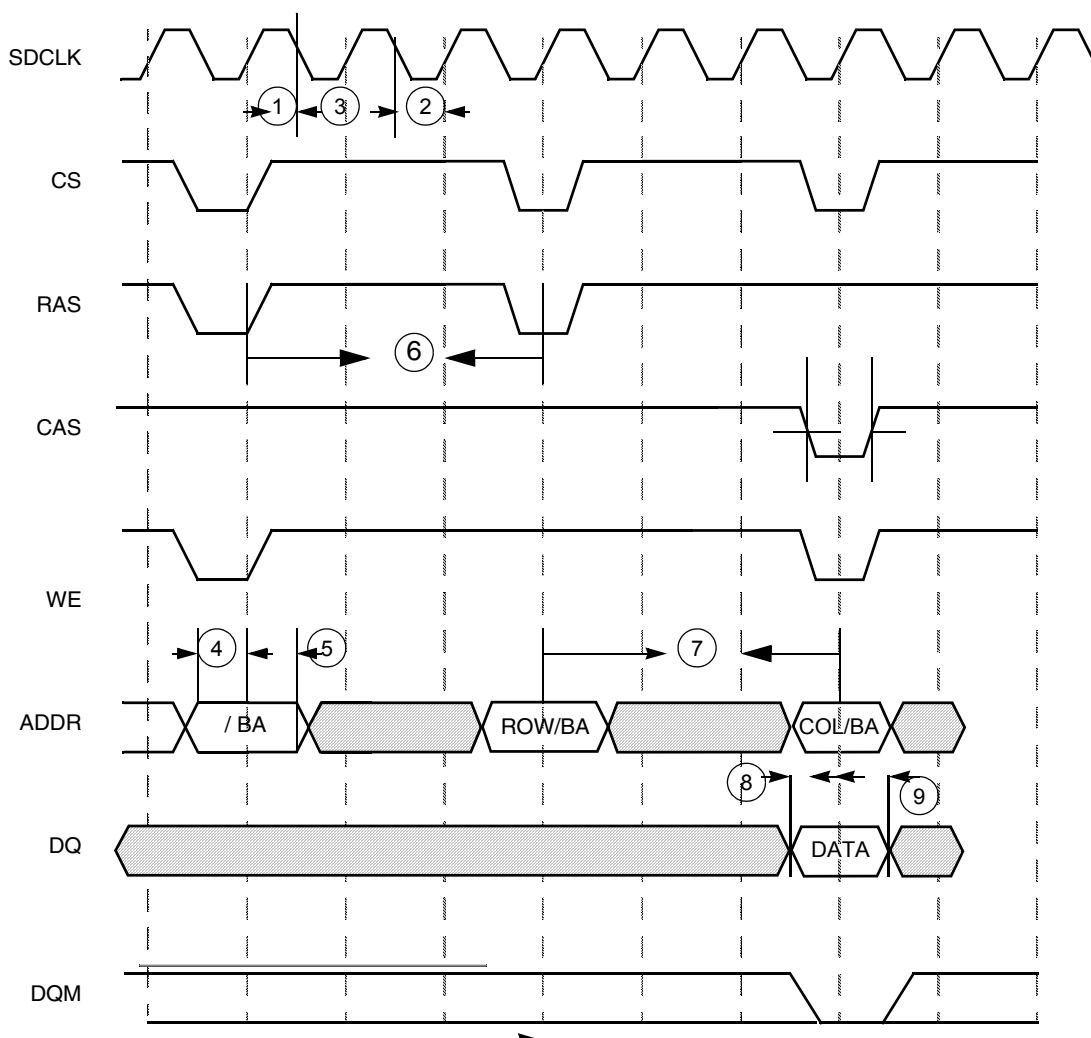


Figure 49. SDRAM/SyncFlash Write Cycle Timing Diagram

Table 23. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	—	4	—	ns
2	SDRAM clock low-level width	6	—	4	—	ns
3	SDRAM clock cycle time	11.4	—	10	—	ns
4	Address setup time	3.42	—	3	—	ns
5	Address hold time	2.28	—	2	—	ns
6	Precharge cycle period ¹	t_{RP} ²	—	t_{RP} ²	—	ns
7	Active to read/write command delay	t_{RCD} ²	—	t_{RCD} ²	—	ns

Table 23. SDRAM Write Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
8	Data setup time	4.0	—	2	—	ns
9	Data hold time	2.28	—	2	—	ns

1. Precharge cycle timing is included in the write timing diagram.
2. t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the MC9328MXL reference manual.

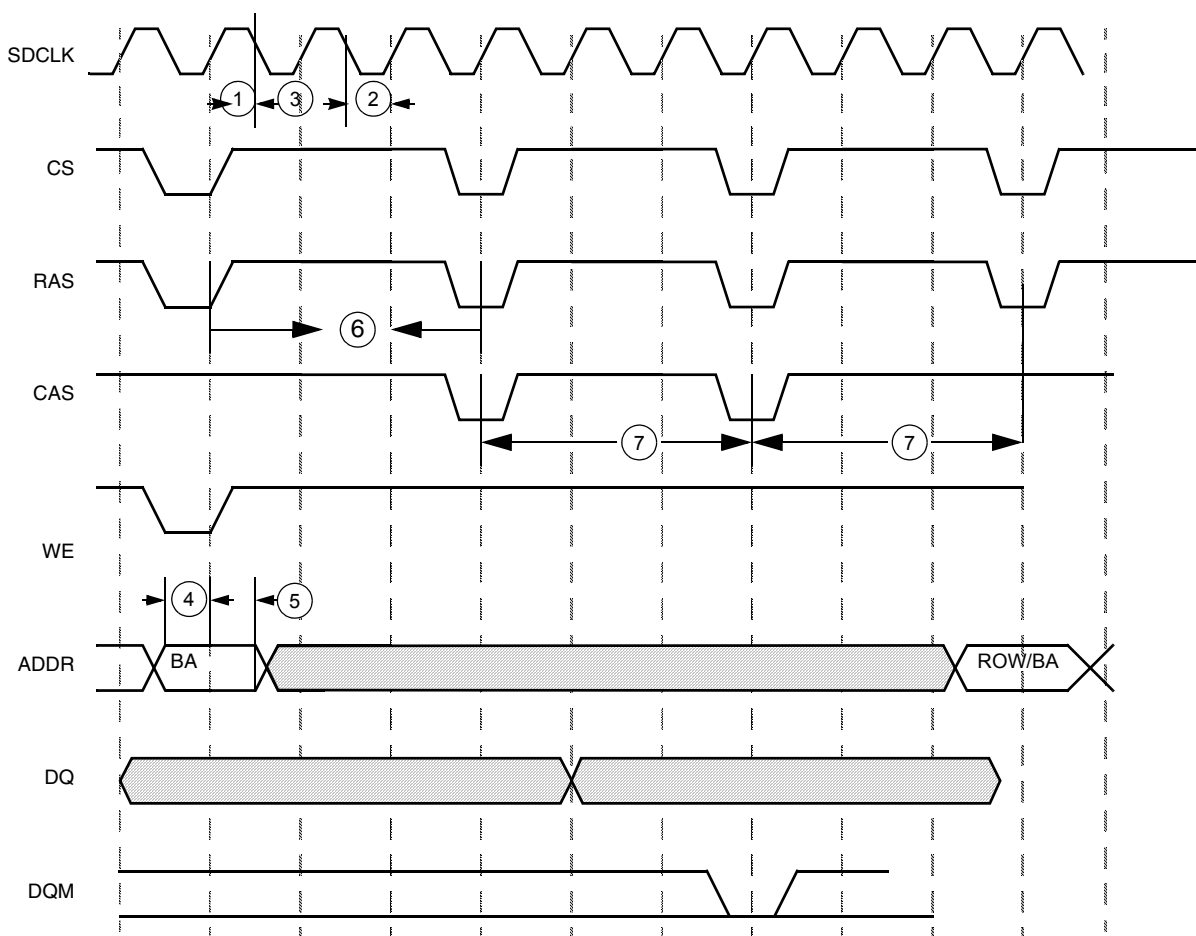


Figure 50. SDRAM Refresh Timing Diagram

Table 24. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	—	4	—	ns
2	SDRAM clock low-level width	6	—	4	—	ns

Table 24. SDRAM Refresh Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
3	SDRAM clock cycle time	11.4	—	10	—	ns
4	Address setup time	3.42	—	3	—	ns
5	Address hold time	2.28	—	2	—	ns
6	Precharge cycle period	t_{RP}^1	—	t_{RP}^1	—	ns
7	Auto precharge command period	t_{RC}^1	—	t_{RC}^1	—	ns

1. t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the MC9328MXL reference manual.

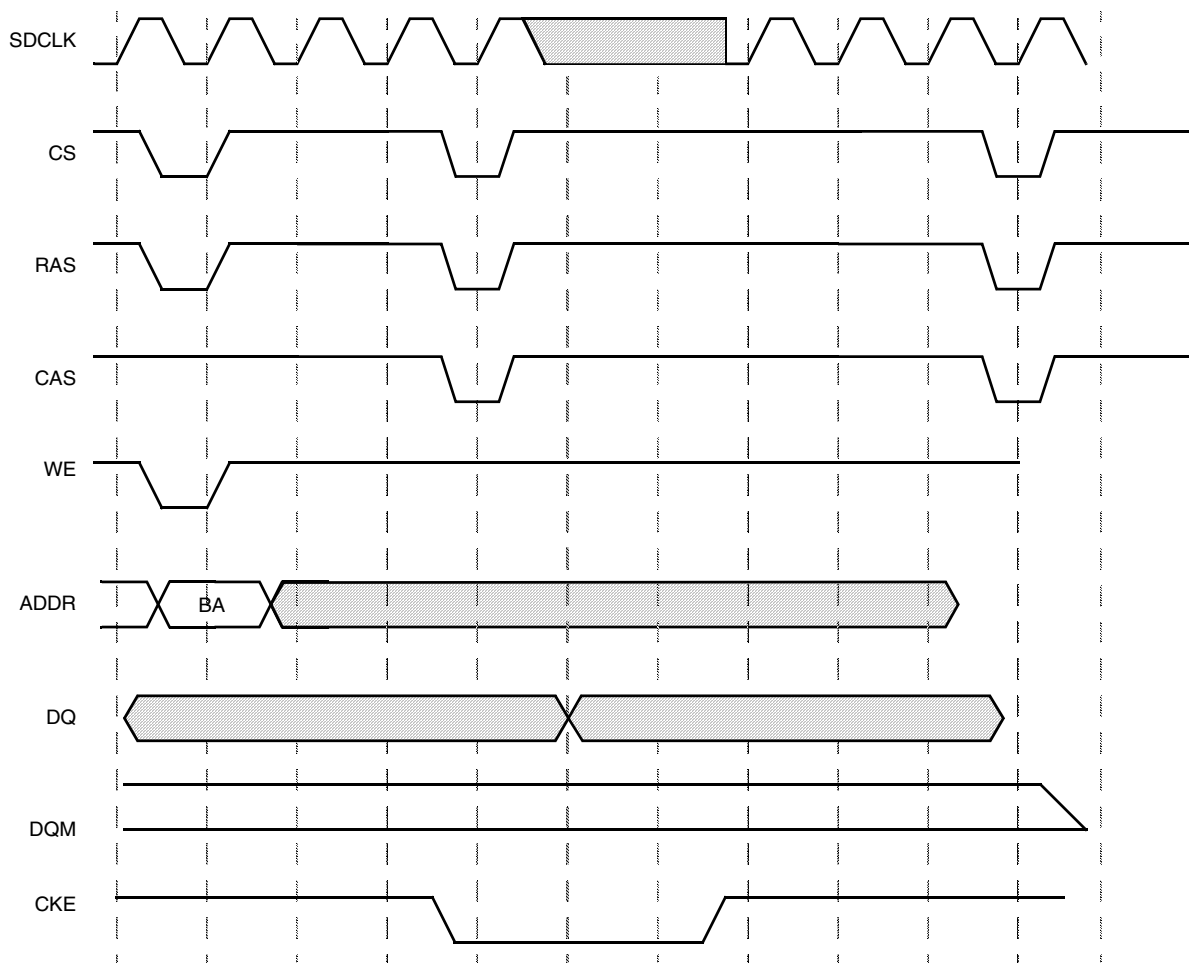


Figure 51. SDRAM Self-Refresh Cycle Timing Diagram

3.15 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

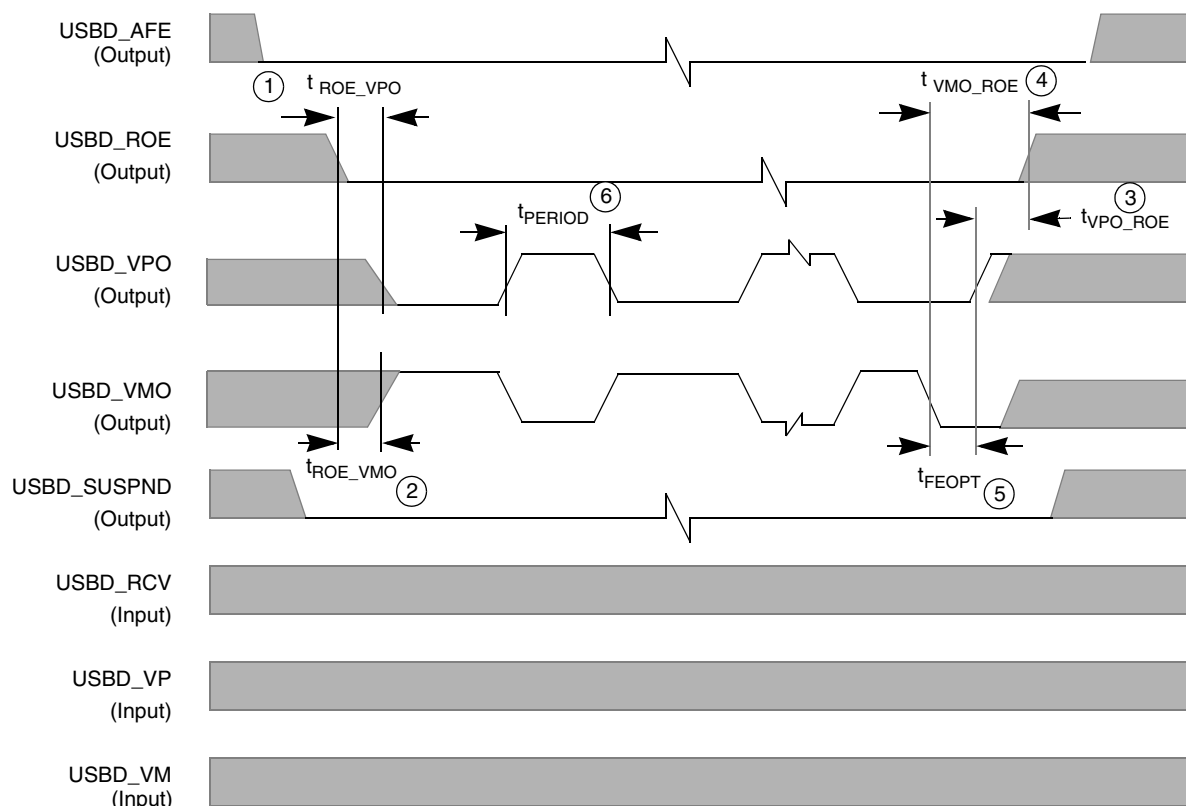


Figure 52. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 25. USB Device Timing Parameter Table for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	t_{ROE_VPO} : USBD_ROE active to USBD_VPO low	83.14	83.47	83.14	83.47	ns
2	t_{ROE_VMO} : USBD_ROE active to USBD_VMO high	81.55	81.98	81.55	81.98	ns
3	t_{VPO_ROE} : USBD_VPO high to USBD_ROE deactivated	83.54	83.80	83.54	83.80	ns

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Table 25. USB Device Timing Parameter Table for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
4	t_{VMO_ROE} ; USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.90	249.13	248.90	249.13	ns
5	t_{FEOPT} ; SE0 interval of EOP	160.00	175.00	160.00	175.00	ns
6	t_{PERIOD} ; Data transfer rate	11.97	12.03	11.97	12.03	Mb/s

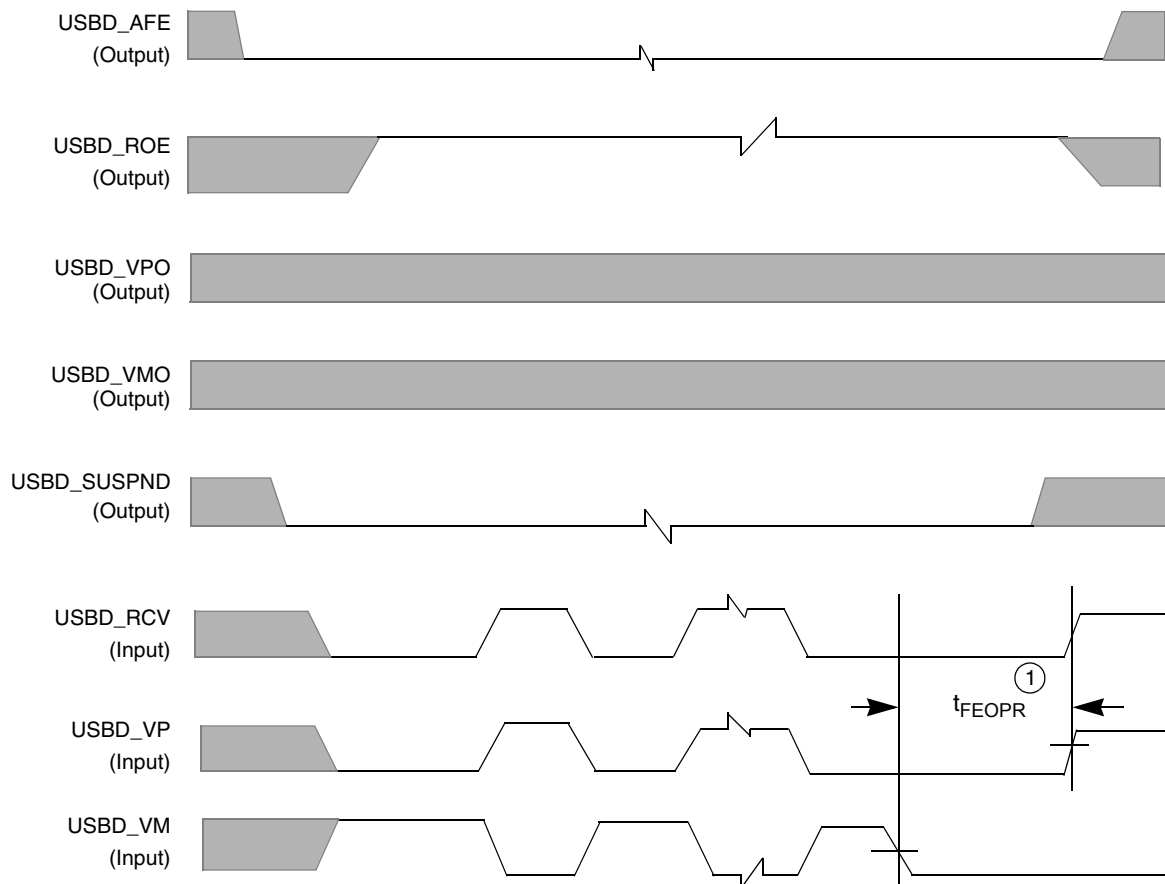


Figure 53. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 26. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	t_{FEOPR} ; Receiver SE0 interval of EOP	82	—	82	—	ns

3.16 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

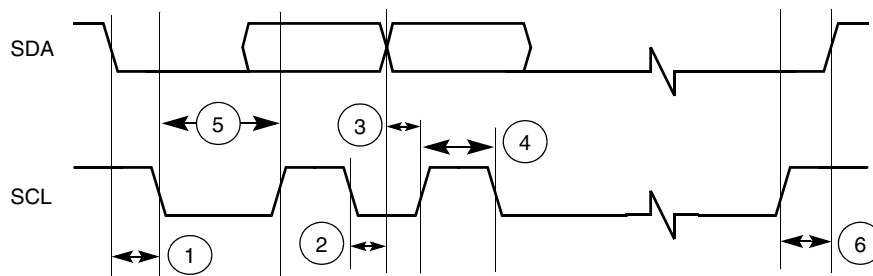


Figure 54. Definition of Bus Timing for I²C

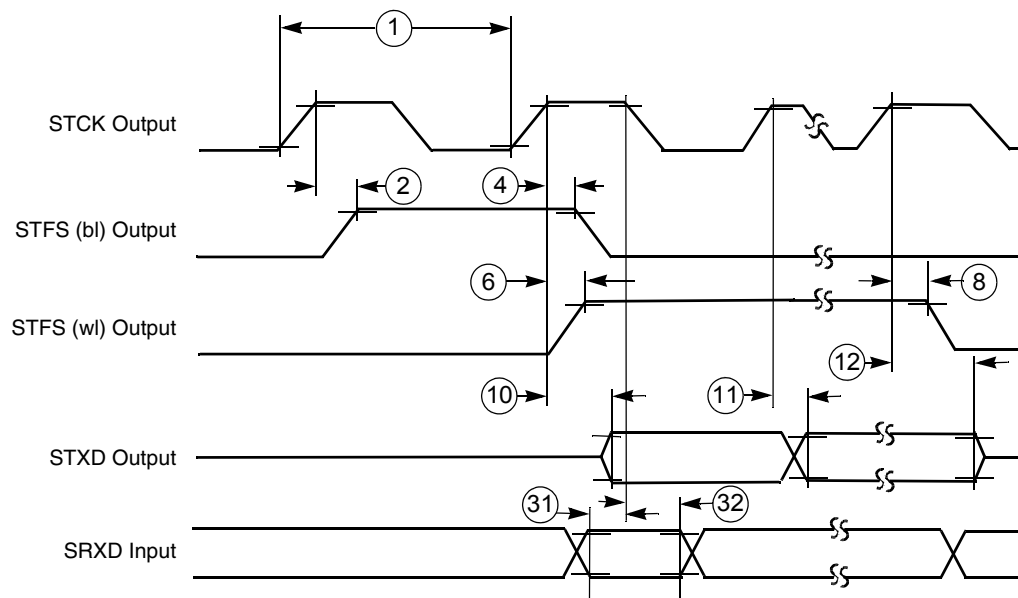
Table 27. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	—	160	—	ns
2	Data hold time	0	171	0	150	ns
3	Data setup time	11.4	—	10	—	ns
4	HIGH period of the SCL clock	80	—	120	—	ns
5	LOW period of the SCL clock	480	—	320	—	ns
6	Setup time for STOP condition	182.4	—	160	—	ns

3.17 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 56 through Figure 58 on page 69.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



Note: SRXD input in synchronous mode only.

Figure 55. SSI Transmitter Internal Clock Timing Diagram

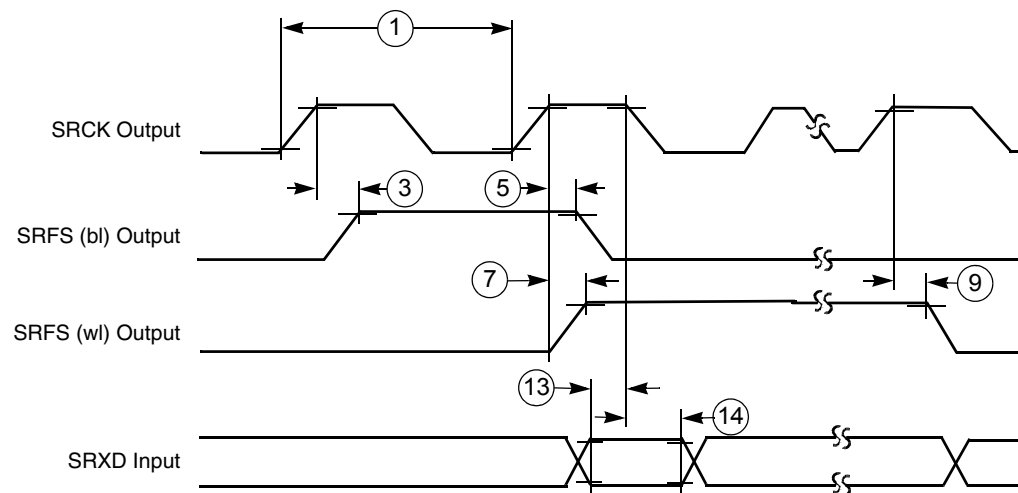


Figure 56. SSI Receiver Internal Clock Timing Diagram

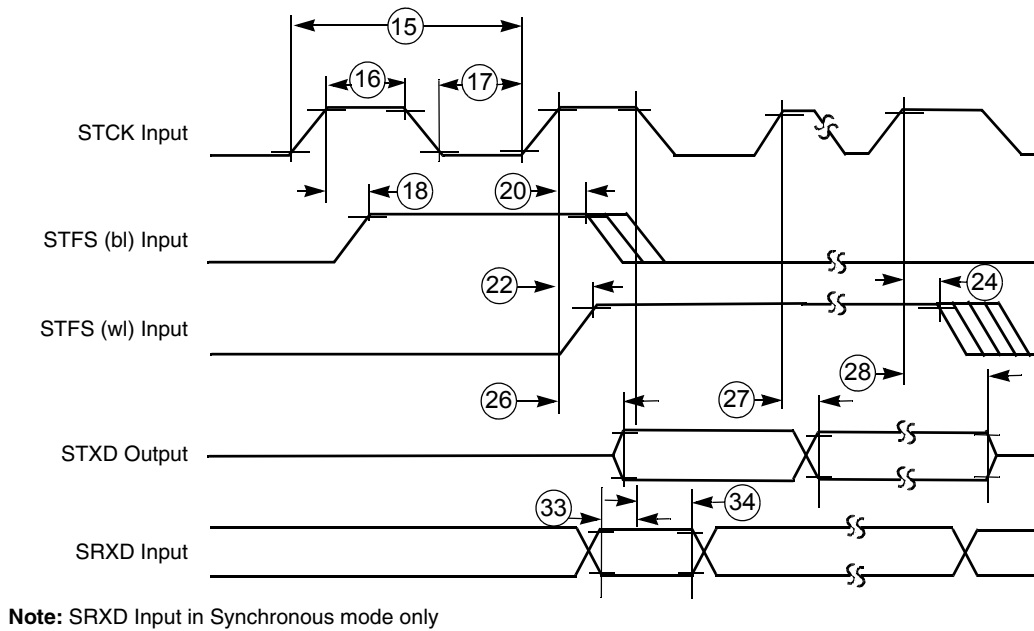


Figure 57. SSI Transmitter External Clock Timing Diagram

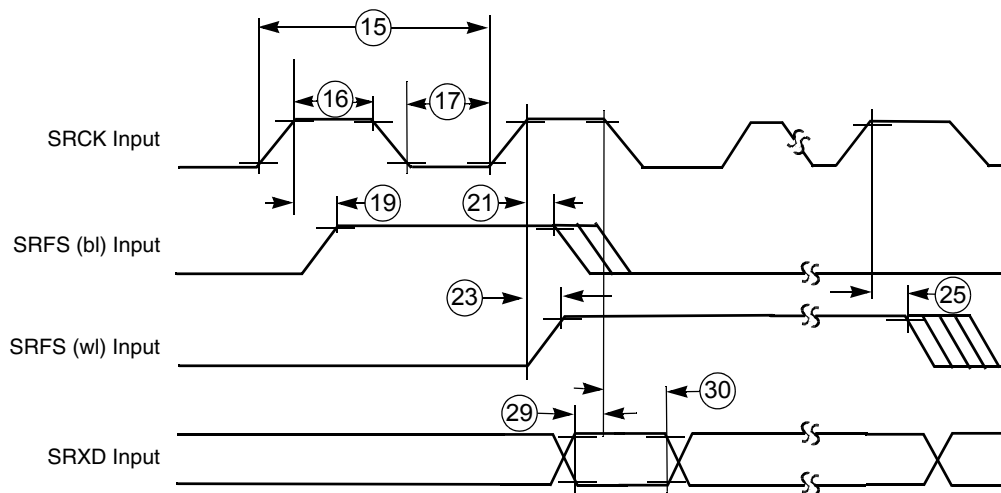


Figure 58. SSI Receiver External Clock Timing Diagram

Table 28. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation ¹ (Port C Primary Function ²)						
1	STCK/SRCK clock period ¹	95	—	83.3	—	ns
2	STCK high to STFS (bl) high ³	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high ³	-1.2	-1.7	-1.1	-1.5	ns

Table 28. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
4	STCK high to STFS (bl) low ³	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low ³	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high ³	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high ³	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low ³	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low ³	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	—	18.5	—	ns
14	SRXD hold time after SRCK low	0	—	0	—	ns
External Clock Operation (Port C Primary Function²)						
15	STCK/SRCK clock period ¹	92.8	—	81.4	—	ns
16	STCK/SRCK clock high period	27.1	—	40.7	—	ns
17	STCK/SRCK clock low period	61.1	—	40.7	—	ns
18	STCK high to STFS (bl) high ³	—	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	—	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	—	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	—	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	—	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	—	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	—	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	—	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns

Table 28. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	—	1.0	—	ns
30	SRXD hold time after SRCK low	0	—	0	—	ns
Synchronous Internal Clock Operation (Port C Primary Function²)						
31	SRXD setup before STCK falling	15.4	—	13.5	—	ns
32	SRXD hold after STCK falling	0	—	0	—	ns
Synchronous External Clock Operation (Port C Primary Function²)						
33	SRXD setup before STCK falling	1.14	—	1.0	—	ns
34	SRXD hold after STCK falling	0	—	0	—	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length.

Table 29. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation ¹ (Port B Alternate Function ²)						
1	STCK/SRCK clock period ¹	95	—	83.3	—	ns
2	STCK high to STFS (bl) high ³	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high ³	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low ³	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low ³	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high ³	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high ³	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low ³	3.08	5.24	2.7	4.6	ns

Table 29. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
9	SRCK high to SRFS (wl) low ³	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	—	17.5	—	ns
14	SRXD hold time after SRCK low	0	—	0	—	ns
External Clock Operation (Port B Alternate Function²)						
15	STCK/SRCK clock period ¹	92.8	—	81.4	—	ns
16	STCK/SRCK clock high period	27.1	—	40.7	—	ns
17	STCK/SRCK clock low period	61.1	—	40.7	—	ns
18	STCK high to STFS (bl) high ³	—	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	—	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	—	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	—	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	—	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	—	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	—	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	—	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns
28	STCK high to STXD high impedance	17.90	29.75	15.7	26.1	ns
29	SRXD setup time before SRCK low	1.14	—	1.0	—	ns
30	SRXD hold time after SRCK low	0	—	0	—	ns
Synchronous Internal Clock Operation (Port B Alternate Function²)						

Table 29. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8V \pm 0.10V		3.0V \pm 0.30V		Unit
		Minimum	Maximum	Minimum	Maximum	
31	SRXD setup before STCK falling	18.81	—	16.5	—	ns
32	SRXD hold after STCK falling	0	—	0	—	ns
Synchronous External Clock Operation (Port B Alternate Function²)						
33	SRXD setup before STCK falling	1.14	—	1.0	—	ns
34	SRXD hold after STCK falling	0	—	0	—	ns

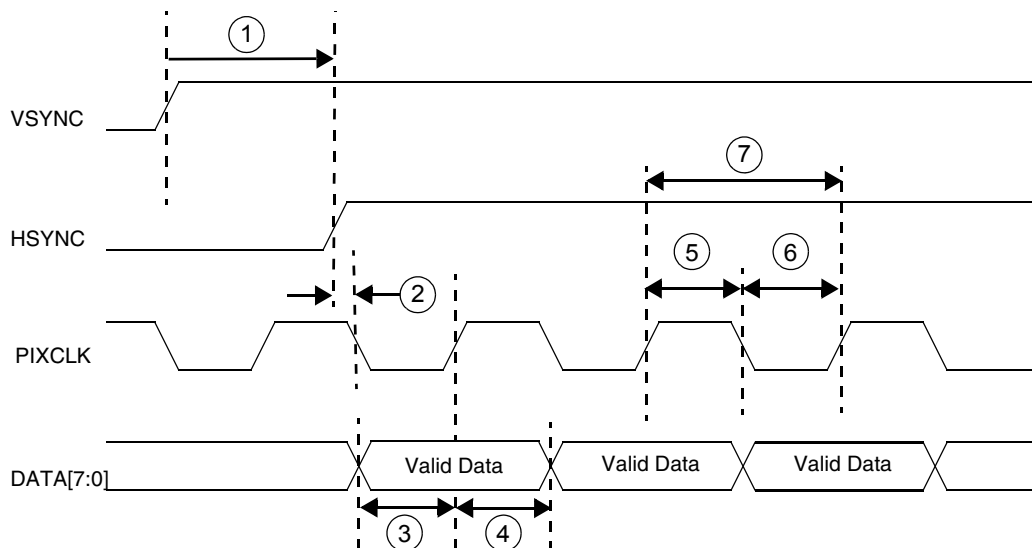
1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFISI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
2. There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.
3. bl = bit length; wl = word length.

3.18 CMOS Sensor Interface

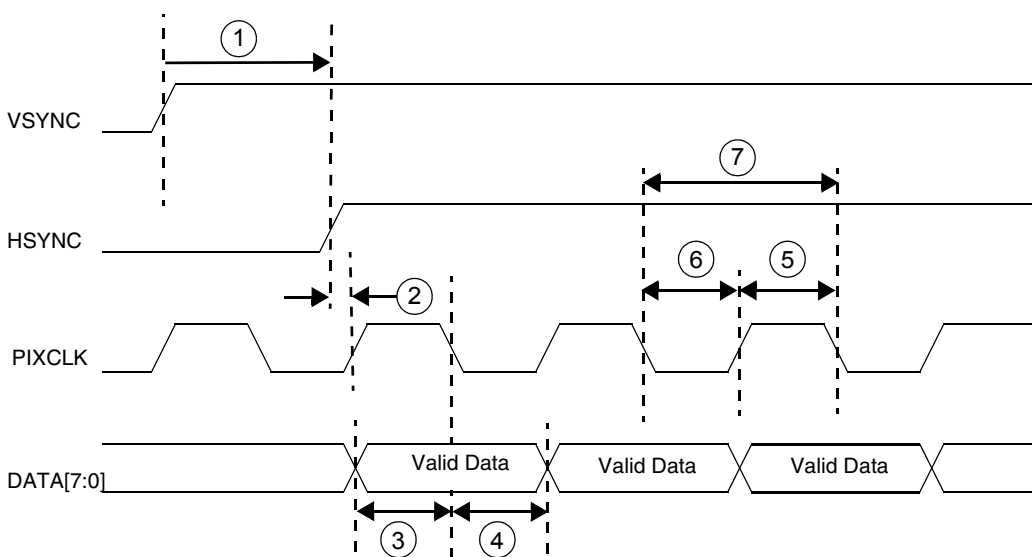
The CMOS Sensor Interface (CSI) module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32×32 image data receive FIFO, and a 16×32 statistic data FIFO.

3.18.1 Gated Clock Mode

Figure 59 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 60 on page 74 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 30 on page 75.



**Figure 59. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 60. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 30. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	-	ns
2	csi_hsync to csi_pixclk	1	-	ns
3	csi_d setup time	1	-	ns
4	csi_d hold time	1	-	ns
5	csi_pixclk high time	10.42	-	ns
6	csi_pixclk low time	10.42	-	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = $10 / 2 = 5\text{ns}$
 \Rightarrow max rise time allowed = $5 - 1 = 4\text{ns}$

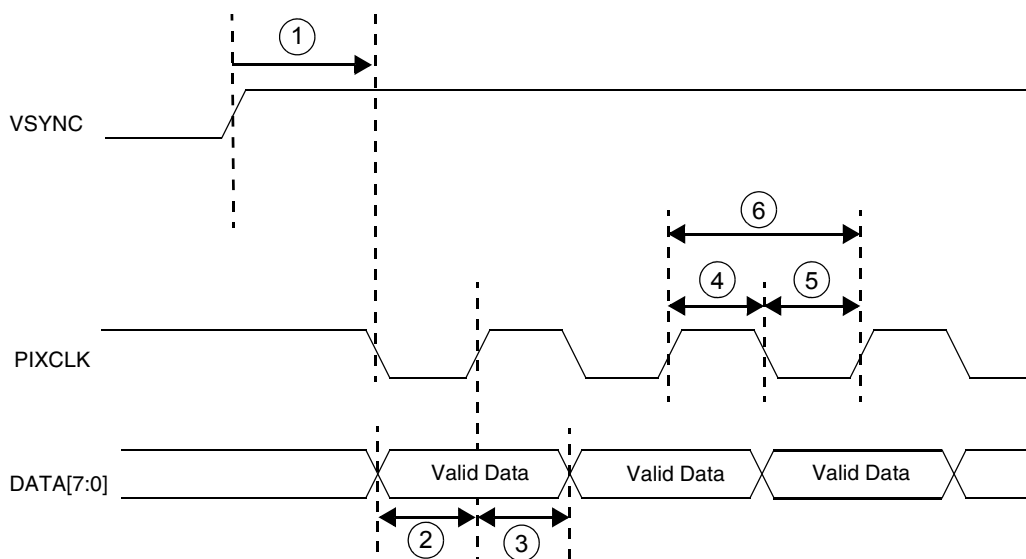
negative duty cycle = $10 / 2 = 5\text{ns}$
 \Rightarrow max fall time allowed = $5 - 1 = 4\text{ns}$

Falling-edge latch data

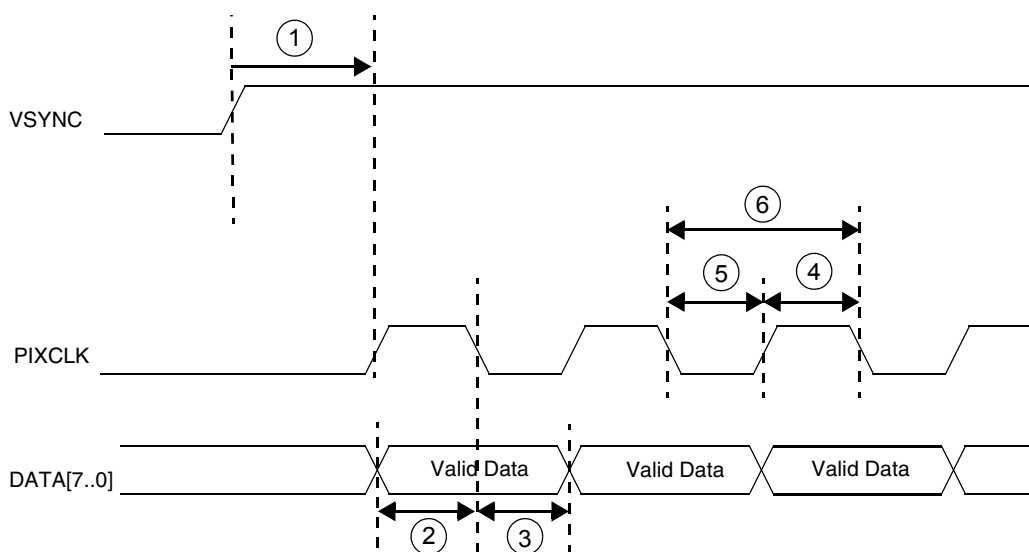
max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

3.18.2 Non-Gated Clock Mode

Figure 61 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 62 on page 76 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 31 on page 76.



**Figure 61. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 62. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 31. Non-Gated Clock Mode Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_pixclk	180	-	ns

Table 31. Non-Gated Clock Mode Parameters (Continued)

Ref No.	Parameter	Min	Max	Unit
2	csi_d setup time	1	-	ns
3	csi_d hold time	1	-	ns
4	csi_pixclk high time	10.42	-	ns
5	csi_pixclk low time	10.42	-	ns
6	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

$$\begin{aligned}\text{max rise time allowed} &= (\text{positive duty cycle} - \text{hold time}) \\ \text{max fall time allowed} &= (\text{negative duty cycle} - \text{setup time})\end{aligned}$$

In most of case, duty cycle is 50 / 50, therefore:

$$\begin{aligned}\text{max rise time} &= (\text{period} / 2 - \text{hold time}) \\ \text{max fall time} &= (\text{period} / 2 - \text{setup time})\end{aligned}$$

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

$$\begin{aligned}\text{positive duty cycle} &= 10 / 2 = 5\text{ns} \\ \Rightarrow \text{max rise time allowed} &= 5 - 1 = 4\text{ns}\end{aligned}$$

$$\begin{aligned}\text{negative duty cycle} &= 10 / 2 = 5\text{ns} \\ \Rightarrow \text{max fall time allowed} &= 5 - 1 = 4\text{ns}\end{aligned}$$

Falling-edge latch data

$$\begin{aligned}\text{max fall time allowed} &= (\text{negative duty cycle} - \text{hold time}) \\ \text{max rise time allowed} &= (\text{positive duty cycle} - \text{setup time})\end{aligned}$$

4 Pin-Out and Package Information

Table 32 illustrates the package pin assignments for the 256-pin MAPBGA package.

Table 32. MC9328MXL 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NVSS1	DAT3	CLK	NVSS4	USBD_AFE	NVDD4	NVSS3	UART1_RTS	UART1_RXD	NVDD3	N.C.	N.C.	QVDD4	N.C.	N.C.	N.C.
B	A24	DAT1	CMD	SSI1_RXDAT	USBD_ROE	USBD_VP	SSI0_RXCLK	SSI0_TXCLK	SPI1_SCLK	N.C.	N.C.	N.C.	QVSS4	N.C.	N.C.	N.C.
C	A23	D31	DAT0	SSI1_RXCLK	USBD_RCV	UART2_CTS	UART2_RXD	SSI0_RXFS	UART1_TXD	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
D	A22	D30	D29	SSI1_RXFS	USBD_SUSPND	USBD_VPO	USBD_VMO	SSI0_RXDAT	SPI1_SPI_RDY	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
E	A20	A21	D28	D26	DAT2	USBD_VM	UART2_RTS	SSI0_TXDAT	SPI1_SS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
F	A18	D27	D25	A19	A16	SSI1_TXFS	UART2_TXD	SSI0_TXFS	SPI1_MISO	N.C.	N.C.	REV	N.C.	N.C.	LSCLK	SPL_SPR
G	A15	A17	D24	D23	D21	SSI1_TXDAT	SSI1_TXCLK	UART1_CTS	SPI1_MOSI	N.C.	CLS	CONTRAST	OE_ACD	HSYNC	VSYNC	LD1
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS1	QVSS1	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS1	NVDD1	NVSS2	NVSS2	LD6	LD7	LD8	LD11	QVDD3	QVSS3
K	A10	D16	A9	D17	NVDD1	NVSS1	NVSS1	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TOUT2	LD15
L	A8	A7	D13	D15	D14	NVDD1	NVSS1	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3
M	A5	D12	D11	A6	SDCLK	NVSS1	RW	MA10	RAS	RESET_IN	BIG_ENDIAN	CSI_D4	CSI_HSYNC	CSI_VSYNC	CSI_D6	CSI_D5
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF	RESET_OUT	BOOT2	CSI_PIXCLK	CSI_D7	TMS	TDI
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_CLK	I2C_DATA	XTAL32K
R	EB2	EB3	A1	CS4	D8	D5	LB̄A	BCLK	D0	DQM0	SDCKE0	POR	BOOT1	TDO	QVDD2	EXTAL32K
T	NVSS1	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS2

Table 33 illustrates the package pin assignments for the 225-pin PBGA package.

Table 33. MC9328MXL 225 PBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	CMD	SSI1_RXCLK	SSI1_TXCLK	USBD_ROE	USBD_SUSPND	USBD_VM	SSI0_RXFS	SSI0_TXCLK	SPI1_RDY	SPI1_SCLK	REV	PS	LD2	LD4	LD5
B	DAT3	CLK	SSI1_RXDAT	USBD_AFE	USBD_RCV	USBD_VMO	SSI0_RXDAT	UART1_TXD	SPI1_SS	LSCLK	SPL_SPR	LD0	LD3	LD6	LD7
C	D31	DAT0	SSI1_RXFS	SSI1_TXFS	DAT2	USBD_VPO	UART2_RXD	SSI0_TXFS	UART1_RTS	CONTRAST	VSYNCR	LD8	LD9	LD12	NVDD2
D	A23	A24	DAT1	SSI1_TXDAT	NVDD1	USBD_VP	QVDD4	UART2_TXD	NVDD3	SPI1_MOSI	HSYNCR	LD1	LD11	TOUT2	LD13
E	A21	A22	D30	D29	NVDD1	QVSS	UART2_RTS	UART1_RXD	UART1_CTS	SPI1_MISO	OE_ACD	LD10	TIN	CSI_D0	CSI_MCLK
F	A20	A19	D28	D27	NVDD1	NVDD1	UART2_CTS	SSI0_RXCLK	SSI0_TXDAT	CLS	QVDD3	LD14	LD15	CSI_D2	CSI_D4
G	A17	A18	D26	D25	NVDD1	NVSS	NVDD4	NVSS	NVSS	QVSS	PWMO	CSI_D3	CSI_D7	CSI_HSYNCR	CSI_D5
H	A15	A16	D23	D24	D22	NVSS	NVSS	NVSS	NVSS	NVDD2	CSI_D1	CSI_VSYNCR	CSI_PIXCLK	I2C_DATA	TMS
J	A14	A12	D21	D20	NVDD1	NVSS	NVSS	QVDD1	NVSS	CSI_D6	I2C_CLK	TCK	TDO_B	BOOT1	BOOT0
K	A13	A11	CS2_B	D19	NVDD1	NVSS	QVSS	NVDD1	NVSS	D1	BOOT2	TDI	BIG_ENDIAN	RESET_OUT_B	XTAL32K
L	A10	A9	D17	D18	NVDD1	NVDD1	CS5_B	D2	ECB_B	NVSS	NVSS	POR	QVSS	XTAL16M	EXTAL32K
M	D16	D15	D13	D10	EB3_B	NVDD1	CS4_B	CS1_B	BCLK	RW_B	NVSS	BOOT3	QVDD2	RESET_IN_B	EXTAL16M
N	A8	A7	D12	EB0_B	D9	D8	CS3_B	CS0_B	PA17	D0	DQM2	DQM0	SDCKE0	TRISTATE	TRST_B
P	D14	A5	A4	A3	A2	A1	D6	D5	MA10	MA11	DQM1	RAS_B	SDCKE1	CLKO	RESETSF_B
R	A6	D11	EB1_B	EB2_B	OE_B	D7	A0	SDCLK	D4	LBA_B	D3	DQM3	CAS_B	SDWE_B	AVDD1

4.1 MAPBGA 256 Package Dimensions

Figure 63 illustrates the 256 MAPBGA 14 mm × 14 mm × 1.30 mm package, which has 0.8 mm spacing between the pads. The device designator for the MAPBGA package is VH.

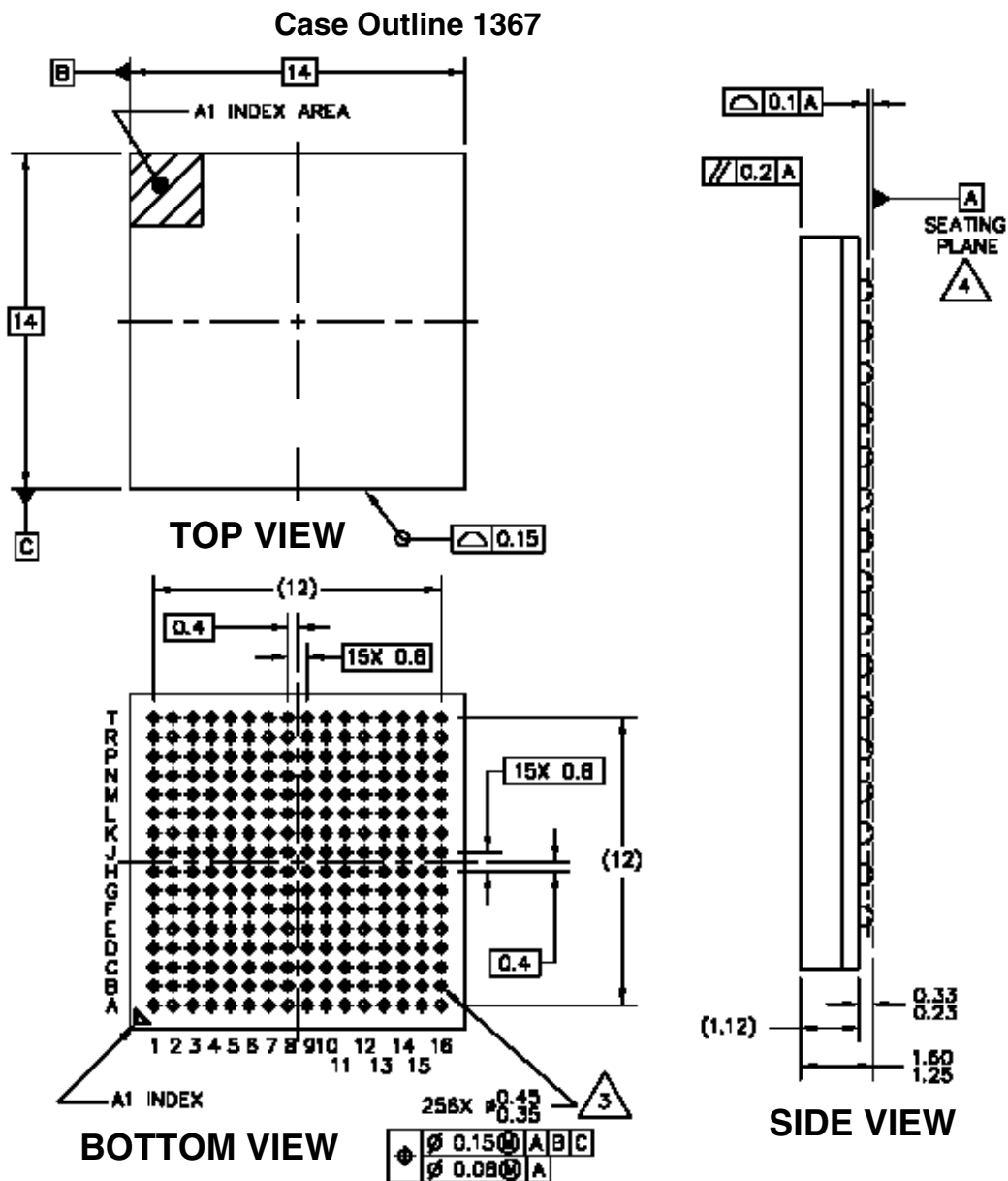
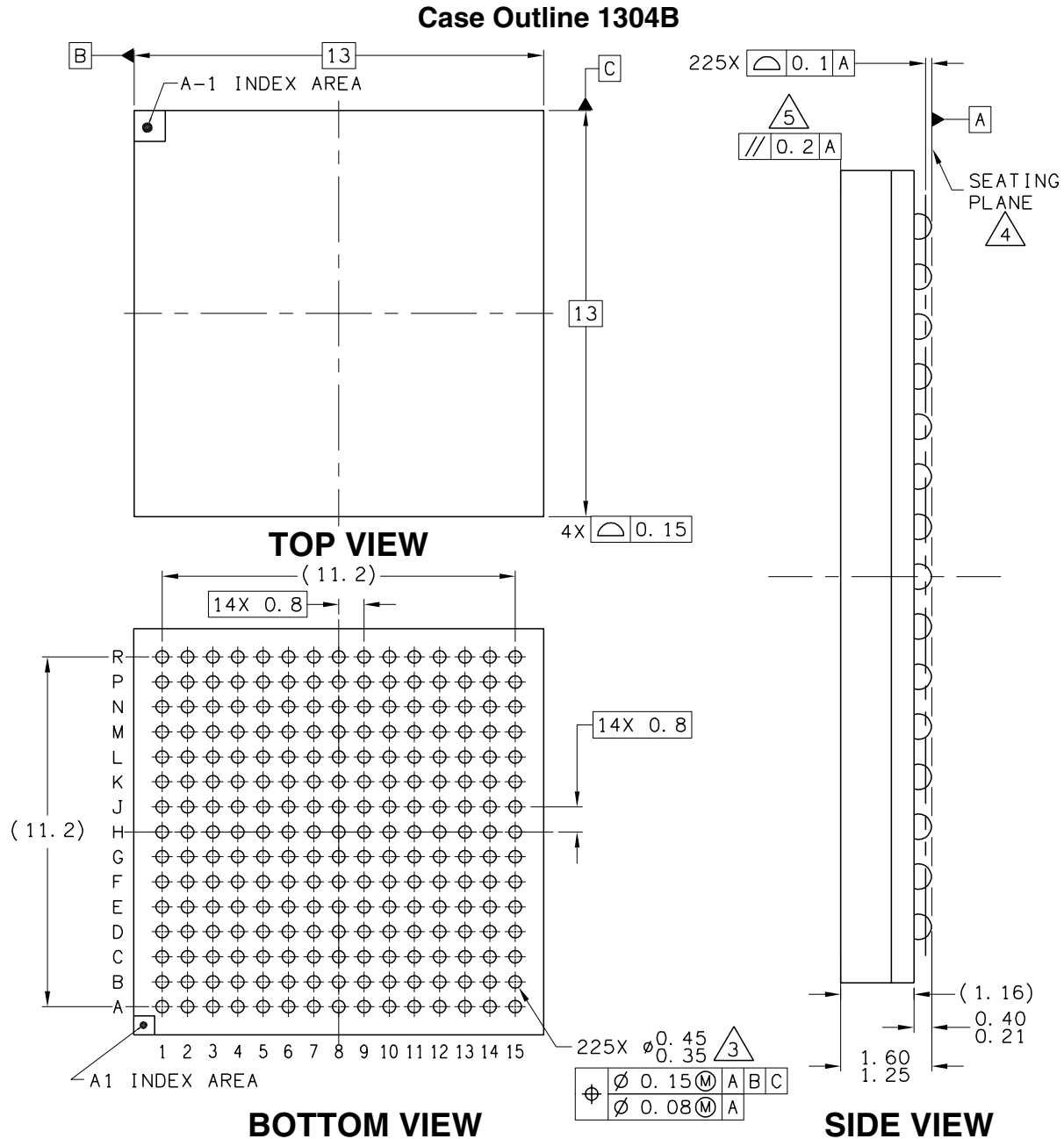


Figure 63. MC9328MXL 256 MAPBGA Mechanical Drawing

4.2 PBGA 225 Package Dimensions

Figure 64 illustrates the 225 PBGA 13 mm × 13 mm × 0.8 mm package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 64. MC9328MXL 225 PBGA Mechanical Drawing

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