



PSMN3R8-30LL

N-channel DFN3333-8 30 V 3.7 mΩ logic level MOSFET

Rev. 4 — 12 December 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in DFN3333-8 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources
- Small footprint for compact designs

1.3 Applications

- Battery protection
- DC-to-DC converters
- Load switching
- Power ORing

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 150 \text{ }^\circ\text{C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V};$ see Figure 2	-	-	40	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C};$ see Figure 1	-	-	69	W
T_j	junction temperature		-55	-	150	$^\circ\text{C}$
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	4.5	5.8	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	-	-	5.1	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	3	3.7	$\text{m}\Omega$

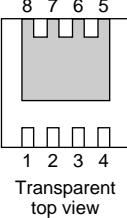
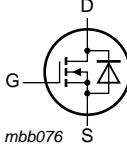


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 15$ A; $V_{DS} = 15$ V; see Figure 14 ; see Figure 15	-	5.3	-	nC
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5$ V; $I_D = 15$ A; $V_{DS} = 15$ V; see Figure 14 ; see Figure 15	-	38	-	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(\text{init})} = 25$ °C; $I_D = 40$ A; $V_{\text{sup}} \leq 30$ V; unclamped; $R_{GS} = 50$ Ω	-	-	109	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5,6,7,8	D	drain		
mb	D	mounting base; connected to drain		
SOT873-1 (DFN3333-8)				

3. Ordering information

Table 3. Ordering information

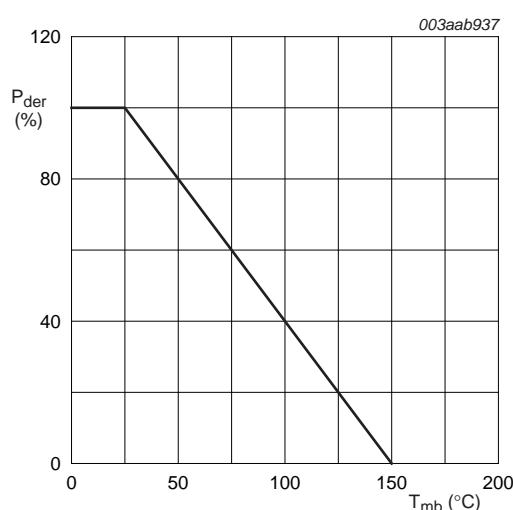
Type number	Package		Version
	Name	Description	
PSMN3R8-30LL	DFN3333-8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals	SOT873-1

4. Limiting values

Table 4. Limiting values

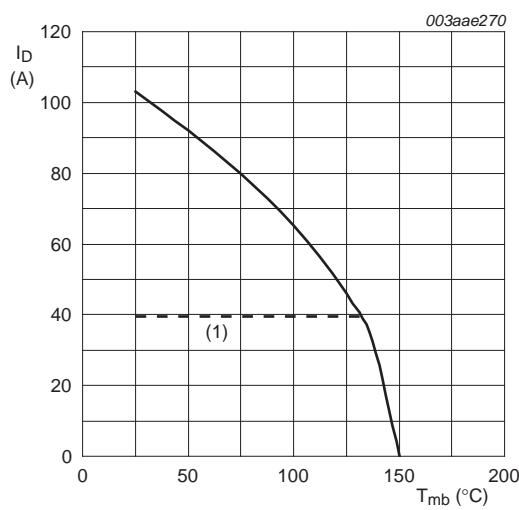
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_{mb} \leq 150^\circ\text{C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \leq 150^\circ\text{C}; T_{mb} \geq 25^\circ\text{C}; R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100^\circ\text{C}$; see Figure 2	-	40	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25^\circ\text{C}$; see Figure 2	-	40	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25^\circ\text{C}$; see Figure 3	-	413	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; see Figure 1	-	69	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25^\circ\text{C}$	-	40	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25^\circ\text{C}$	-	413	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25^\circ\text{C}; I_D = 40\text{ A}; V_{sup} \leq 30\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	109	mJ



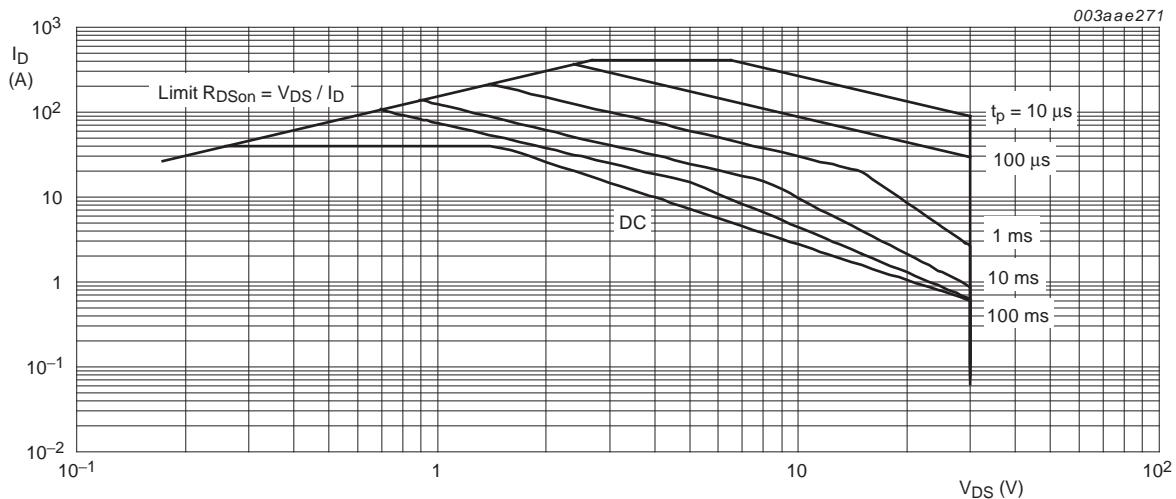
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 10\text{ V}; (1) \text{ Capped at } 40\text{ A due to package.}$

Fig 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25\text{ }^\circ\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1	1.3	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	[1]	-	53	60	K/W

[1] $R_{th(j\text{-}a)}$ is guaranteed by design and assumes that the device is mounted on a 40mm x 40mm x 70 μ m copper pad at 20°C ambient temperature. In practice $R_{th(j\text{-}a)}$ will be determined by the customer's PCB characteristics

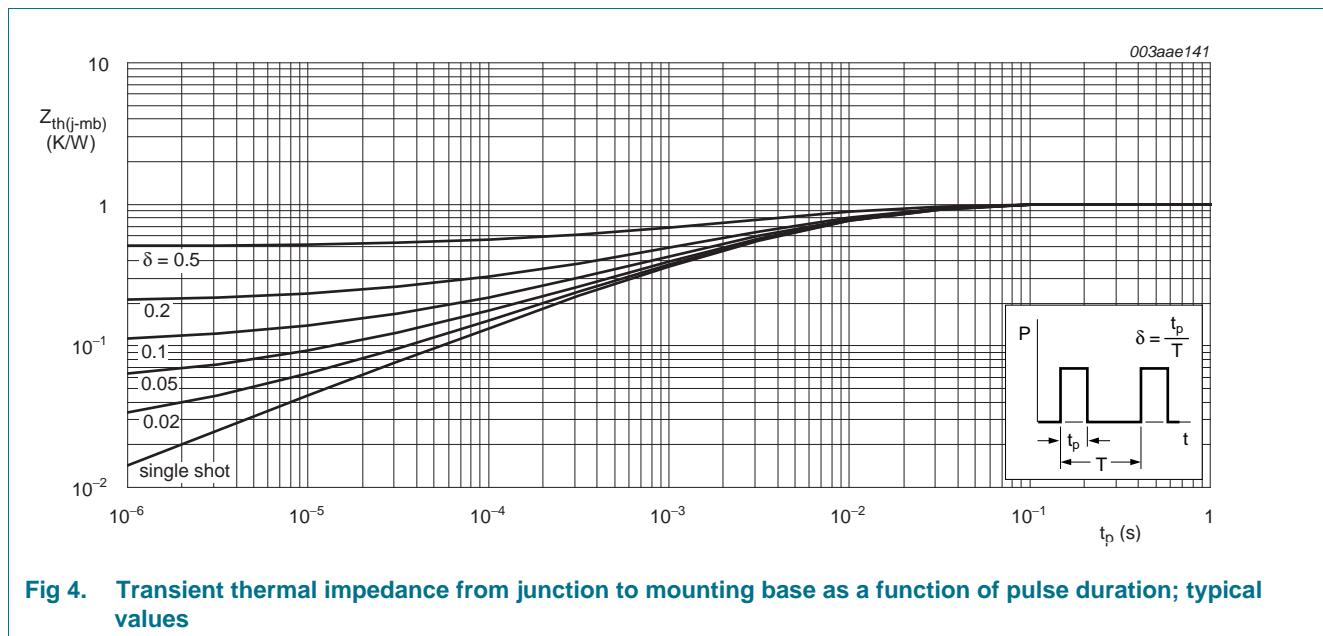


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

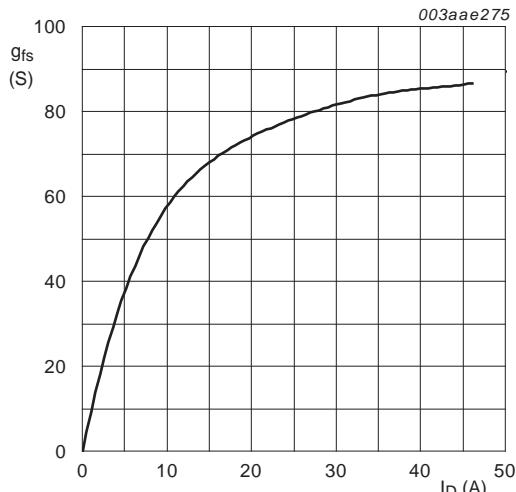
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 10 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 10 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	0.05	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12 $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12 $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	4.5	5.8	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 $I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 14 ; see Figure 15 $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	38	-	nC
Q_{GS}	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	6.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	3.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3	-	nC
Q_{GD}	gate-drain charge	$I_D = 15 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	5.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 15 \text{ V};$ see Figure 14 ; see Figure 15	-	2.8	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2085	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	396	-	pF
C_{rss}	reverse transfer capacitance		-	187	-	pF

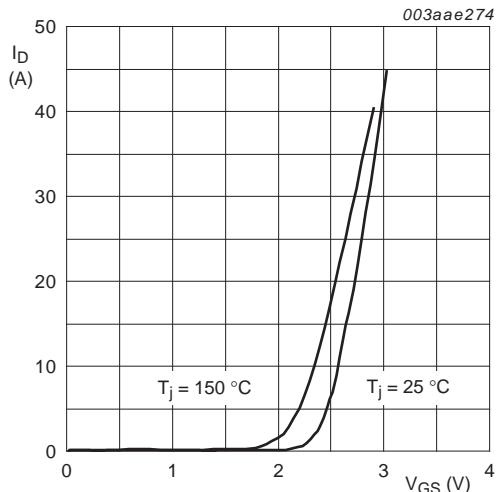
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 1 \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 4.7 \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	27	-	ns
t_r	rise time		-	67	-	ns
$t_{d(off)}$	turn-off delay time		-	39	-	ns
t_f	fall time		-	18	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 17	-	0.85	1.5	V
t_{rr}	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = 100 \text{ A}/\mu\text{s};$	-	36	-	ns
Q_r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	30	-	nC



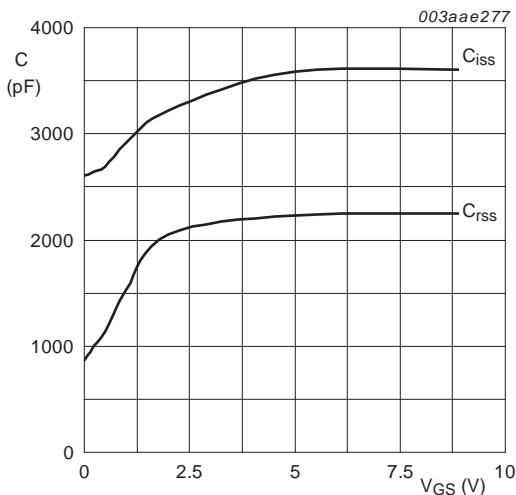
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 10 \text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



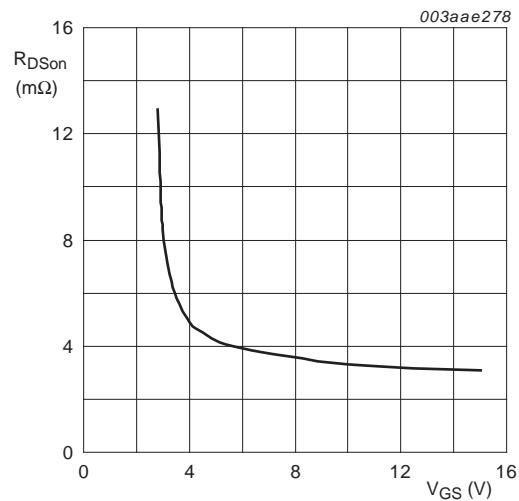
$V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



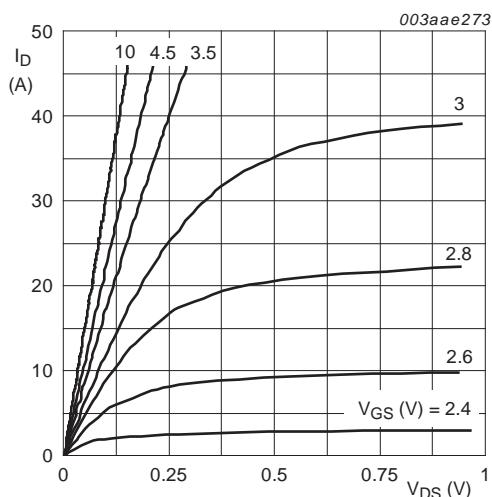
$V_{DS} = 0V; f = 1MHz$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



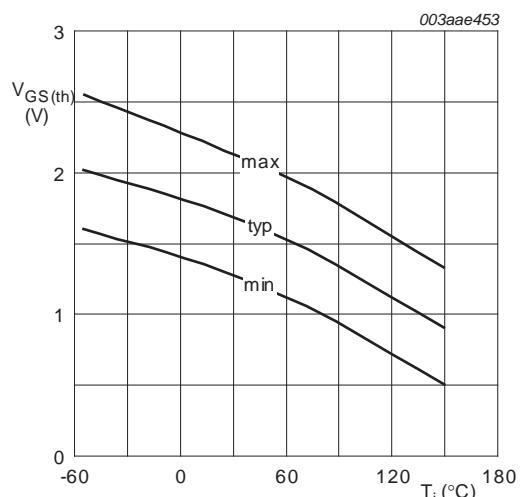
$T_j = 25^\circ C; I_D = 15A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



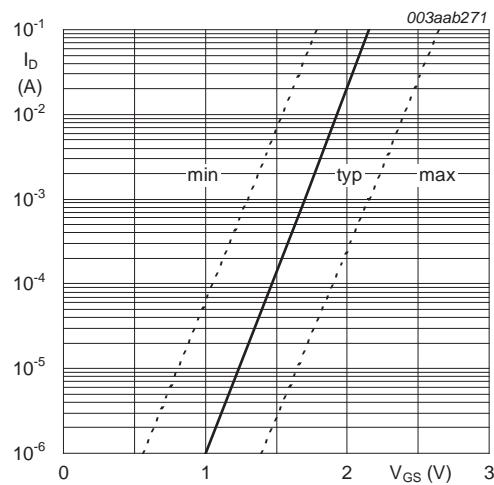
$T_j = 25^\circ C$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



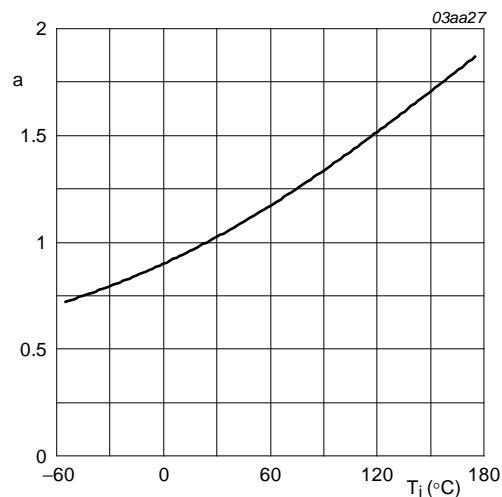
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



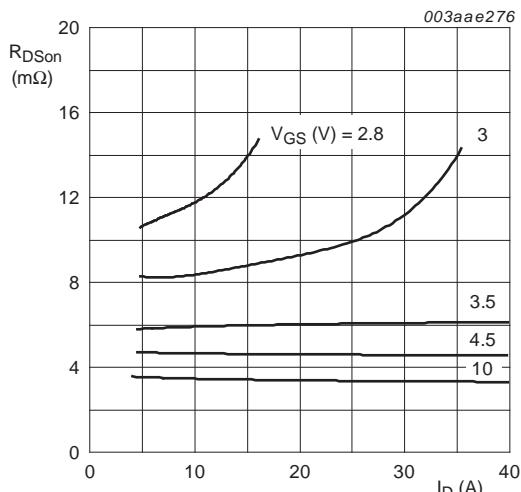
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

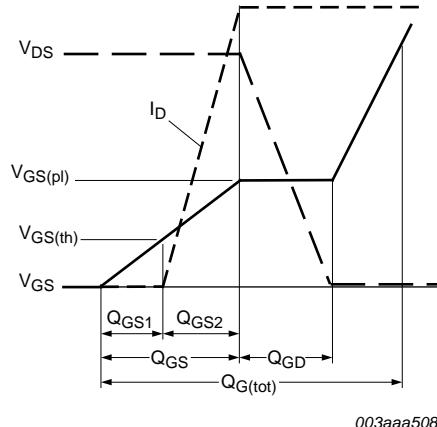
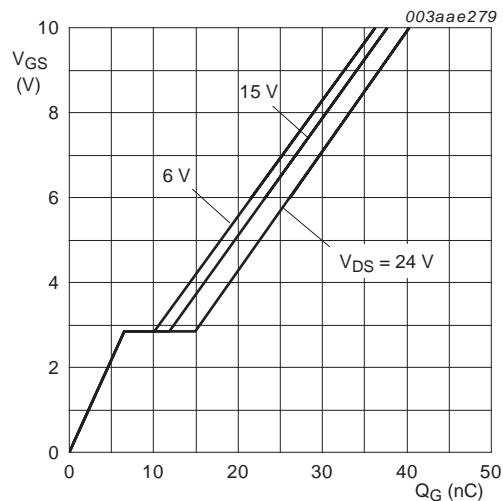
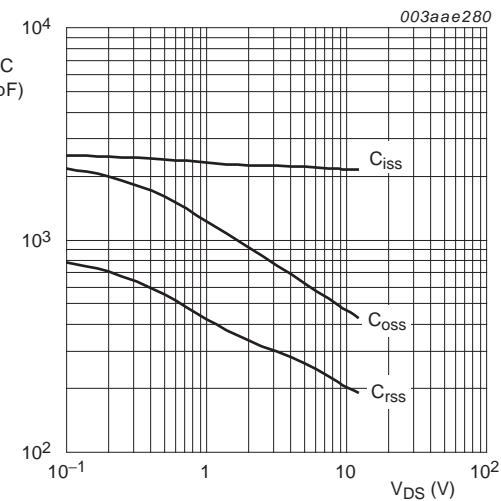


Fig 14. Gate charge waveform definitions



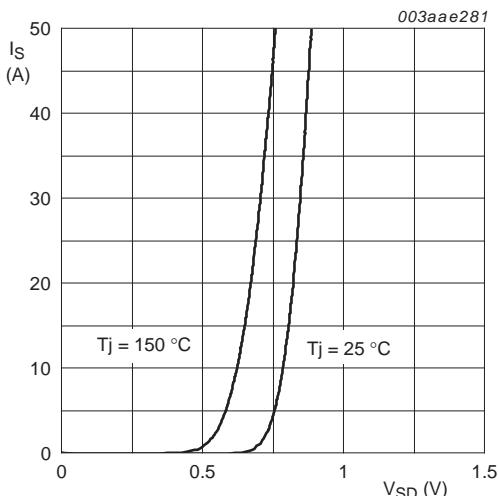
$T_j = 25^\circ\text{C}$; $I_D = 15\text{A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}$; $f = 1\text{MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

DFN3333-8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3.3 x 3.3 x 1.0 mm

SOT873-1

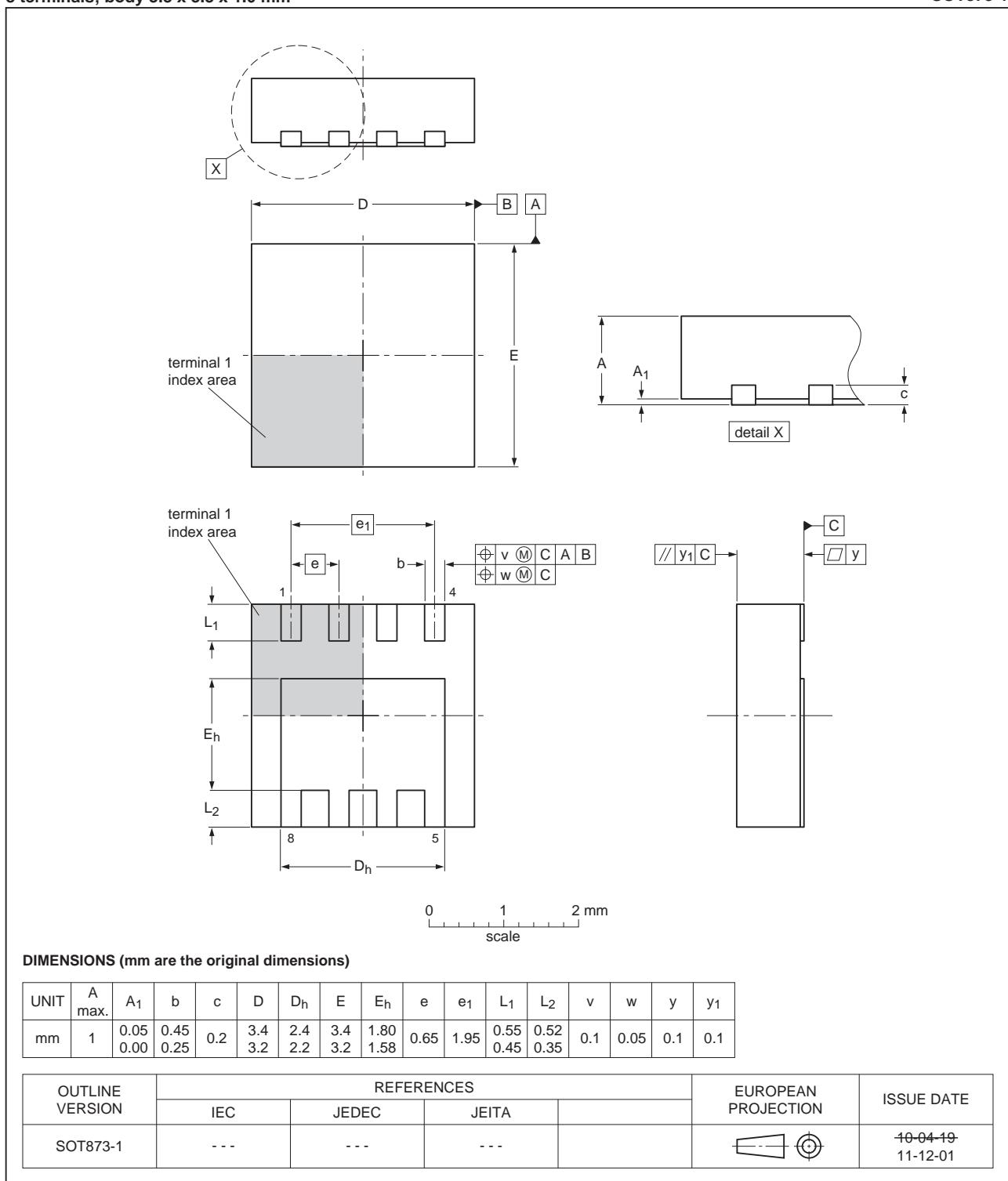


Fig 18. Package outline SOT873-1 (DFN3333-8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R8-30LL v.4	20111212	Product data sheet	-	PSMN3R8-30LL v.3
Modifications:		• Various changes to content.		
PSMN3R8-30LL v.3	20100818	Product data sheet	-	PSMN3R8-30LL v.2

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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