IS61(64)LF12832A IS64VF12832A
IS61(64)LF12836A IS61(64)VF12836A
IS61(64)LF25618A IS61(64)VF25618A

128K x 32, 128K x 36, 256K x 18
4 Mb SYNCHRONOUS FLOW-THROUGH STATIC RAM

JANUARY 2010

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply

  LF: V_{DD} 3.3V ± 5%, V_{DDQ} 3.3V/2.5V ± 5%

  VF: V_{DD} 2.5V -5% +10%, V_{DDQ} 2.5V -5% +10%
- JEDEC 100-Pin TQFP, 119-pin PBGA, and 165-pin PBGA packages
- Automotive temperature available
- Lead-free available

DESCRIPTION

The *ISSI* IS61(64)LF12832A, IS64VF12832A, IS61(64)LF/VF12836A and IS61(64)LF/VF25618A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61(64)LF12832A is organized as 131,072 words by 32 bits. The IS61(64)LF/VF12836A is organized as 131,072 words by 36 bits. The IS61(64)LF/VF25618A is organized as 262,144 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$) input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

Symbol	Parameter	-6.5	-7.5	Units
t_{KQ}	Clock Access Time	6.5	7.5	ns
t_{KC}	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

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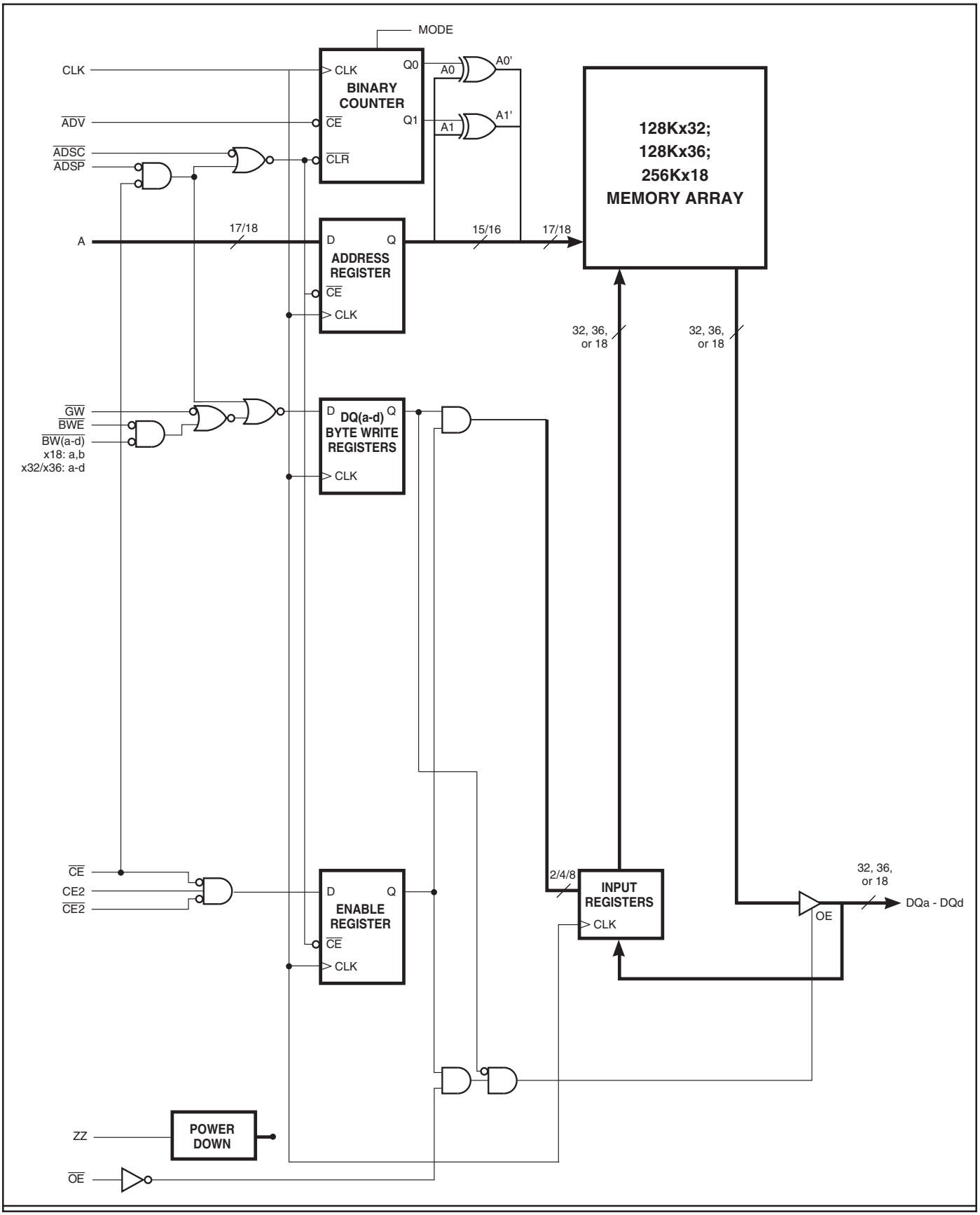
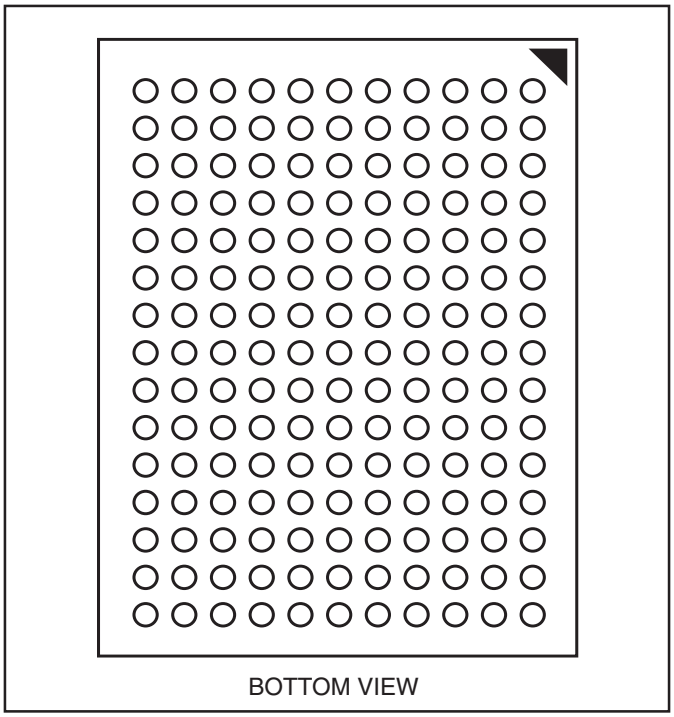
BLOCK DIAGRAM



165-PIN BGA

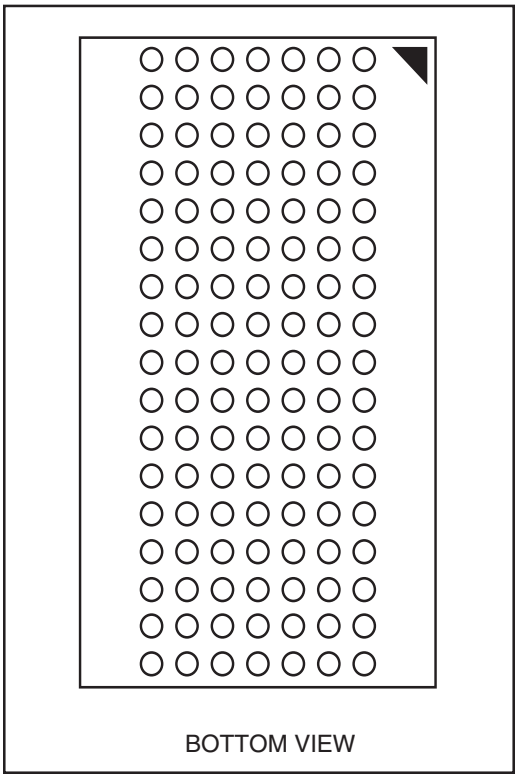
165-Ball, 13x15 mm BGA



BOTTOM VIEW

119-PIN BGA

119-Ball, 14x22 mm BGA



BOTTOM VIEW

119 BGA PACKAGE PIN CONFIGURATION

128K x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE2	A	$\overline{ADSC}$	A	$\overline{CE2}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	Vss	NC	Vss	DQPb	DQb
E	DQc	DQc	Vss	$\overline{CE}$	Vss	DQb	DQb
F	V_{DDQ}	DQc	Vss	$\overline{OE}$	Vss	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	Vss	$\overline{GW}$	Vss	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	Vss	$\overline{BWE}$	Vss	DQa	V_{DDQ}
N	DQd	DQd	Vss	A_1*	Vss	DQa	DQa
P	DQd	DQPd	Vss	A_0*	Vss	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Select
$\overline{BW}$x (x=a-d)	Synchronous Byte Write Controls
$\overline{BWE}$	Byte Write Enable

Symbol	Pin Name
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Output Power Supply
V_{DD}	Power Supply
V_{DDQ}	Output Power Supply
Vss	Ground

119 BGA PACKAGE PIN CONFIGURATION

256Kx18 (TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE2	A	$\overline{ADSC}$	A	$\overline{CE2}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	Vss	NC	Vss	DQPa	NC
E	NC	DQb	Vss	$\overline{CE}$	Vss	NC	DQa
F	V_{DDQ}	NC	Vss	$\overline{OE}$	Vss	DQa	V_{DDQ}
G	NC	DQb	$\overline{BWb}$	$\overline{ADV}$	Vss	NC	DQa
H	DQb	NC	Vss	$\overline{GW}$	Vss	DQa	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	Vss	CLK	Vss	NC	DQa
L	DQb	NC	Vss	NC	$\overline{BWa}$	DQa	NC
M	V_{DDQ}	DQb	Vss	$\overline{BWE}$	Vss	NC	V_{DDQ}
N	DQb	NC	Vss	A_1*	Vss	DQa	NC
P	NC	DQPb	Vss	A_0*	Vss	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Select
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Controls
$\overline{BWE}$	Byte Write Enable

Symbol	Pin Name
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Output Power Supply
V_{DD}	Power Supply
V_{DDQ}	Output Power Supply
Vss	Ground

165 PBGA PACKAGE PIN CONFIGURATION

128K x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQPc	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	Vss	NC	NC	NC	Vss	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	NC	A_1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A_0*	NC	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b,c,d)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Byte Write Enable
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground

165 PBGA PACKAGE PIN CONFIGURATION

256K x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	Vss	NC	NC	NC	Vss	V_{DDQ}	NC	NC
P	NC	NC	A	A	NC	A_1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A_0*	NC	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

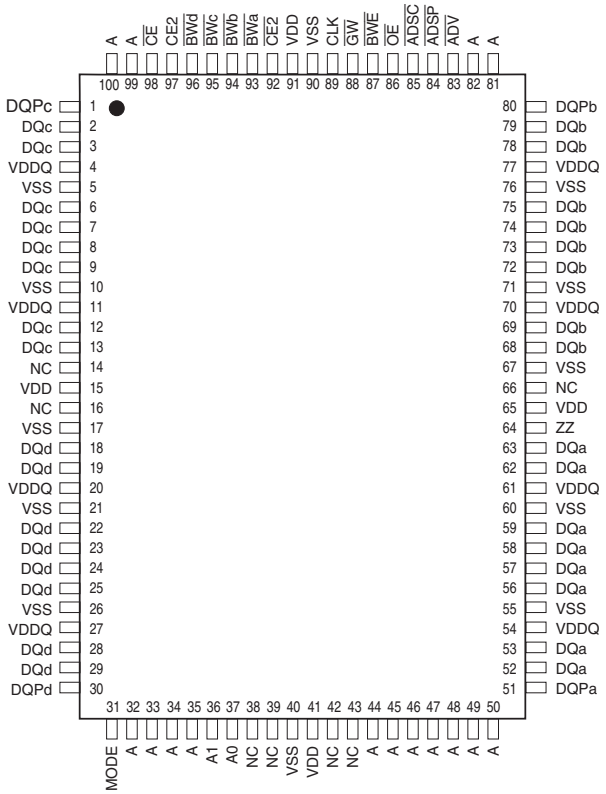
PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Byte Write Enable
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground

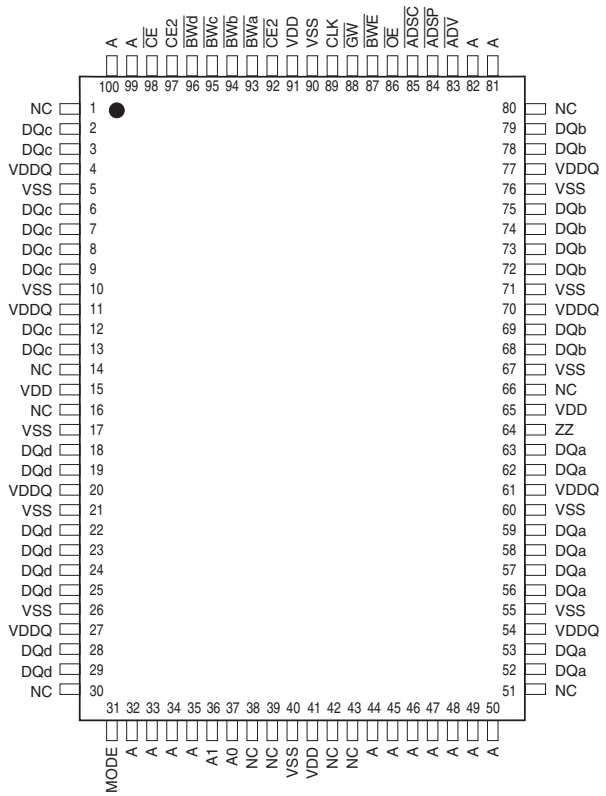
PIN CONFIGURATION

100-PIN TQFP (128K x 36)



(3 Chip-Enable option)

100-PIN TQFP (128K x 32)



(3 Chip-Enable option)

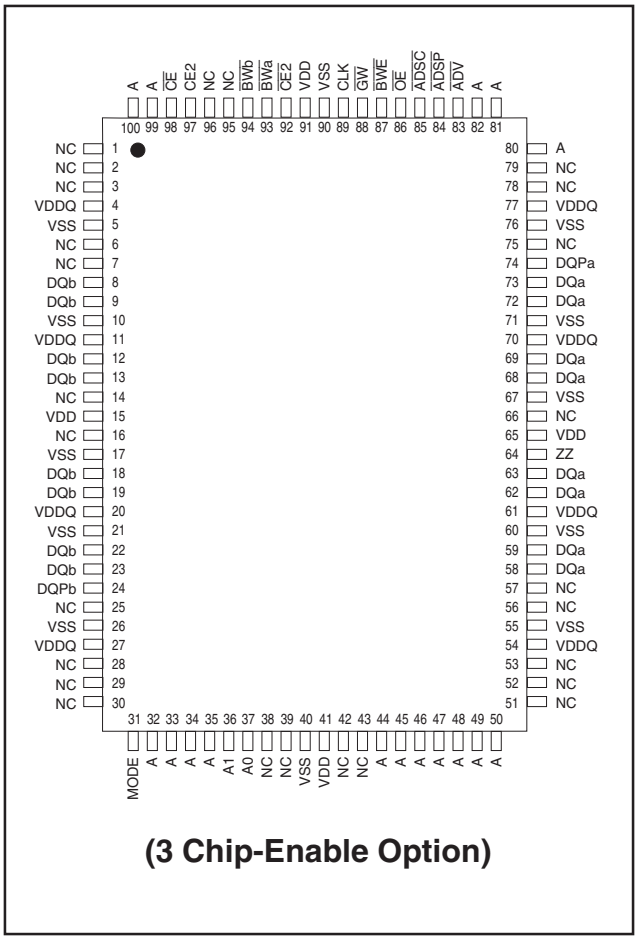
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWa}}$-$\overline{\text{BWd}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable
$\overline{\text{CE}}$, $\overline{\text{CE2}}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock

DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data Input/Output
$\overline{\text{GW}}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{\text{OE}}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable

PIN CONFIGURATION

100-PIN TQFP (256K x 18)



(3 Chip-Enable Option)

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWa}}$-$\overline{\text{BWb}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable
$\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Input/Output

DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
$\overline{\text{GW}}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{\text{OE}}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable

TRUTH TABLE[1-8]

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa-d}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

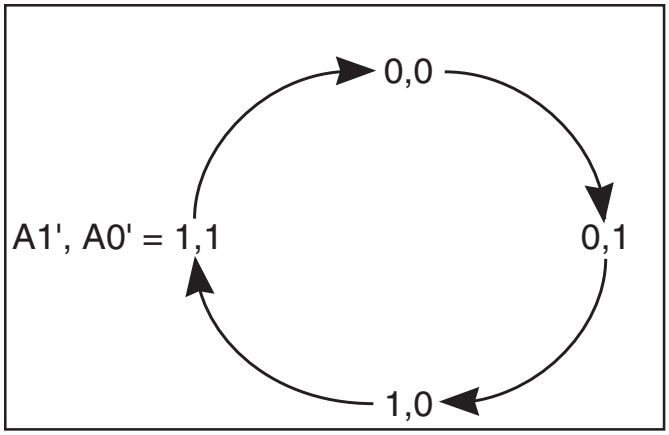
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = VSS)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ} + 0.5	V
V_{IN}	Voltage Relative to Vss for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61/64LFxxxxx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V/2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V/2.5V ± 5%
Automotive	-40°C to +125°C	3.3V ± 5%	3.3V/2.5V ± 5%

OPERATING RANGE (IS61/64VFxxxxx)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V -5% +10%	2.5V -5% +10%
Industrial	-40°C to +85°C	2.5V -5% +10%	2.5V -5% +10%
Automotive	-40°C to +125°C	2.5V -5% +10%	2.5V -5% +10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			3.3V		2.5V		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V)	2.4	—	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	–0.3	0.7	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$(1)	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE}$ = V_{IH}	–5	5	–5	5	µA

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	6.5 MAX x18	6.5 MAX x32/x36	7.5 MAX x18	7.5 MAX x32/x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com.	175	175	155	155	mA
			Ind.	180	180	160	160	
			Auto.	190	190	175	175	
			typ.[2]	120		110		
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com.	90	90	90	90	mA
			Ind.	100	100	100	100	
			Auto.	120	120	120	120	
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., V_{IN} ≤ V_{SS} + 0.2V or ≥V_{DD} – 0.2V	Com.	70	70	70	70	mA
			Ind.	75	75	75	75	
			Auto.	90	90	90	90	
		f = 0	typ.	40		40		
I_{SB2}	Sleep Mode	ZZ>V_{IH}	Com.	30	30	30	30	mA
			Ind.	35	35	35	35	
			Auto.	45	45	45	45	
			typ.	25		25		

Note:
1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100 µA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

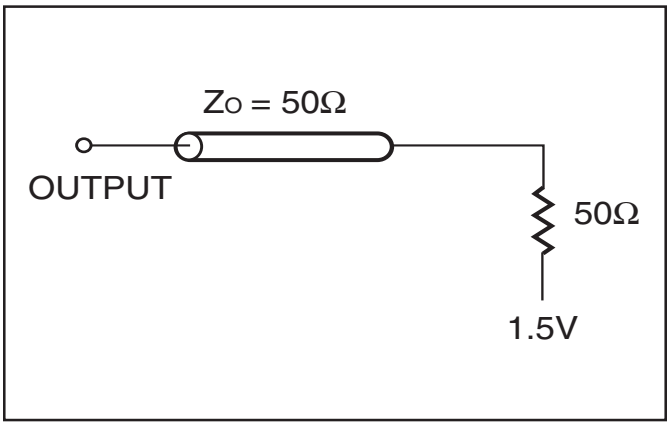


Figure 1

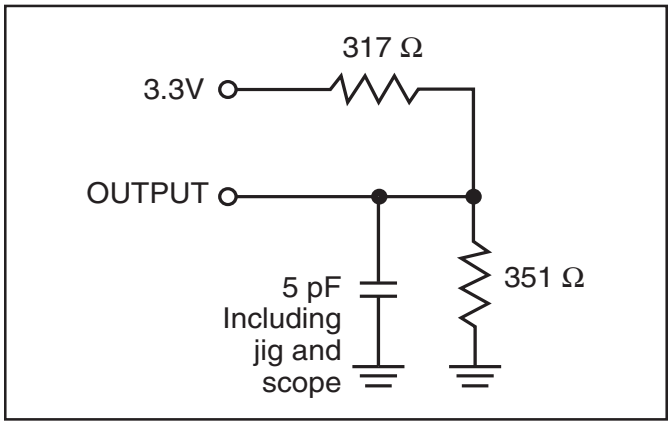


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

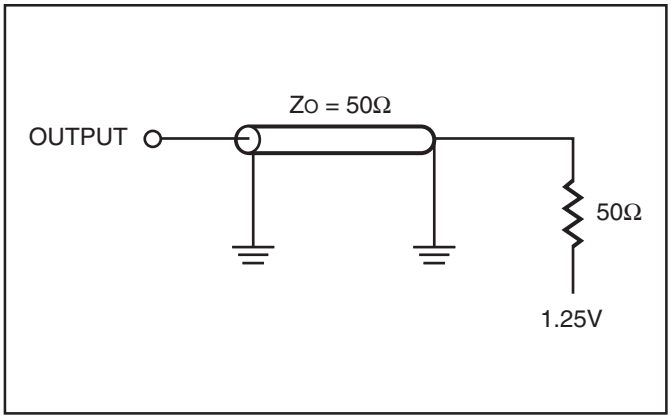


Figure 3

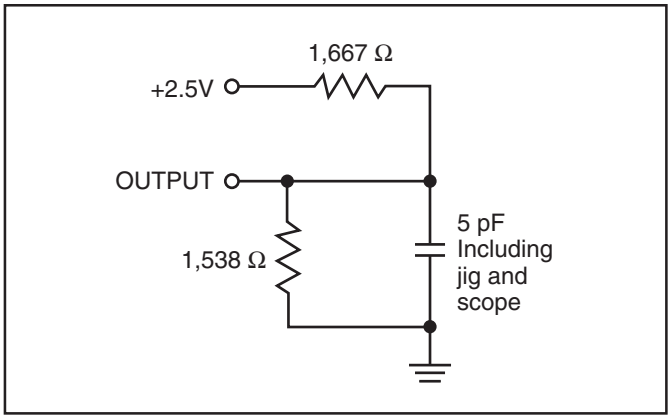


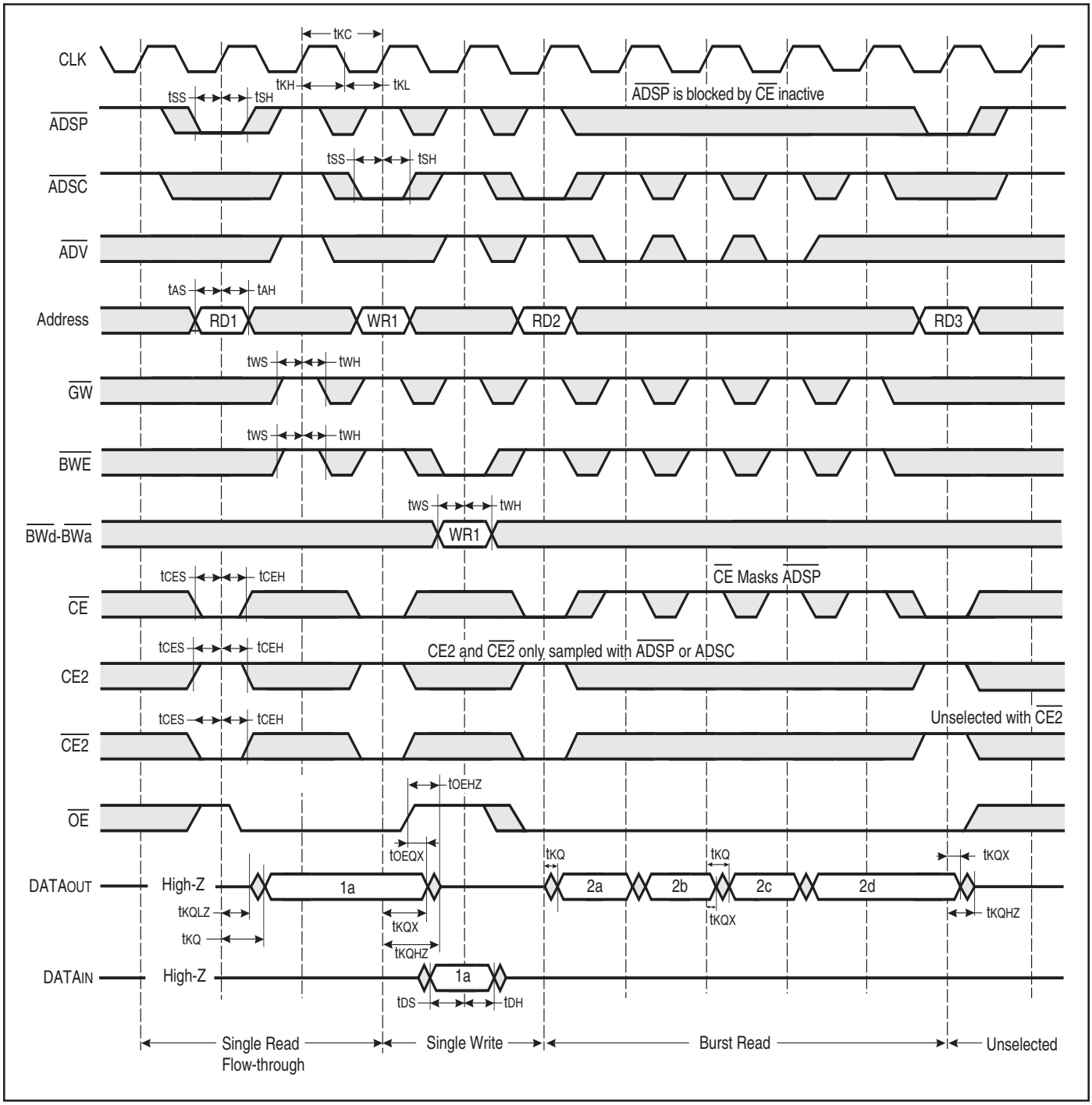
Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

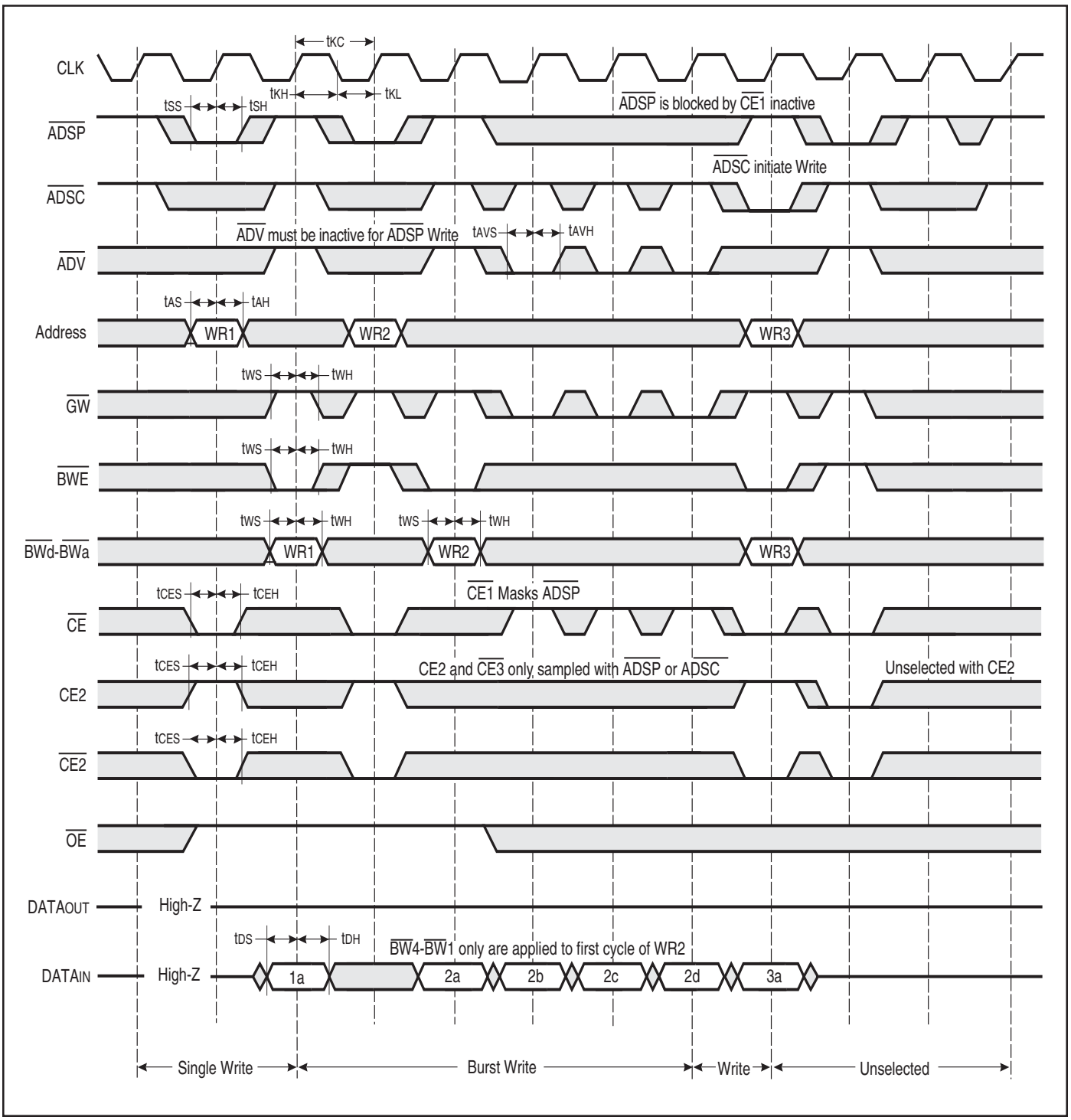
Symbol	Parameter	6.5 Min.	6.5 Max.	7.5 Min.	7.5 Max.	Unit
fmax	Clock Frequency	—	133	—	117	MHz
t_{KC}	Cycle Time	7.5	—	8.5	—	ns
t_{KH}	Clock High Time	2.2	—	2.5	—	ns
t_{KL}	Clock Low Time	2.2	—	2.5	—	ns
t_{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t_{KQX}[2]	Clock High to Output Invalid	2.5	—	2.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	2.5	—	2.5	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	3.8	—	4.0	ns
t_{OEQ}	Output Enable to Output Valid	—	3.2	—	3.4	ns
t_{OEQX}[2]	Output Enable to Output Invalid	2.5	—	2.5	—	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	3.5	—	3.5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{DS}	Data Setup Time	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



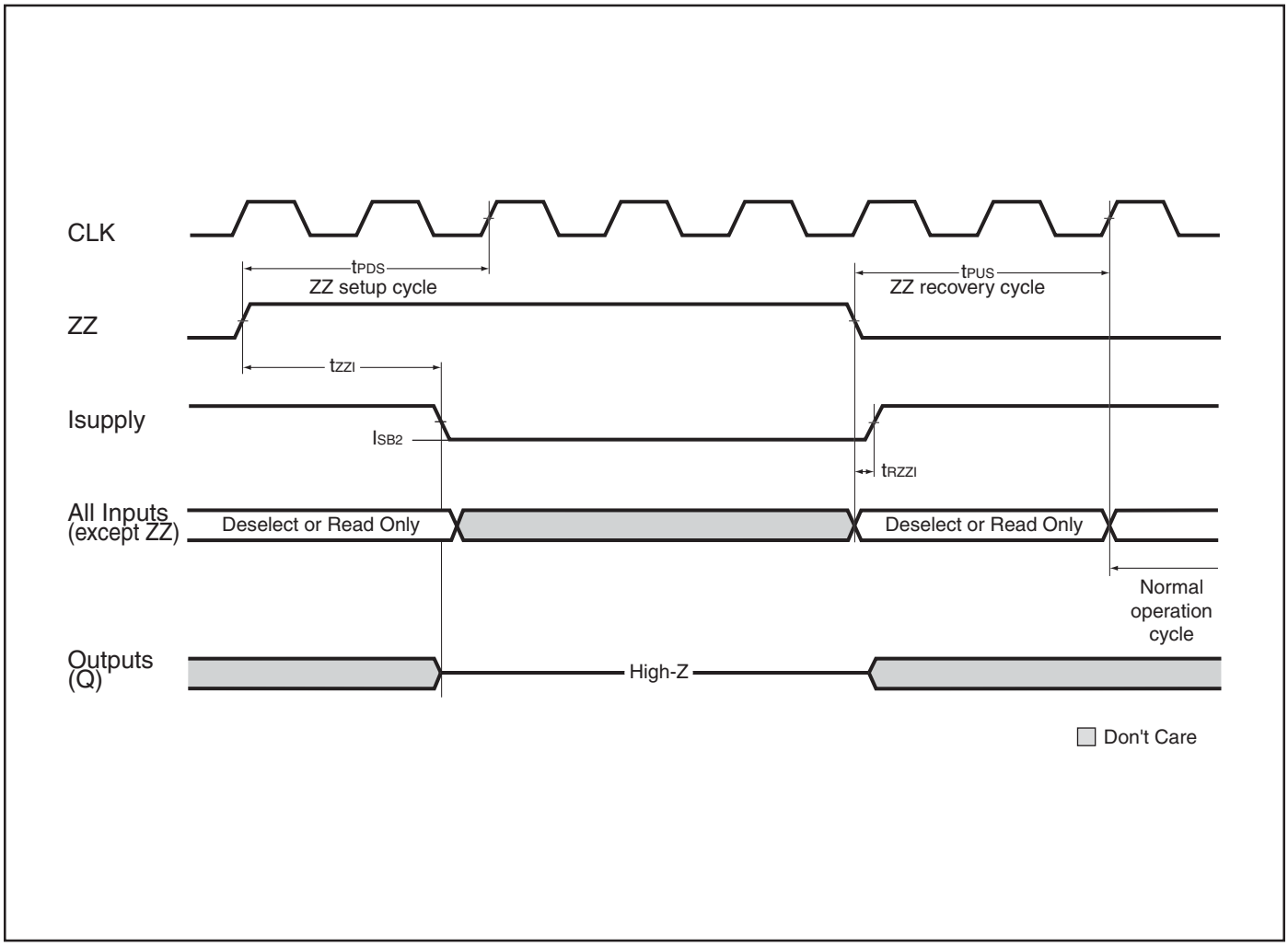
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ Vih	—	60	mA
t_{PDS}	ZZ active to input ignored		—	2	cycle
t_{PUS}	ZZ inactive to input sampled		2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0	—	ns

SNOOZE MODE TIMING



ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)

Commercial Range: 0°C to +70°C

Configuration	Access Time	Order Part Number	Package
128Kx32	6.5	IS61LF12832A-6.5TQ	100 TQFP
		IS61LF12832A-6.5B2	119 PBGA
		IS61LF12832A-6.5B3	165 PBGA
128Kx32	7.5	IS61LF12832A-7.5TQ	100 TQFP
		IS61LF12832A-7.5B2	119 PBGA
		IS61LF12832A-7.5B3	165 PBGA
128Kx36	6.5	IS61LF12836A-6.5TQ	100 TQFP
		IS61LF12836A-6.5B2	119 PBGA
		IS61LF12836A-6.5B3	165 PBGA
128Kx36	7.5	IS61LF12836A-7.5TQ	100 TQFP
		IS61LF12836A-7.5B2	119 PBGA
		IS61LF12836A-7.5B3	165 PBGA
256Kx18	6.5	IS61LF25618A-6.5TQ	100 TQFP
		IS61LF25618A-6.5TQL	100 TQFP, Lead-free
		IS61LF25618A-6.5B2	119 PBGA
		IS61LF25618A-6.5B3	165 PBGA
256Kx18	7.5	IS61LF25618A-7.5TQ	100 TQFP
		IS61LF25618A-7.5B2	119 PBGA
		IS61LF25618A-7.5B3	165 PBGA

ORDERING INFORMATION (V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V)

Industrial Range: -40°C to +85°C

Configuration	Access Time	Order Part Number	Package
128Kx32	6.5	IS61LF12832A-6.5TQI	100 TQFP
		IS61LF12832A-6.5B2I	119 PBGA
		IS61LF12832A-6.5B3I	165 PBGA
128Kx32	7.5	IS61LF12832A-7.5TQI	100 TQFP
		IS61LF12832A-7.5TQLI	100 TQFP, Lead-free
		IS61LF12832A-7.5B2I	119 PBGA
		IS61LF12832A-7.5B3I	165 PBGA
128Kx36	6.5	IS61LF12836A-6.5TQI	100 TQFP
		IS61LF12836A-6.5TQLI	100 TQFP, Lead-free
		IS61LF12836A-6.5B2I	119 PBGA
		IS61LF12836A-6.5B3I	165 PBGA
128Kx36	7.5	IS61LF12836A-7.5TQI	100 TQFP
		IS61LF12836A-7.5TQLI	100 TQFP, Lead-free
		IS61LF12836A-7.5B2I	119 PBGA
		IS61LF12836A-7.5B3I	165 PBGA
256Kx18	6.5	IS61LF25618A-6.5TQI	100 TQFP
		IS61LF25618A-6.5B2I	119 PBGA
		IS61LF25618A-6.5B3I	165 PBGA
256Kx18	7.5	IS61LF25618A-7.5TQI	100 TQFP
		IS61LF25618A-7.5TQLI	100 TQFP, Lead-free
		IS61LF25618A-7.5B2I	119 PBGA
		IS61LF25618A-7.5B3I	165 PBGA

Automotive Range: -40°C to +125°C

Configuration	Access Time	Order Part Number	Package
128Kx32	7.5	IS64LF12832A-7.5TQA3	100 TQFP
		IS64LF12832A-7.5TQLA3	100 TQFP, Lead-free
128Kx36	7.5	IS64LF12836A-7.5TQA3	100 TQFP
256Kx18	7.5	IS64LF25618A-7.5TQA3	100 TQFP

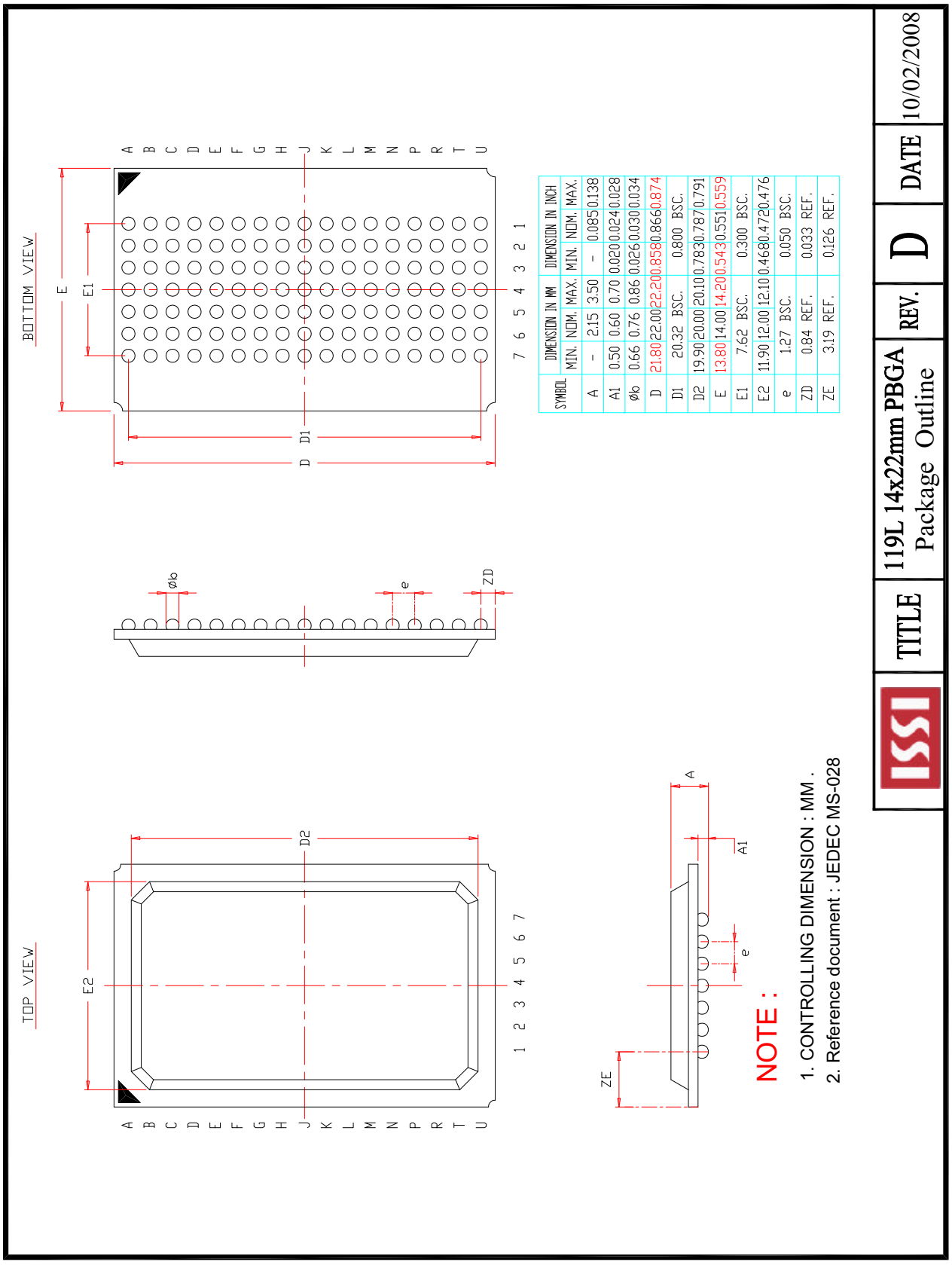
ORDERING INFORMATION (V_{DD} = 2.5V /V_{DDQ} = 2.5V)

Commercial Range: 0°C to +70°C

Configuration	Access Time	Order Part Number	Package
128Kx36	6.5	IS61VF12836A-6.5TQ	100 TQFP
		IS61VF12836A-6.5B2	119 PBGA
		IS61VF12836A-6.5B3	165 PBGA
128Kx36	7.5	IS61VF12836A-7.5TQ	100 TQFP
		IS61VF12836A-7.5B2	119 PBGA
		IS61VF12836A-7.5B3	165 PBGA
256Kx18	6.5	IS61VF25618A-6.5TQ	100 TQFP
		IS61VF25618A-6.5B2	119 PBGA
		IS61VF25618A-6.5B3	165 PBGA
256Kx18	7.5	IS61VF25618A-7.5TQ	100 TQFP
		IS61VF25618A-7.5B2	119 PBGA
		IS61VF25618A-7.5B3	165 PBGA

Industrial Range: -40°C to +85°C

Configuration	Access Time	Order Part Number	Package
128Kx36	6.5	IS61VF12836A-6.5TQI	100 TQFP
		IS61VF12836A-6.5B2I	119 PBGA

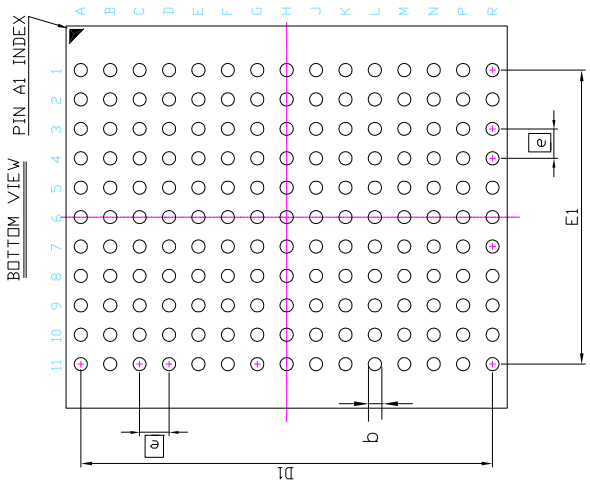


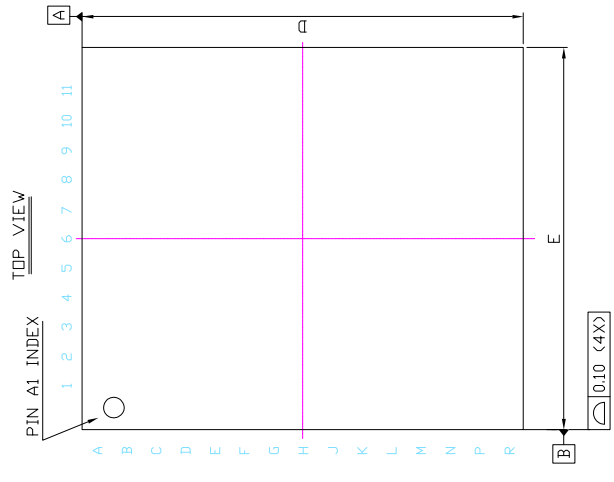
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	2.15	3.50	–	0.085	0.138
A1	0.50	0.60	0.70	0.020	0.024	0.028
øb	0.66	0.76	0.86	0.026	0.030	0.034
D	21.80	22.00	22.20	0.858	0.866	0.874
D1		20.32	BSC.		0.800	BSC.
D2	19.90	20.00	20.10	0.783	0.787	0.791
E	13.80	14.00	14.20	0.543	0.551	0.559
E1		7.62	BSC.		0.300	BSC.
E2	11.90	12.00	12.10	0.468	0.472	0.476
e		1.27	BSC.		0.050	BSC.
ZD		0.84	REF.		0.033	REF.
ZE		3.19	REF.		0.126	REF.

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.35	0.40	0.010	0.014	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .





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