Texas Instruments

THS4226EVM

User's Guide

May 2003

High Performance Linear Products

SLOU157

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4 V (differential) and ±7.5 V (Vs–, Vs+) when using a dual-supply power source—maximum 15 V when using a single-supply power source (Vs).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C. The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to <u>you</u>.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4226 data sheet (SLOS399)
- Application report (SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits,* http://www–s.ti.com/sc/psheets/sloa069/sloa069.pdf
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, http://www–s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (SLMA004), PowerPAD Made Easy, http://www–s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (SSYA008), Electrostatic Discharge (ESD), http://www–s.ti.com/sc/psheets/ssya008/ssya008.pdf
- High-Speed Amplifier PCB Layout Tips, http://www–s.ti.com/sc/psheets/sloa102/sloa102.pdf

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Chapter 1

Introduction and Description

This EVM provides a platform for testing the THS4226 in the 10-pin MSOP (DGQ) package. It contains the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations.

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for the default schematic diagram. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The EVM includes the following features:

- Wide operating supply voltage range: dual supply ±1.35 V to dual supply ±7.5 V operation (see the device data sheet). Single supply operation is obtained by connecting both J8 (GND) and J7 (VS–) to ground. Operating supply voltage range for single supply is 2.7 V to 15 V.
- Convenient GND test point (TP1)
- Power supply ripple rejection provided by inductors FB1 and FB2 followed by tantalum capacitors C5 and C6
- Decoupling capacitors, C7 and C8, populated with 0.1 µF and capacitors, C3 and C4, populated with 100 pF—design final decoupling in accordance with SLOA069
- Nominal 50-Ω input impedance for each of the configured inputs, V1in–, V1in+ and V2in+. Termination can be configured according to the application requirement.
- A good example of high-speed amplifier PCB design and layout. Also see High-Speed Amplifier PCB Layout Tips, SLOA102.
- 50-Ω input matching resistors (R3 and R10)
- 453-Ω resistors along with the 49.9-Ω resistors to ground provide minimum load of 500 Ω on EVM channel 1 and channel 2 respectively.
- User customizable / configurable component choice
- Nominal 50-Ω signal traces for input and outputs to reduce signal reflections within this board

- Power PAD™ heatsinking capability

EVM Channel 1:

The default configuration design for EVM channel 1 provides a voltage gain of +2. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 1) to the voltage at the J3 input. R1 and R6 are equal and therefore provide for a gain of +2.

The noninverting gain of the EVM channel 1 amplifier, when using the default configuration, is affected by a voltage divider composed of R5 and R4. When using a 50-Ω signal source and 50-Ω measurement device, its voltage gain (from J3 to J1) is indicated in the following equation.

$$\frac{V_O}{V_I} = \left(1 + \frac{R6}{R1 + R2}\right)\left(\frac{R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = 0.456 \qquad (1)$$

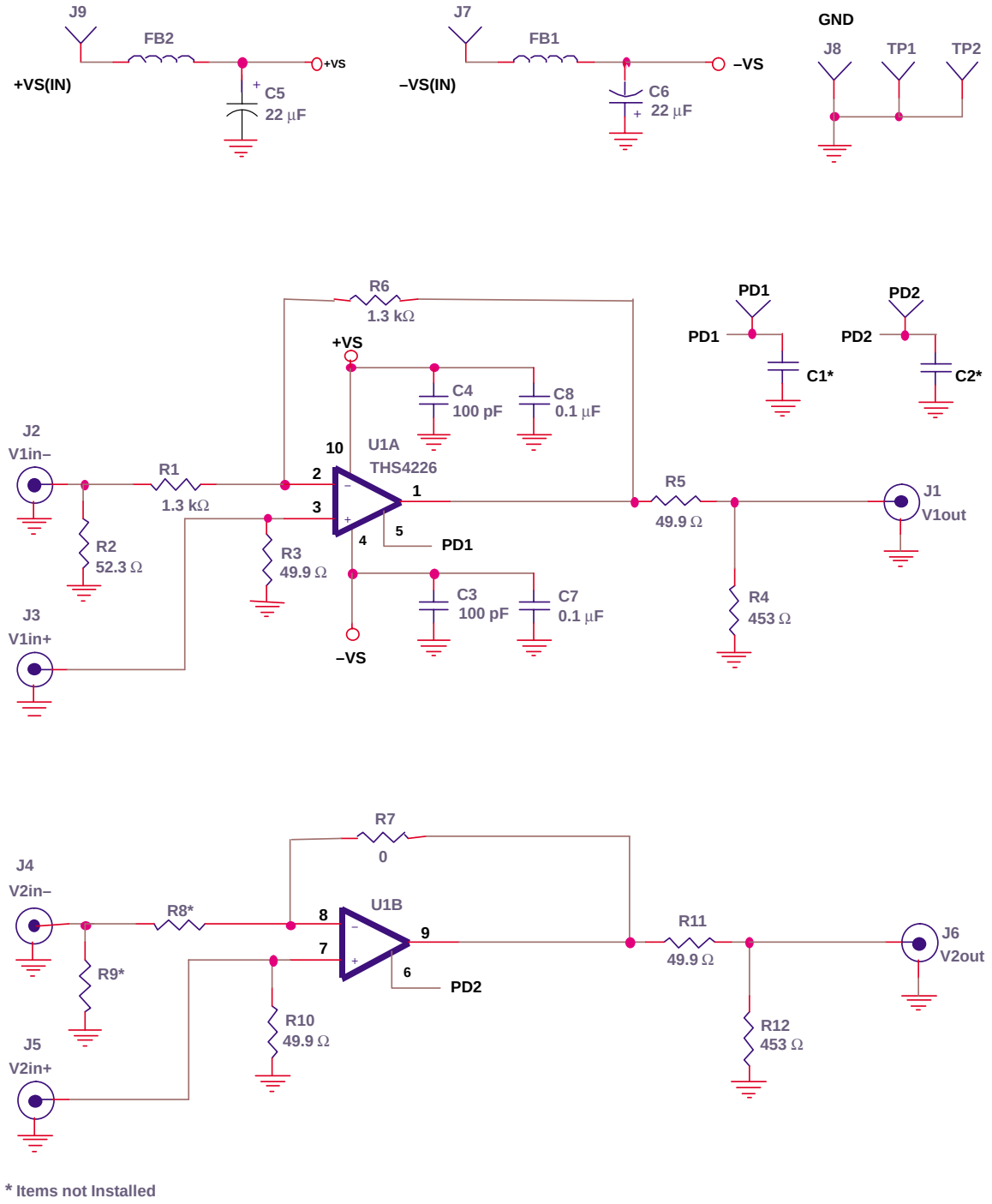
EVM Channel 2:

The default configuration for EVM channel 2 is designed to provide a voltage gain of +1 with the amplifier loaded with approximately 500 Ω. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 9) to the voltage input at J5.

R7 jumper makes EVM section 1 amplifier a unity gain buffer. R10 is 49.9 Ω to match the impedance of a 50-Ω signal generator. R11 and R12 form a voltage divider to J6, the EVM channel 2 output jack. The following equation represents the voltage gain to J6, if a measurement device with a 50-Ω input impedance is connected to J5.

$$\frac{V_O}{V_I} = \left(\frac{R12 \parallel 50\ \Omega}{R12 \parallel 50\ \Omega + R11}\right) = 0.473 \qquad (2)$$

Figure 1–1. Schematic of the THS4226EVM



* Items not Installed

Chapter 2

Using the THS4226EVM

This chapter shows how to connect the THS4226EVM to test equipment. It is recommended that the user connect the EVM as shown in this chapter to avoid damage to the EVM or the THS4226 installed on the board. Figure 2-1 shows how to connect the power supplies, 50-Ω signal source and 50-Ω monitoring instrument.

Figure 2-1. THS4226EVM Connection Diagram

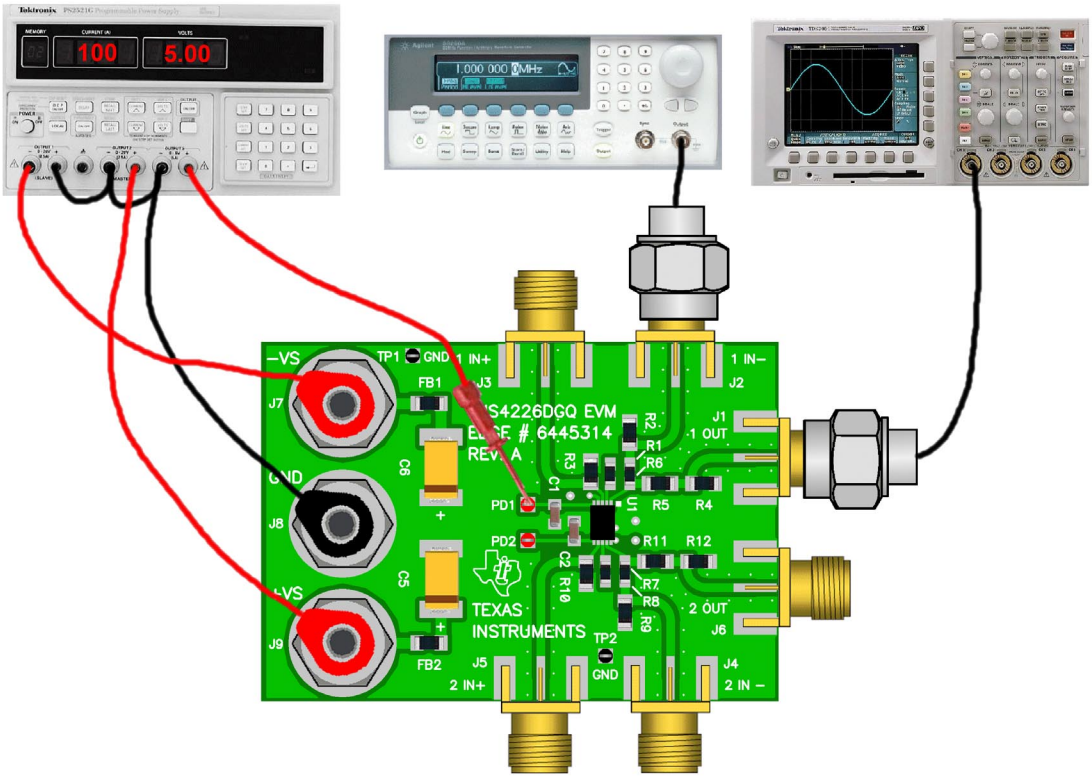


Figure 2-1 shows the connections to measure output 1 while a signal is inserted into the channel 1, noninverting input of the EVM. If the oscilloscope input is connected to J1, and the signal source is connected to J2, EVM channel 2 is also configured for a noninverting signal path.

Chapter 3

THS4226EVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That is the function of an evaluation board.

3.1 Inverting Video Gain Stage

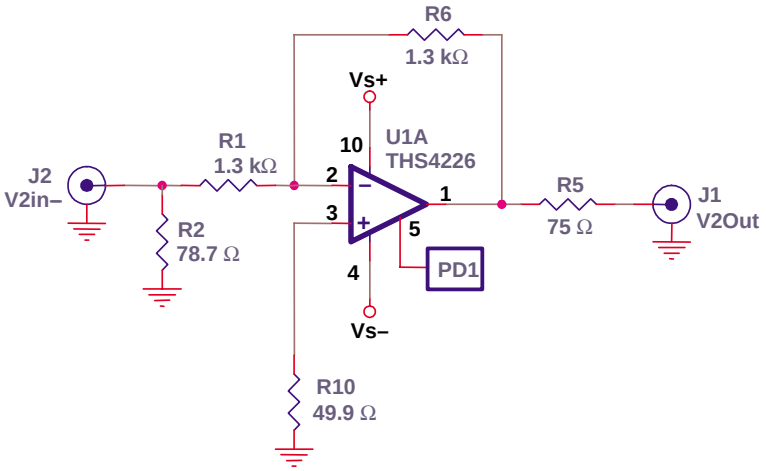
The circuit described in Chapter 1 is an inverting gain stage with a voltage divider on the output. Equation 1 indicates the gain when R2 is changed to 78.7 Ω, R5 is changed to 75 Ω and R4 is removed. Rt is the termination resistance of the measurement device. The voltage gain from J2 to J1 is simplified, as shown:

$$\frac{V_O}{V_I} = -\frac{R6}{R1}\left(\frac{Rt}{Rt + R5}\right) = 0.5 \qquad (1)$$

R5 is used to match the output impedance of the amplifier to the line being driven and the instrument taking measurements. For short transmission line length, R5 can be replaced with a jumper.

R5 can also be used to isolate the amplifier from large capacitive loads.

Figure 3–1. Inverting Video Gain Stage

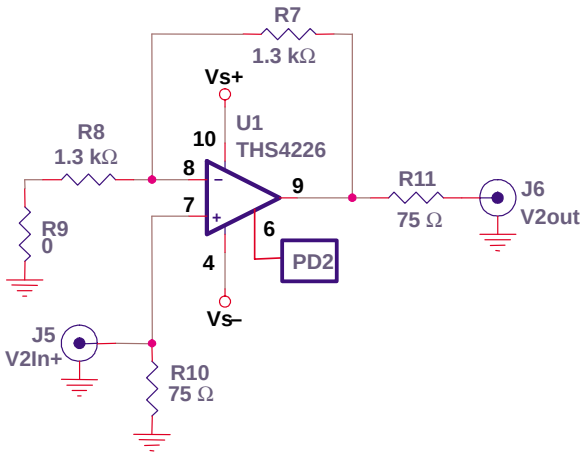


3.2 Noninverting Video Gain Stage

For a noninverting stage in EVM channel 2, the gain error imposed by R9 can be eliminated by replacing R9 with a 0-Ω resistor. Rt is the termination resistor of 75 Ω, as shown in Figure 3–2. As in the inverting gain stage example above, R12 has been removed. The following equation indicates the voltage gain from J5 to J6 when connected to a 75-Ω measurement instrument.

$$\frac{V_O}{V_I} = \left(1 + \frac{R7}{R8}\right)\left(\frac{Rt}{Rt + R11}\right) = 1 \qquad (2)$$

Figure 3–2. Noninverting Video Gain Stage



This is a common amplifier configuration used to drive transmission lines. The 75-Ω resistor in series with the output is for connection to a video instrument or circuit.

3.3 Applications for EVM Channel 2

Since the board layout of EVM Channel 1 is identical to EVM Channel 2, the applications above can be applied identically. The only physical difference is the component values installed in the default configuration for the different EVM channels. In addition, the components are labeled differently for each EVM channel. Refer to the complete schematic and board silkscreen to locate and resolve the differences.

3.4 Power-Down Functionality Saves Power

The THS4226 EVM features a power-down pin (PD) for each channel, which lowers the quiescent current from 14 mA/channel down to 700 µA/channel, ideal for reducing system power. The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the *power-on* mode of operation. To turn off the amplifier and conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables in the data sheets. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies, depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds, because the amplifier moves in and out of the linear mode of operation in these transitions.

Chapter 4

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed circuit board layout.

Table 4–1. THS4226EVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB QTY	Manufacturer's Part Number	Distributor's Part Number
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R–00	(Digi-Key) 240–1010–1–ND
2	Cap, 22 µF, tanatalum, 25 V, 10%	D	C5, C6	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C1, C2, C7, C8	4	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C3, C4	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
5	Open	0805	R8	1		
6	Resistor, 0 Ω, 1/8 W	0805	R7	1	(Phycomp) 9C08052A0R00JLHFT	(Garrett) 9C08052A0R00JLHFT
7	Resistor, 1.3 kΩ, 1/8 W, 1%	0805	R1, R6	2	(Phycomp) 9C08052A1301FKHFT	(Garrett) 9C08052A1301FKHFT
8	Open	1206	R4, R9, R12	3		
9	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R3, R10	2	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
10	Resistor, 52.3 Ω, 1/4W, 1%	1206	R2	1	(Phycomp) 9C12063A52R3FKRFT	(Garrett) 9C12063A52R3FKRFT
11	Resistor, 453 Ω, 1/4 W, 1%	1206	R11	1	(Phycomp) 9C12063A4530FKRFT	(Garrett) 9C12063A4530FKRFT
12	Resistor, 953 Ω, 1/4 W, 1%	1206	R5	1	(Phycomp) 9C12063A9530FKRFT	(Garrett) 9C12063A9530FKRFT
13	Jack, banana, 0.25" Dia. Hole		J7, J8, J9	3	(SPC) 813	(Newark) 39N867
14	Test point, red		PD1, PD2	2	(Keystone) 5000	(Digi–Key) 5000K–ND
15	Test point, black		TP1, TP2	2	(Keystone) 5001	(Digi–Key) 5001K–ND
16	Connector, edge, SMA PCB Jack		J1, J2, J3, J4, J5, J6	6	(Johnson) 142–0701–801	(Newark) 90F2624
17	IC, THS4226		U1	1	(TI) THS4226DGQ	
18	Board, printed-circuit			1	(TI) EDGE #6445314	

Figure 4-1. Top View Showing Top Layer and Component Placement for THS4226EVM

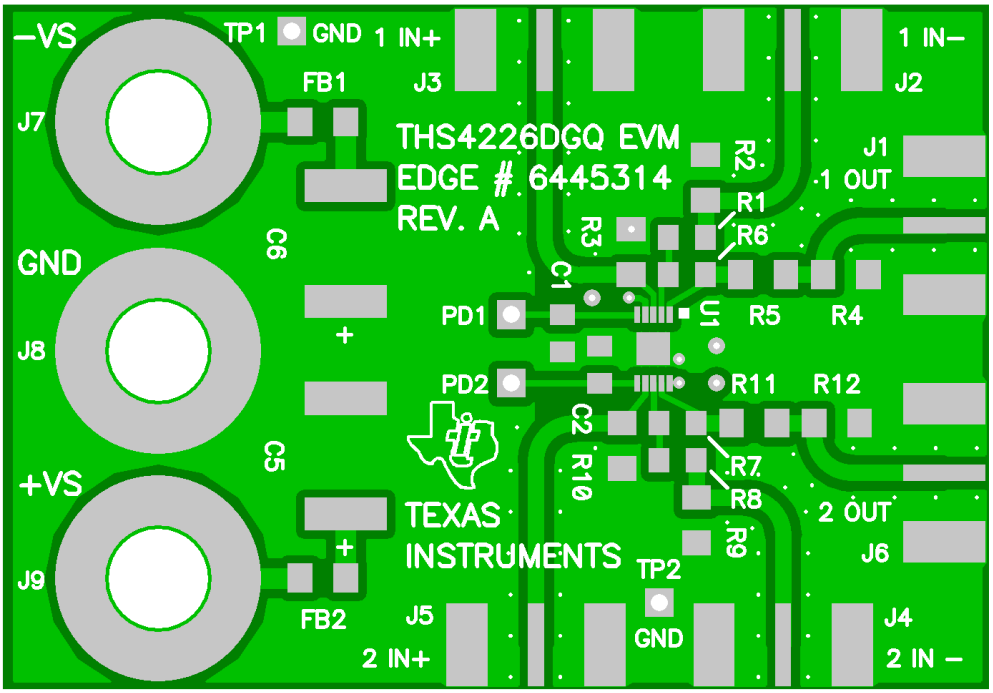


Figure 4-2. Internal Plane (Layer 2) Ground Plane

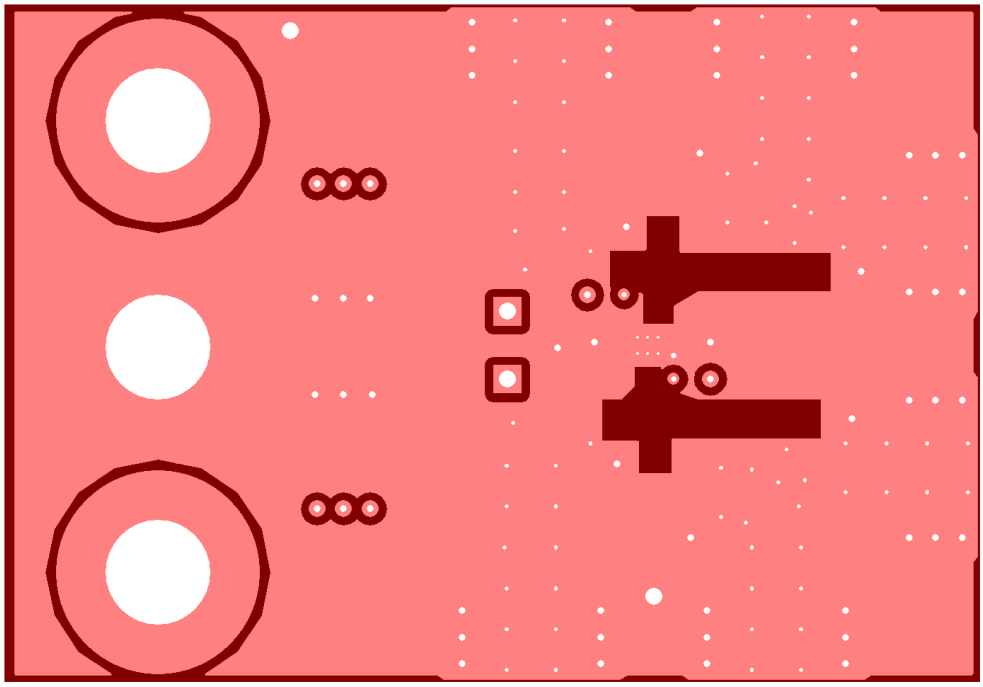


Figure 4-3. Internal Plane (Layer 3) Power Plane7

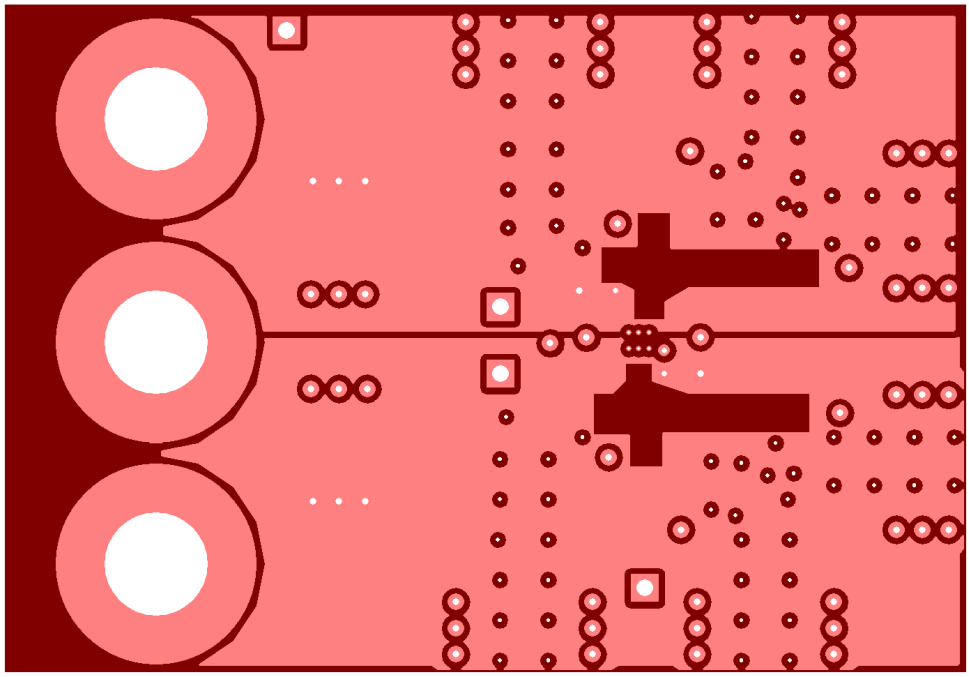
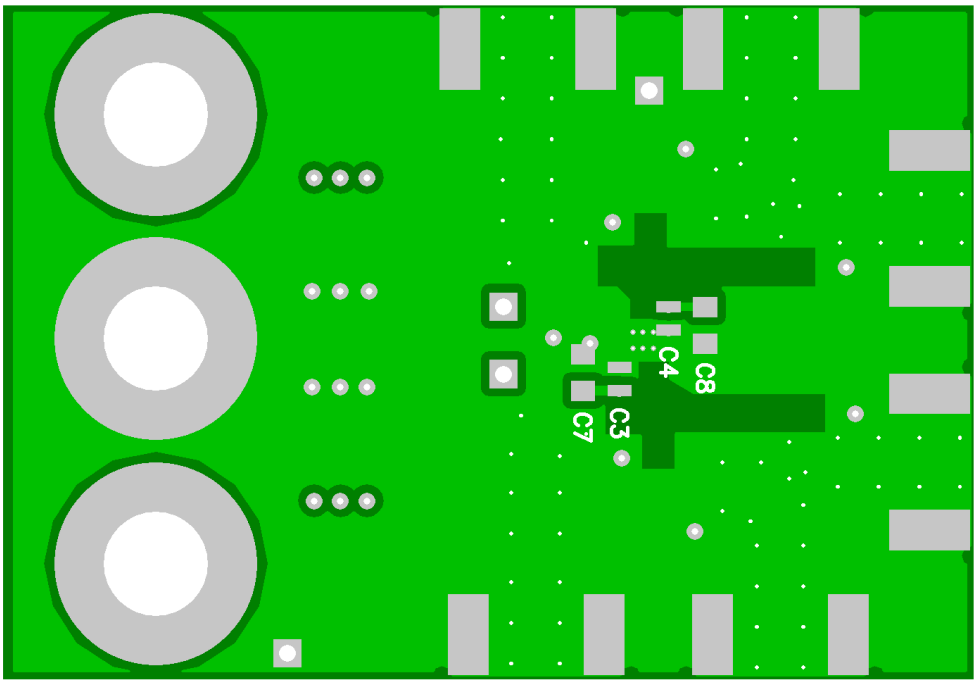



Figure 4-4. Bottom (Layer 4) Ground and Signal