INTEGRATED CIRCUITS

DATA SHEET

HEF4794B
8-stage shift-and-store register LED driver

Product specification
File under Integrated Circuits, IC04

June 1994

Philips Semiconductors

PHILIPS

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APPLICATIONS

- Automotive
- Industrial.

GENERAL DESCRIPTION

The HEF4794B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel LED driver outputs O_0 to O_7. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O_S') are available for cascading a number of HEF4794B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_S' on the next negative-going clock edge and provides cascading HEF4794B devices when the clock rise time is slow.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4794BT	16	SO16	plastic	SOT109-1
HEF4794BP	16	DIP16	plastic	SOT38-3

FUNCTIONAL DIAGRAM

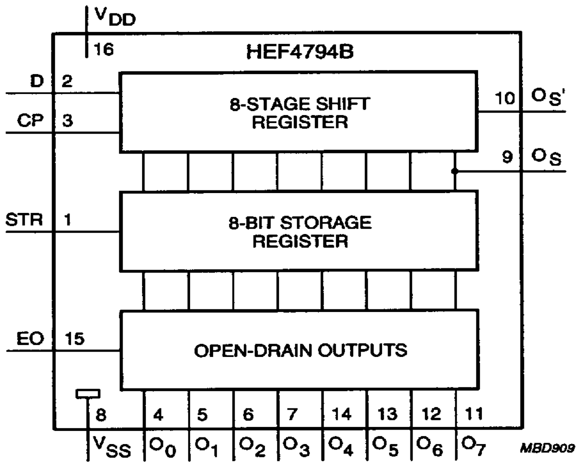


Fig.1 Functional diagram.

LOGIC DIAGRAMS

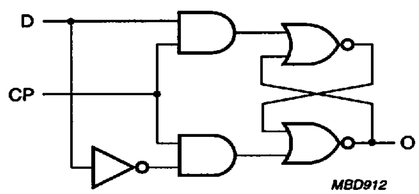


Fig.2 One D-latch.

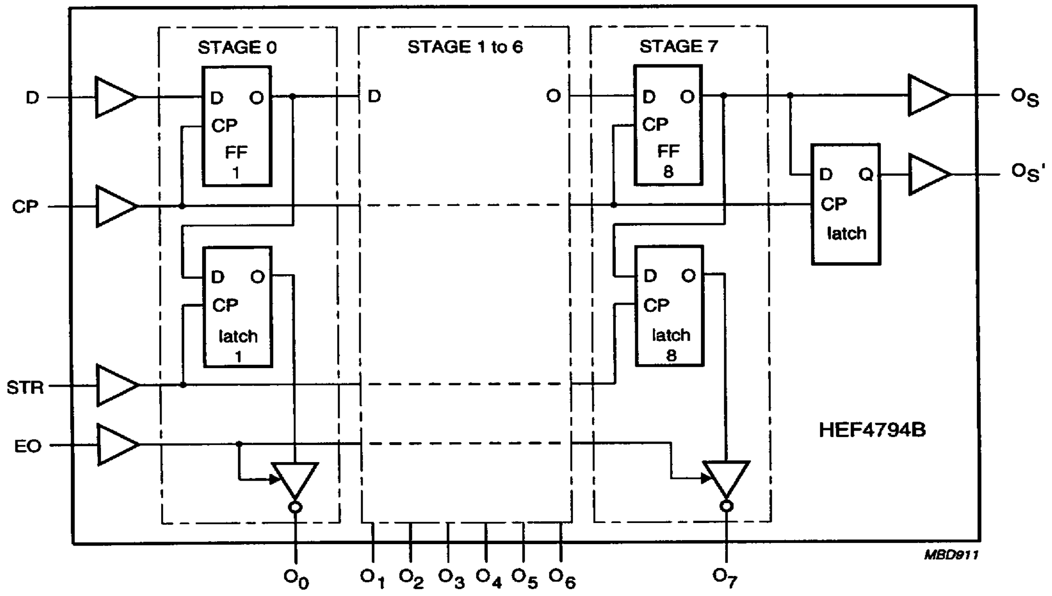


Fig.3 Logic diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STR	1	strobe input
D	2	data input
CP	3	clock input
O_0 to O_3	4 to 7	parallel outputs 0 to 3 (open drain)
V_{SS}	8	ground
O_S, O_S'	9 and 10	serial outputs
O_7	11	parallel output 7 (open drain)
O_6	12	parallel output 6 (open drain)
O_5	13	parallel output 5 (open drain)
O_4	14	parallel output 4 (open drain)
EO	15	output enable input
V_{DD}	16	supply voltage

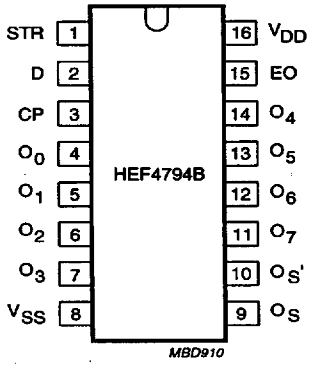


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

Table 1 Function table; note 1.

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	EO	STR	D	O_0	O_n	O_S	O_S'
↑	L	X	X	Z	Z	O_6'	nc
↓	L	X	X	Z	Z	nc	O_7
↑	H	L	X	nc	nc	O_6'	nc
↑	H	H	L	L	O_{n-1}	O_6'	nc
↑	H	H	H	H	O_{n-1}	O_6'	nc
↓	H	H	H	nc	nc	nc	O_7

Note

1. H = HIGH state;
   L = LOW state;
   X = don't care;
   ↑ = positive-going transition;
   ↓ = negative-going transition;
   Z = high-impedance OFF state;
   nc = no change;
   O_6' = the information in the seventh shift register stage.

   At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and the O_S output.

FAMILY DATA

See *"Family Specifications"* except for: rating for DC current into any open-drain output is 40 mA.

I_{DD} LIMITS CATEGORY MSI

See *"Family Specifications"* for ratings.

DC CHARACTERISTICS

V_{SS} = 0 V.

SYMBOL	PARAMETER	CONDITIONS	T_{amb} (°C)						UNIT
			−40		+25		+85		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OL}	LOW level output voltage	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 20$ mA; $V_{DD} = 5$ V	−	0.75	−	0.75	−	1.5	V
		$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 20$ mA; $V_{DD} = 10$ V	−	0.75	−	0.75	−	1.5	V
		$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 20$ mA; $V_{DD} = 15$ V	−	0.75	−	0.75	−	1.5	V
I_{OZH}	HIGH level output leakage current; 3-state	$V_O = 15$ V; $V_{DD} = 5$ V	−	2	−	2	−	15	μA
		$V_O = 15$ V; $V_{DD} = 10$ V	−	2	−	2	−	15	μA
		$V_O = 15$ V; $V_{DD} = 15$ V	−	2	−	2	−	15	μA

AC POWER CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL FORMULA FOR P (μW)[(1)]
P	dynamic power dissipation per package	V_{DD} = 5 V	$1200f_i + \Sigma(f_oC_L) \times V_{DD}^2$
		V_{DD} = 10 V	$5550f_i + \Sigma(f_oC_L) \times V_{DD}^2$
		V_{DD} = 15 V	$15000f_i + \Sigma(f_oC_L) \times V_{DD}^2$

Note

1. Where:
   $R_L = \infty$;
   f_i = input frequency (MHz);
   f_o = output frequency (MHz);
   C_L = load capacitance (pF);
   $\Sigma(f_oC_L)$ = sum of outputs;
   V_{DD} = supply voltage (V).

AC TIMING CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns; unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
t_{PHL}	propagation delay time CP to O_S; HIGH-to-LOW	5	–	160	320	ns	132 ns + (0.55 ns/pF)C_L
		10	–	65	130	ns	53 ns + (0.23 ns/pF)C_L
		15	–	45	90	ns	37 ns + (0.16 ns/pF)C_L
t_{PLH}	propagation delay time CP to O_S; LOW-to-HIGH	5	–	130	260	ns	102 ns + (0.55 ns/pF)C_L
		10	–	55	110	ns	44 ns + (0.23 ns/pF)C_L
		15	–	40	80	ns	32 ns + (0.16 ns/pF)C_L
t_{PHL}	propagation delay time CP to O_S'; HIGH-to-LOW	5	–	120	240	ns	92 ns + (0.55 ns/pF)C_L
		10	–	50	100	ns	39 ns + (0.23 ns/pF)C_L
		15	–	40	80	ns	32 ns + (0.16 ns/pF)C_L
t_{PLH}	propagation delay time CP to O_S'; LOW-to-HIGH	5	–	130	260	ns	102 ns + (0.55 ns/pF)C_L
		10	–	60	120	ns	49 ns + (0.23 ns/pF)C_L
		15	–	45	90	ns	37 ns + (0.16 ns/pF)C_L
t_{PZL}	propagation delay time CP to O_n; OFF-to-LOW	5	–	240	480	ns	note 1
		10	–	80	160	ns	
		15	–	55	110	ns	
t_{PLZ}	propagation delay time CP to O_n; LOW-to-OFF	5	–	170	340	ns	note 1
		10	–	75	150	ns	
		15	–	60	120	ns	

SYMBOL	PARAMETER	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
t_{PZL}	propagation delay time STR to O_n; OFF-to-LOW	5	–	140	280	ns	note 1
		10	–	70	140	ns	
		15	–	55	110	ns	
t_{PLZ}	propagation delay time STR to O_n; LOW-to-OFF	5	–	100	200	ns	note 1
		10	–	40	100	ns	
		15	–	35	70	ns	
t_{THL}	output transition time O_S and O_S'; HIGH-to-LOW	5	–	85	170	ns	35 ns + (1.0 ns/pF)C_L
		10	–	40	80	ns	19 ns + (0.42 ns/pF)C_L
		15	–	30	60	ns	16 ns + (0.28 ns/pF)C_L
t_{TLH}	output transition time O_S and O_S'; LOW-to-HIGH	5	–	85	170	ns	35 ns + (1.0 ns/pF)C_L
		10	–	40	80	ns	19 ns + (0.42 ns/pF)C_L
		15	–	30	60	ns	16 ns + (0.28 ns/pF)C_L
t_{PZL}	output enable time EO to O_n; OFF-to-LOW	5	–	100	200	ns	note 1
		10	–	55	110	ns	
		15	–	50	100	ns	
t_{PLZ}	output disable time EO to O_n; LOW-to-OFF	5	–	80	160	ns	note 1
		10	–	40	80	ns	
		15	–	30	60	ns	
t_{WCPL}	minimum clock pulse width LOW	5	60	30	–	ns	
		10	30	15	–	ns	
		15	24	12	–	ns	
t_{WSTRH}	minimum strobe pulse width HIGH	5	80	40	–	ns	
		10	60	30	–	ns	
		15	24	12	–	ns	
t_{su}	set-up time D to CP	5	60	30	–	ns	
		10	20	10	–	ns	
		15	15	5	–	ns	
t_h	hold time D to CP	5	+5	−15	–	ns	
		10	20	5	–	ns	
		15	20	5	–	ns	
$f_{clk(max)}$	maximum clock frequency	5	5	10	–	MHz	
		10	11	22	–	MHz	
		15	14	28	–	MHz	

Note

1. Definition of symbol equivalent to 3-state outputs.

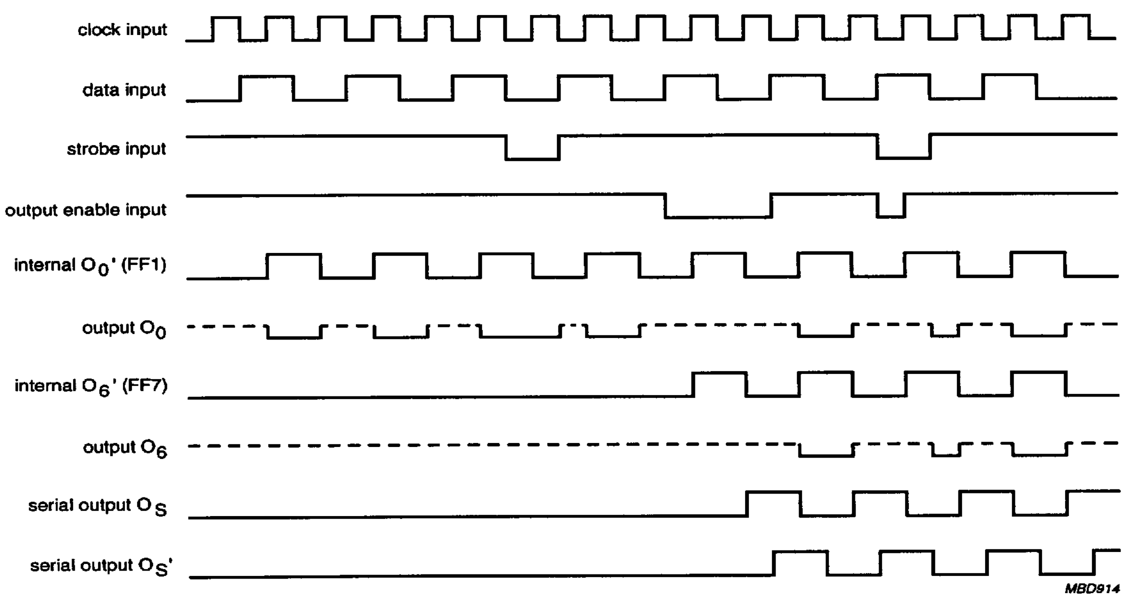


Fig.5 Timing diagram.

APPLICATION INFORMATION

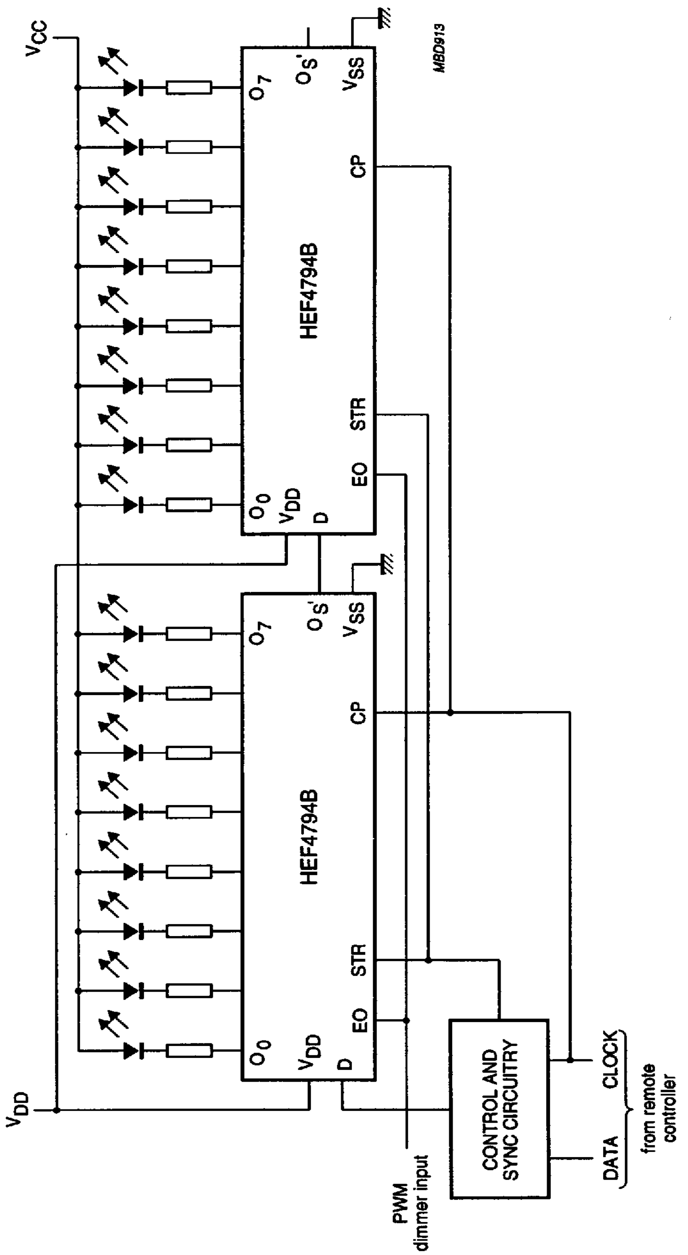
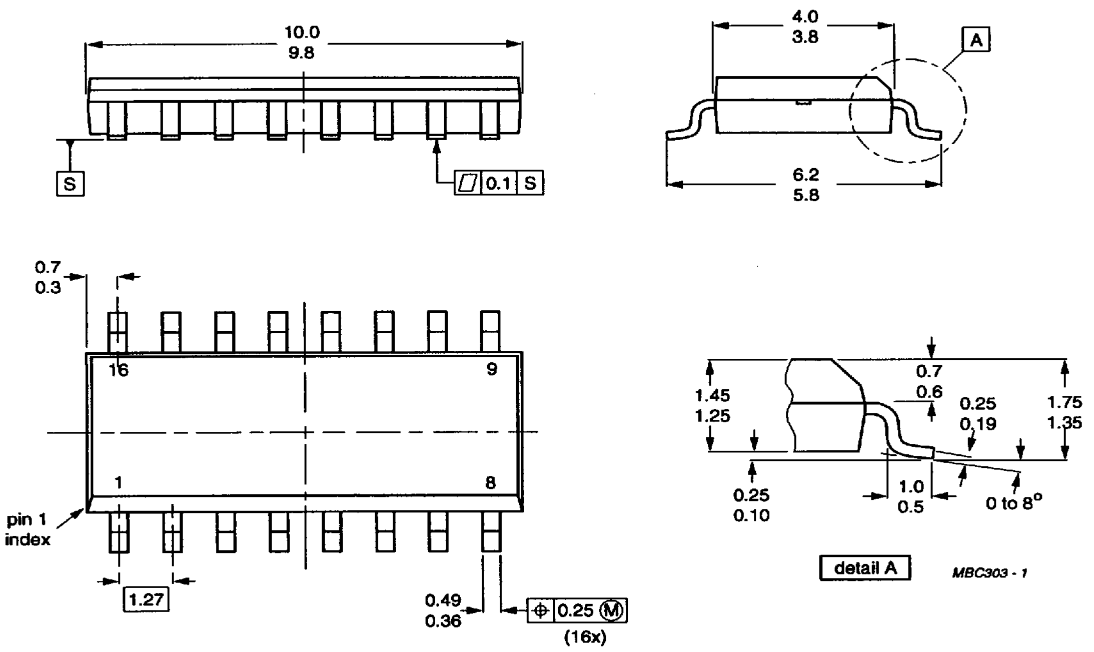


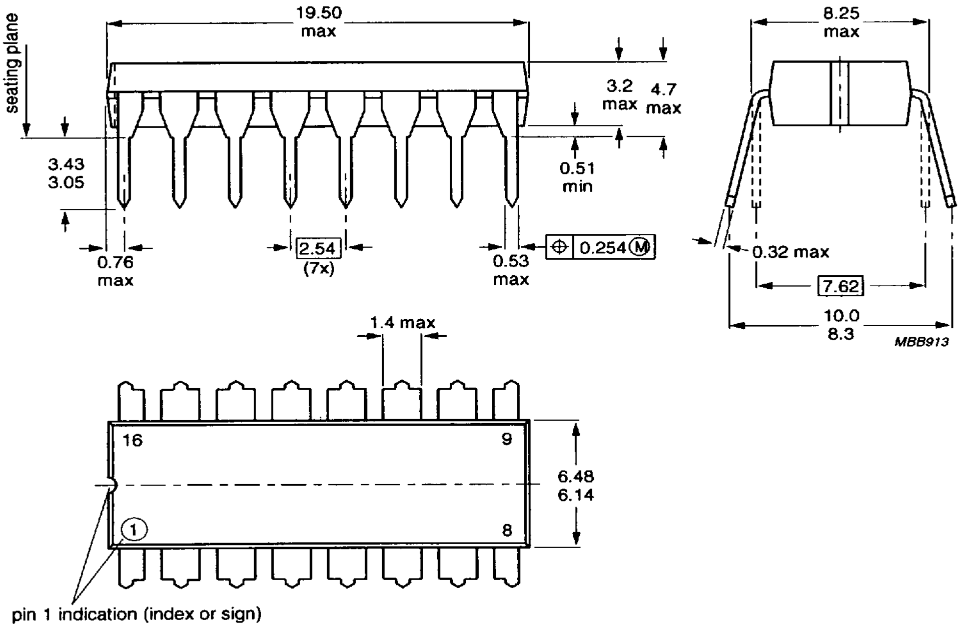
Fig.6 Application example: serial-to-parallel converting LED drivers.

PACKAGE OUTLINES



Dimensions in mm.

Fig.7 Plastic small outline package; 16 leads; (SO16; SOT109-1).



Dimensions in mm.

Fig.8 Plastic dual in-line package; 16 leads (300 mil); (DIP16; SOT38-3).

SOLDERING

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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