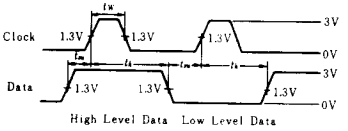
HD74ALS74 ●Dual D-type Positive-edge-triggered Flip-Flops (with Preset and Clear)

■FUNCTION TABLE

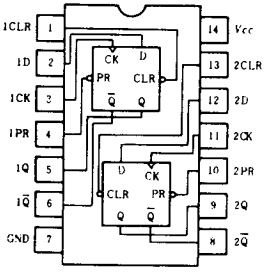
Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_0	$\overline{Q_0}$

Notes: H = high level, L = low level, X = irrelevant
↑ = transition from low to high level
Q_0 = level of Q before the indicated steady-state conditions were established.
$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
* = This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■TIMING DEFINITION



■PIN ARRANGEMENT



(Top View)

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Fan out	High level	N	—	—	20	
	Low level		—	—	20	
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width	High level	$t_{w(CK)}$	12	—	—	ns
	Low level		20	—	—	
Preset and clear pulse width		t_w	15	—	—	ns
Setup time	High level	t_{su}	15	—	—	ns
	Low level		15	—	—	
Hold time		t_h	0	—	—	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$	2.5	—	—	V
			$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$	2.7	—	—	
		V_{OL}	$V_{CC}=4.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=4mA$	—	—	0.4	V
			$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=8mA$	—	—	0.5	
Input current	All inputs	I_{IH}	$V_{CC}=5.5V$, $V_I=2.7V$	—	—	20	μA
		I_I	$V_{CC}=5.5V$, $V_I=7V$	—	—	0.1	mA
	Clock, D	I_{IL}	$V_{CC}=5.5V$, $V_I=0.4V$	—	—	−0.2	mA
	Clear, Preset			—	—	−0.4	
Output drive current		I_{OD}	$V_{CC}=5.5V$, $V_O=2.125V$	−10	—	−80	mA
Supply current		I_{CC}**	$V_{CC}=5.5V$	—	2.4	4	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.5V$, $I_{IN}=-18mA$	—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

** : With all outputs open, I_{CC} is measured with Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

■SWITCHING CHARACTERISTICS (V_{CC}=5±0.5V, Ta=−20∼+75°C)

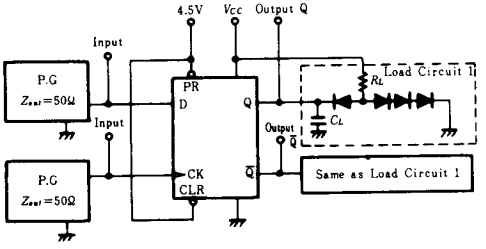
Item	Symbol	Input	Output	Test Conditions		min	typ	max	Unit
Maximum clock frequency	f_{max}			V_{CC}=5V, Ta=25°C		30	—	—	MHz
Propagation delay time	t_{PLH}	Clear Preset	$\overline{Q}$ Q	R_L=2kΩ	C_L=15pF*	3	9	13	ns
					C_L=50pF	3	—	21	
	t_{PHL}	Clear Preset	Q $\overline{Q}$		C_L=15pF*	5	14	20	
					C_L=50pF	5	—	28	
	t_{PLH}	Clock	Q, $\overline{Q}$		C_L=15pF*	5	9	13	
					C_L=50pF	5	—	21	
	t_{PHL}	Clock	Q, $\overline{Q}$		C_L=15pF*	6	12	18	
					C_L=50pF	6	—	28	

* V_{CC}=5V, Ta=25°C

■TESTING METHOD

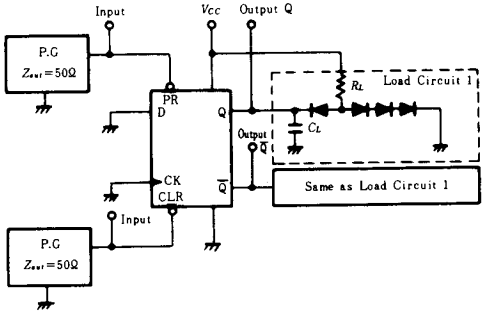
Test Circuit

1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q, $\overline{Q}$)



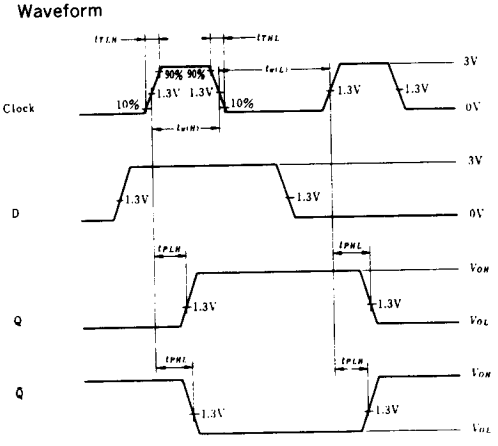
Notes: 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

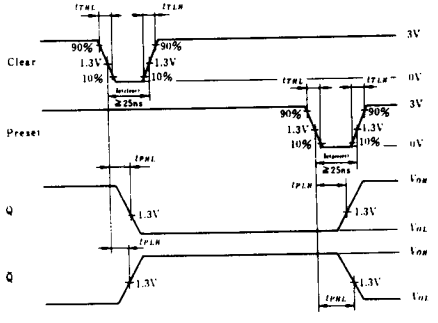
2) t_{PHL}, t_{PLH} (Clear or Preset→Q, $\overline{Q}$)



Notes: 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform





Note: Clock input pulse; t_{TLH} ≦ 6ns, t_{THL} ≦ 6ns, PRR = 1MHz, duty cycle 50% and: for f_{max}, t_{THL} = t_{TLH} ≦ 2.5ns.

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