

## CLC006 Serial Digital Cable Driver with Adjustable Outputs

Check for Samples: [CLC006](#)

### FEATURES

- No External Pull-down Resistors
- Adjustable Output Amplitude
- Differential Input and Output
- Low Power Dissipation
- Single +5V or –5.2V Supply
- Replaces GS9008 in Most Applications

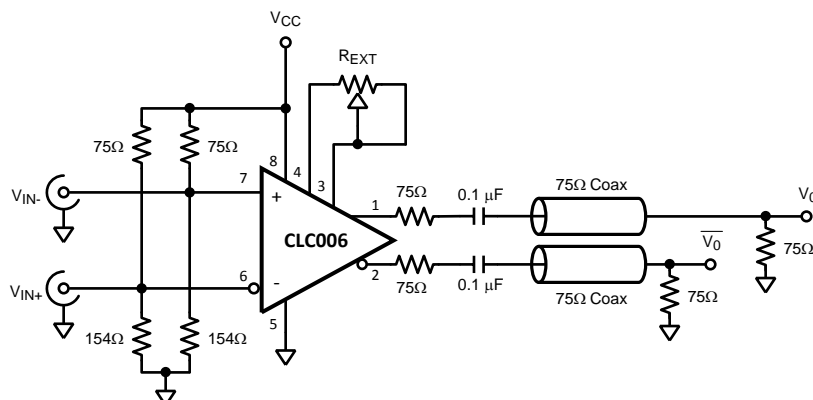
### APPLICATIONS

- Digital Routers and Distribution Amplifiers
- Coaxial Cable Driver for Digital Transmission Line
- Twisted Pair Driver
- Serial Digital Video Interfaces for the Commercial and Broadcast Industry
- SMPTE, Sonet/SDH, and ATM Compatible Driver
- Buffer Applications

### KEY SPECIFICATIONS

- 650 ps Rise and Fall Times
- Data Rates to 400 Mbps
- 200 mV Differential Input
- Low Residual Jitter (25 ps<sub>pp</sub>)

### Typical Application



### DESCRIPTION

Texas Instruments' Comlinear CLC006 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC006 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable. Output swing is adjustable from 0.7 V<sub>P-P</sub> to 2 V<sub>P-P</sub> using external resistors.

The CLC006's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV<sub>P-P</sub> to ECL levels within the specified common-mode limits. All this make the CLC006 an excellent general purpose high speed driver for digital applications.

The CLC006 is powered from a single +5V or –5.2V supply and comes in an 8-pin SOIC package.



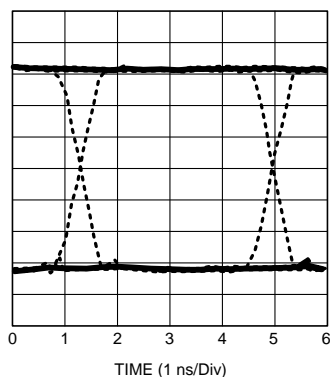
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

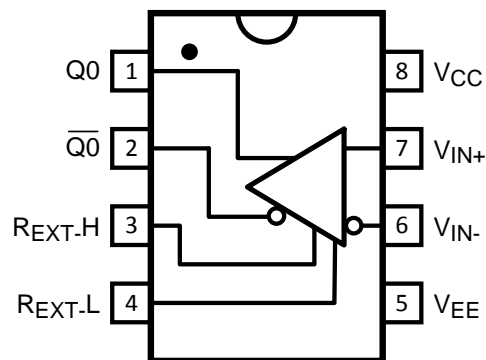
Copyright © 1998–2013, Texas Instruments Incorporated

## 270 Mbps Eye Pattern



**Figure 1.**

## Connection Diagram



**Figure 2. 8-Pin SOIC  
See Package Number D**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)</sup>

Supply Voltage		6V
Output Current		30 mA
Maximum Junction Temperature		+125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)		+300°C
ESD Rating (Human Body Model)		1000V
Package Thermal Resistance	$\theta_{JA}$ 8-pin SOIC	+160°C/W
	$\theta_{JC}$ 8-pin SOIC	+105°C/W
Reliability Information MTTF		254 Mhr

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of [Electrical Characteristics](#) specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## Recommended Operating Conditions

Supply Voltage Range ( $V_{CC} - V_{EE}$ )	+4.5V to +5.5V
--------------------------------------------	----------------

## Electrical Characteristics

( $V_{CC} = 0V$ ,  $V_{EE} = -5V$ ; unless otherwise specified).

Parameter	Condition	Typ +25°C	Min/Max +25°C <sup>(1)</sup>	Min/Max 0°C to +70°C <sup>(1)</sup>	Min/Max –40°C to +85°C <sup>(1)</sup>	Units
<b>STATIC DC PERFORMANCE</b>						
Supply Current, Loaded	150Ω @ 270 Mbps <sup>(2)</sup>	37	—	—	—	mA
Supply Current, Unloaded	<sup>(3)</sup>	34	28/45	26/47	26/47	mA
Output HIGH Voltage ( $V_{OH}$ )	<sup>(3)</sup>	–1.7	–2.0/1.4	–2.0/1.4	–2.0/1.4	V
Output LOW Voltage ( $V_{OL}$ )	<sup>(3)</sup>	–3.3	–3.6/3.0	–3.6/3.0	–3.6/3.0	V
Input Bias Current		10	30	50	50	μA
Output Swing	$R_{EXT} = \infty$ <sup>(3)</sup>	1.65	1.55/1.75	1.53/1.77	1.51/1.79	V
Output Swing	$R_{EXT} = 10\text{ k}\Omega$	1.30	—	—	—	V
Common Mode Input Range Upper Limit		–0.7	–0.8	–0.8	–0.8	V
Common Mode Input Range Lower Limit		–2.6	–2.5	–2.5	–2.5	V
Minimum Differential Input Swing		200	200	200	200	mV
Power Supply Rejection Ratio <sup>(3)</sup>		26	20	20	20	dB
<b>AC PERFORMANCE</b>						
Output Rise and Fall Time	<sup>(3)</sup> (4)(2)	650	425/825	400/850	400/850	ps
Overshoot		5				%
Propagation Delay		1.0				ns
Duty Cycle Distortion		50				ps
Residual Jitter		25	—	—	—	ps <sub>pp</sub>
<b>MISCELLANEOUS PERFORMANCE</b>						
Input Capacitance		1.0				pF
Output Resistance		10				Ω
Output Inductance		6				nH

(1) Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

(2) Measured with both outputs driving 150Ω, AC coupled at 270 Mbps.

(3) Spec is 100% tested at +25°C

(4) Measured between the 20% and 80% levels of the waveform.

## Operation

### INPUT INTERFACING

The CLC006 has high impedance, emitter-follower buffered, differential inputs. Single-ended signals may also be input. Transmission lines supplying input signals must be properly terminated close to the CLC006. Either A.C. or D.C. coupling as in Figure 4 or Figure 5 may be used. Figure 4, Figure 6 and Figure 7 show how Thevenin-equivalent resistor networks are used to provide input termination and biasing. The input D.C. common-mode voltage range is 0.8V to 2.5V below the positive power supply ( $V_{CC}$ ). Input signals plus bias should be kept within the specified common-mode range. For an 800 mV<sub>P-P</sub> input signal, typical input bias levels range from 1.2V to 2.1V below the positive supply.

Load Type	Resistor to $V_{CC}$ (R1)	Resistor to $V_{EE}$ (R2)
ECL, 50Ω, 5V, $V_T=2V$	82.5Ω	124Ω
ECL, 50Ω, 5.2V, $V_T=2V$	80.6Ω	133Ω
ECL, 75Ω, 5V, $V_T=2V$	124Ω	187Ω
ECL, 75Ω, 5.2V, $V_T=2V$	121Ω	196Ω
800 mV <sub>P-P</sub> , 50Ω, 5V, $V_T=1.6V$	75.0Ω	154Ω
800 mV <sub>P-P</sub> , 75Ω, 5V, $V_T=1.6V$	110Ω	232Ω
800 mV <sub>P-P</sub> , 2.2KΩ, 5Ω, $V_T=1.6V$	3240Ω	6810Ω

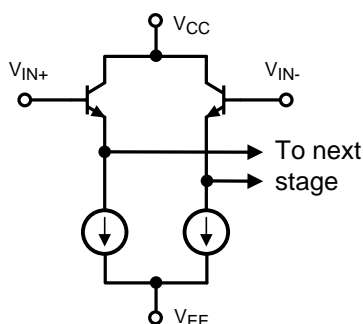


Figure 3. Input Stage

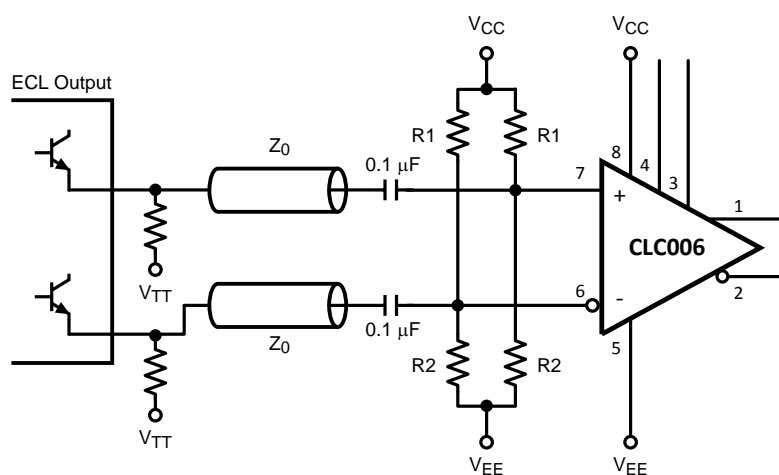
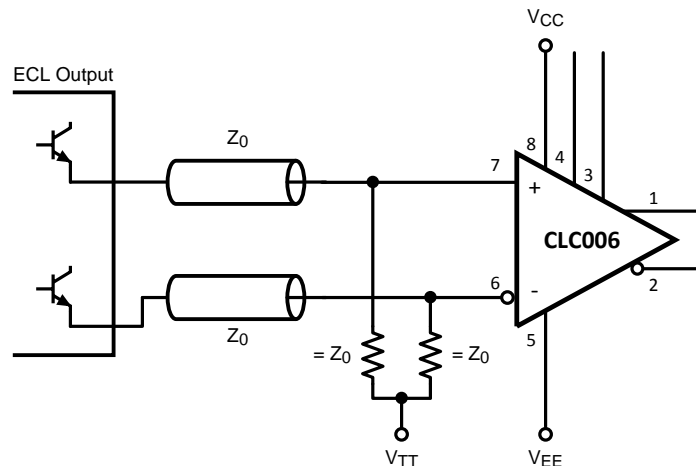
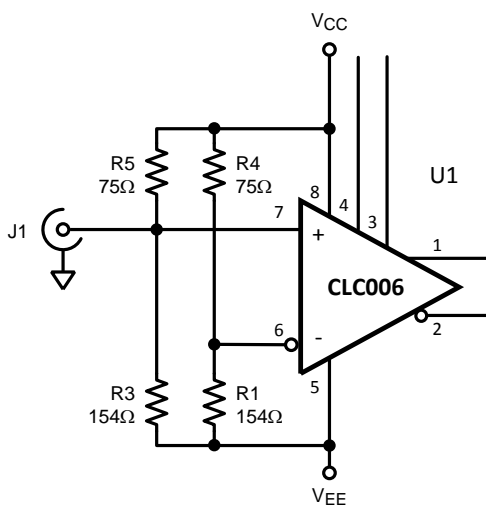


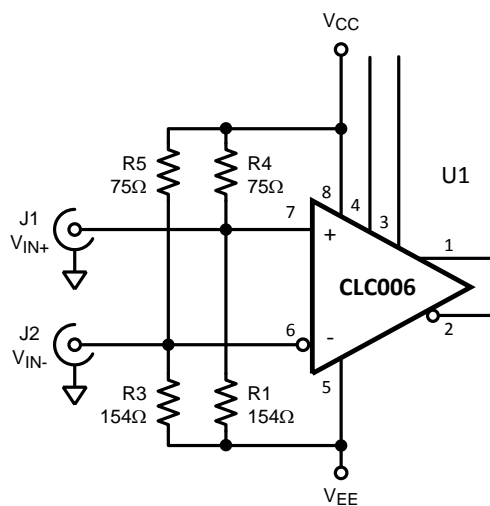
Figure 4. AC Coupled Input



**Figure 5. DC Coupled Input**



**Figure 6. Single Ended 50Ω ECL input**



**Figure 7. Differential 50Ω ECL Input**

## OUTPUT INTERFACING

The CLC006's class AB output stage, [Figure 8](#), requires no standing current in the output transistors and therefore requires no biasing or pull-down resistors. Advantages of this arrangement are lower power dissipation and fewer external components. The output may be either D.C. or A.C. coupled to the load. A bandgap voltage reference sets output voltage levels which are compatible with F100K and 10K ECL when correctly terminated. The outputs do not have the same output voltage temperature coefficient as 10K. Therefore, noise margins will be reduced over the full temperature range when driving 10K ECL. Noise margins will not be affected when interfacing to F100K since F100K is fully voltage and temperature compensated.

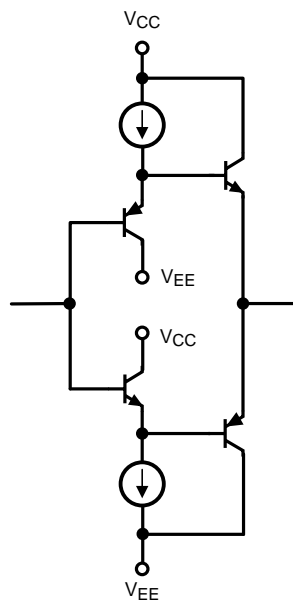


Figure 8. Output Stage

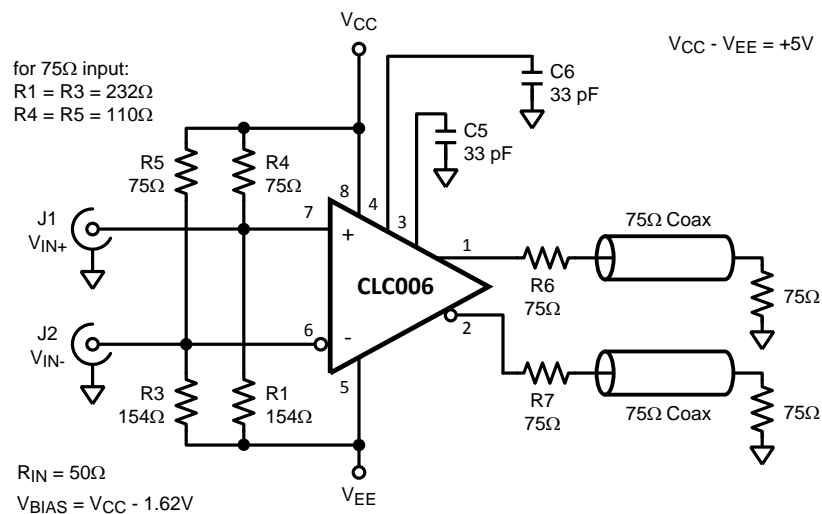


Figure 9. Differential Input DC Coupled Output

## OUTPUT AMPLITUDE ADJUSTMENT

The high and low output levels of the CLC006 are set by a circuit shown simplified in Figure 10. Output high and low levels may be set independently with external resistor networks connected between  $R_{EXT-H}$  (pin 3),  $R_{EXT-L}$  (pin 4) and the power supplies. The resistor networks affect the high and low output levels by changing the internally generated bias voltages,  $V_H$  and  $V_L$ . The nominal high and low output levels are  $V_{CC}-1.7V$  and  $V_{CC}-3.3V$ , respectively, when the pins  $R_{EXT-H}$  and  $R_{EXT-L}$  are left unconnected. Though the internal components which determine output voltage levels have accurate ratios, their absolute values may be controlled only within about  $\pm 15\%$  of nominal. Even so, without external adjustment, output voltages are well controlled. A final design should accommodate the variation in externally set output voltages due to the CLC006's part-to-part and external component tolerances.

Output voltage swing may be reduced with the circuit shown in Figure 11. A single resistance chosen with the aid of the graph, Figure 12, is connected between pins 3 and 4. Output voltage swing may be increased with the circuit of Figure 13. Figure 14 is used to estimate a value for resistor R. Note that both of these circuits and the accompanying graphs assume that the CLC006 is loaded with the standard  $150\Omega$ . Be aware that output loading will affect the output swing and the high and low levels. It may be necessary to empirically select resistances used to set output levels when the D.C. loading on the CLC006 differs appreciably from  $150\Omega$ .

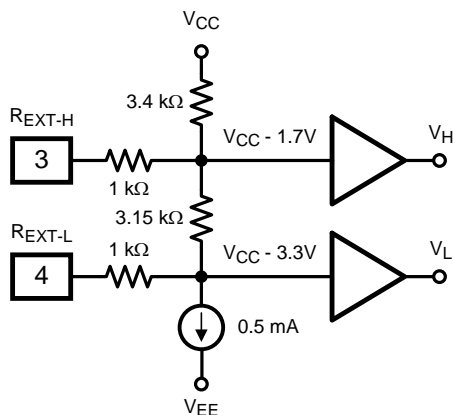


Figure 10. Equivalent Bias Generation Circuit

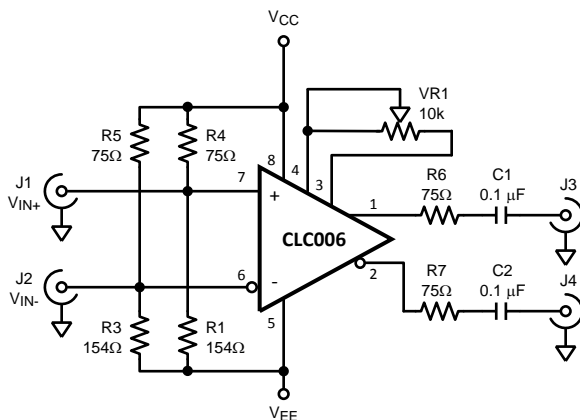
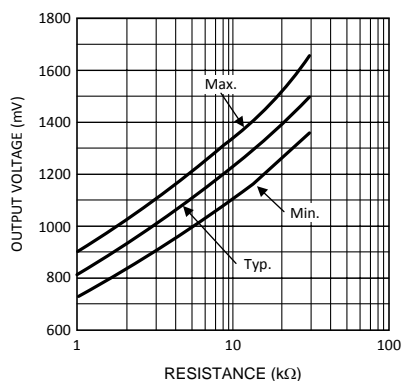
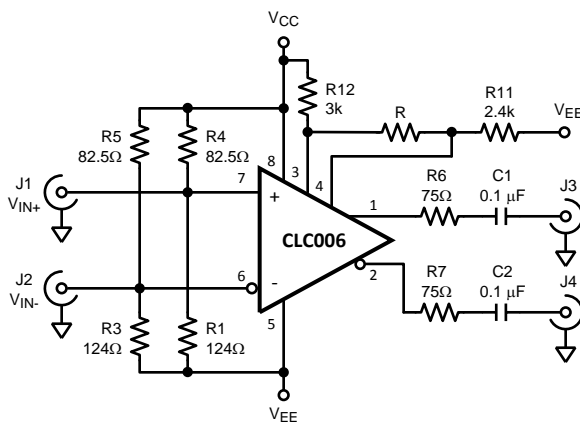


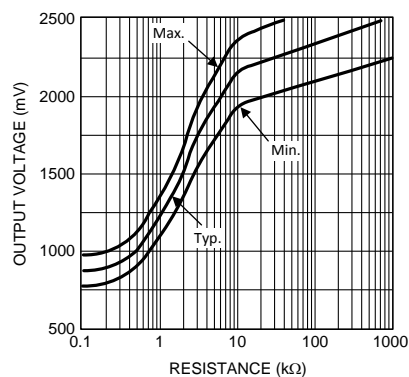
Figure 11. Differential Input Reduced Output



**Figure 12. Resistance Pins 3 to 4 vs Output Voltage Reduced Output @ 150Ω Load**



**Figure 13. Differential Input Increased Output**

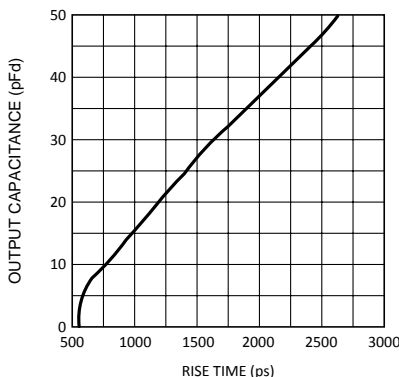


**Figure 14. Resistance Pins 3 to 4 vs Output Voltage Increased Output @ 150Ω Load**



## OUTPUT RISE AND FALL TIMES

Output load capacitance can significantly affect output rise and fall times. The effect of load capacitance, stray or otherwise, may be reduced by placing the output back-match resistor close to the output pin and by minimizing all interconnecting trace lengths. Figure 15 shows the effect on risetime of parallel load capacitance across a 150Ω load.



**Figure 15. Rise Time vs  $C_L$**

## PCB Layout Recommendations

Printed circuit board layout affects the performance of the CLC006. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 μF monolithic ceramic capacitor in parallel with a 6.8 μF tantalum electrolytic capacitor located no more than 0.1" (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
  - inputs,
  - supply bypass capacitors and
  - the output load.
- Provide short, grounded guard traces located
  - under the centerline of the package,
  - 0.1" (2.5 mm) from the package pins
  - on both top and bottom of the board with connecting vias.

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">9</a>

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLC006BM	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	CLC00 6BM>D	<a href="#">Samples</a>
CLC006BM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	CLC00 6BM>D	<a href="#">Samples</a>
CLC006BMX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	CLC00 6BM>D	<a href="#">Samples</a>
CLC006BMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	CLC00 6BM>D	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLC006BMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLC006BMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)