National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM3940-3.3-X REV 0B0

Original Creation Date: 09/30/97
Last Update Date: 11/18/98
Last Major Revision Date: 09/30/97

1A LOW DROPOUT REGULATOR

General Description

The LM3940 is a 1A low dropout regulator designed to provide 3.3V from a 5V supply.

The LM3940 is ideally suited for systems which contain both 5V and 3.3V logic, with prime power provided from a 5V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3V output in regulation with input voltages as low as 4.5V.

Industry Part Number

LM3940

NS Part Numbers

LM3940J-3.3-QML*
LM3940WG3.3-QML**

Prime Die

LM3940

Controlling Document

5962-9688401QEA*, QXA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Excellent load regulation
- Guaranteed 1A output current
- Requires only one external component
- Built-in protection against excess temperature
- Short circuit protected

Applications

- Logic Systems

(Absolute Maximum Ratings)

(Note 1)

Input Supply Voltage		7.5V
Internal Power Dissipation (Note 2, 3)		Internally Limited
Operating Ambient Temperature		-55 C to +125 C
Storage Temperature Range		-65 C to +150 C
Maximum Junction Temperature		150 C
Thermal Resistance (Note 3)		
ThetaJA		
CERDIP	(Still Air)	74 C/W
	(500LF/Min Air flow)	37 C/W
CERAMIC SOIC	(Still Air)	122 C/W
	(500LF/Min Air flow)	77 C/W
ThetaJC		
CERDIP		4 C/W
CERAMIC SOIC		5 C/W
Package Weight		
CEDIP		1970mg
CERAMIC SOIC		360mg
Lead Temperature (Soldering, 5 seconds)		260 C
ESD Susceptibility (Note 4)		4kV

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specification apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 100pF discharged through 1.5K Ohms

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = 5V, IL = 1A, Cout = 33uF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage	5mA ≤ IL ≤ 1A			3.20	3.40	V	1
		5mA ≤ IL ≤ 1A			3.13	3.47	V	2, 3
Delta Vo/Delta Vi	Line Regulation	IL = 5mA, 4.5V ≤ Vin ≤ 5.5V				40	mV	1
		IL = 5mA, 4.5V ≤ Vin ≤ 5.5V				99	mV	2, 3
Delta Vo/IL	Load Regulation	50mA ≤ IL ≤ 1A				50	mV	1
		50mA ≤ IL ≤ 1A				80	mV	2, 3
Iq	Quiescent Current	4.5V ≤ Vin ≤ 5.5V, IL = 5mA				15	mA	1
		4.5V ≤ Vin ≤ 5.5V, IL = 5mA				20	mA	2, 3
		Vin = 5V, IL = 1A				200	mA	1
						250	mA	2, 3
Vo - Vin	Dropout Voltage	IL = 1A	1			0.8	V	1
			1			1.0	V	2, 3
		IL = 100mA	1			150	mV	1
			1			200	mV	2, 3
IL(SC)	Short Circuit Current	Rl = 0			1.2		A	1, 2, 3

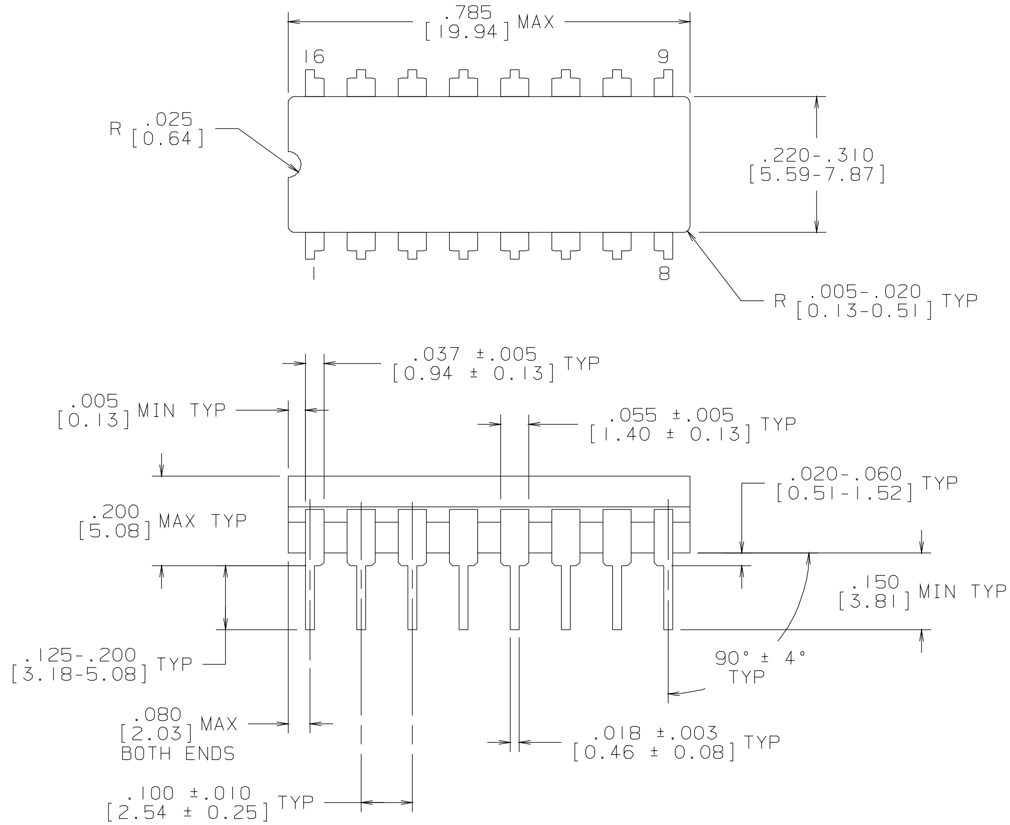
Note 1: Dropout voltage is defined as the input-output differential voltage where the regulator output drops to a value that is 100 mV below the value that is measured at Vin = 5V.

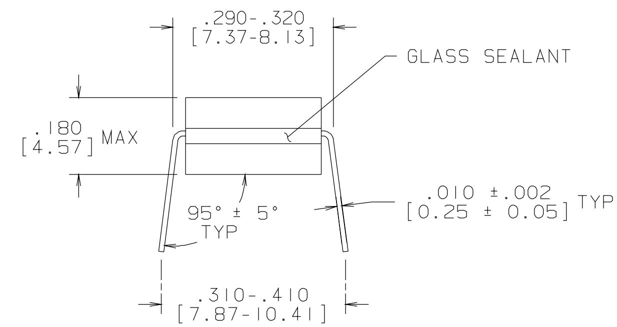
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06332HRA2	CERDIP (J), 16 LEAD (B/I CKT)
06351HRA1	CERPACK (W), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000377A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
P000389A	CERDIP (J), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/





MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

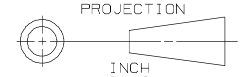
CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

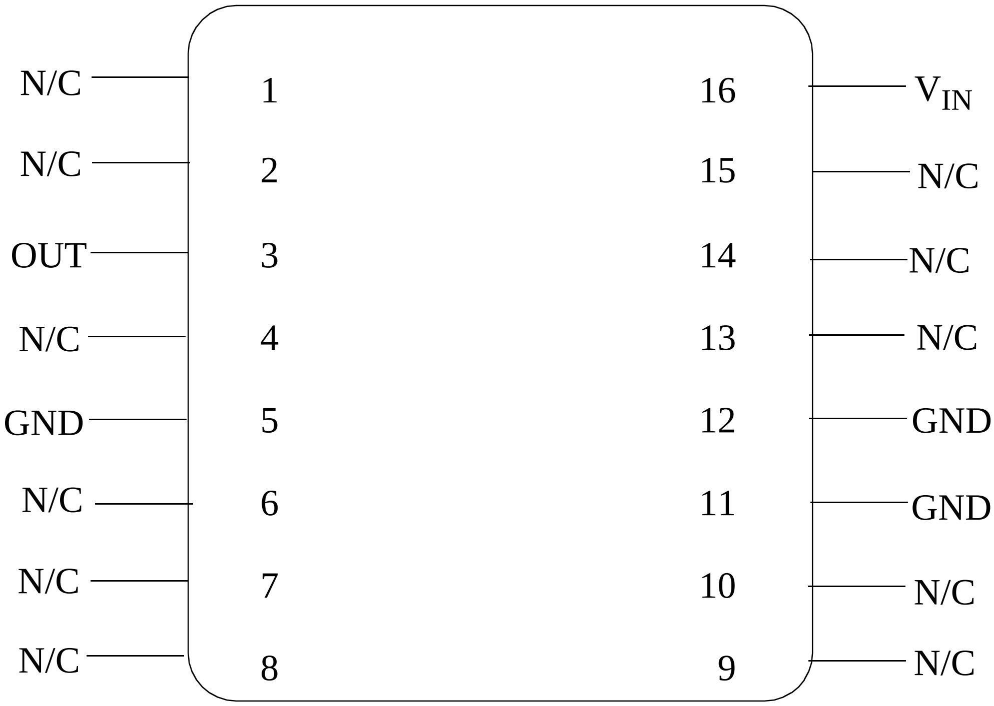
CERDIP (J),
16 LEAD

PROJECTION



SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING SHEET 1 OF 1



LM3940WG

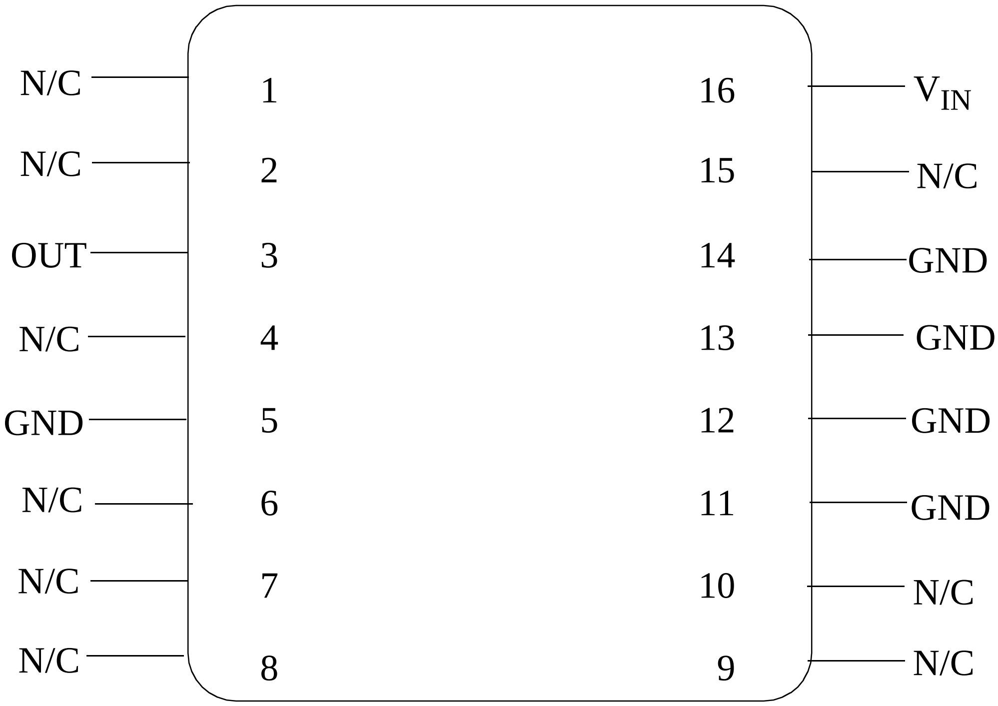
16 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM

TOP VIEW

P000377A

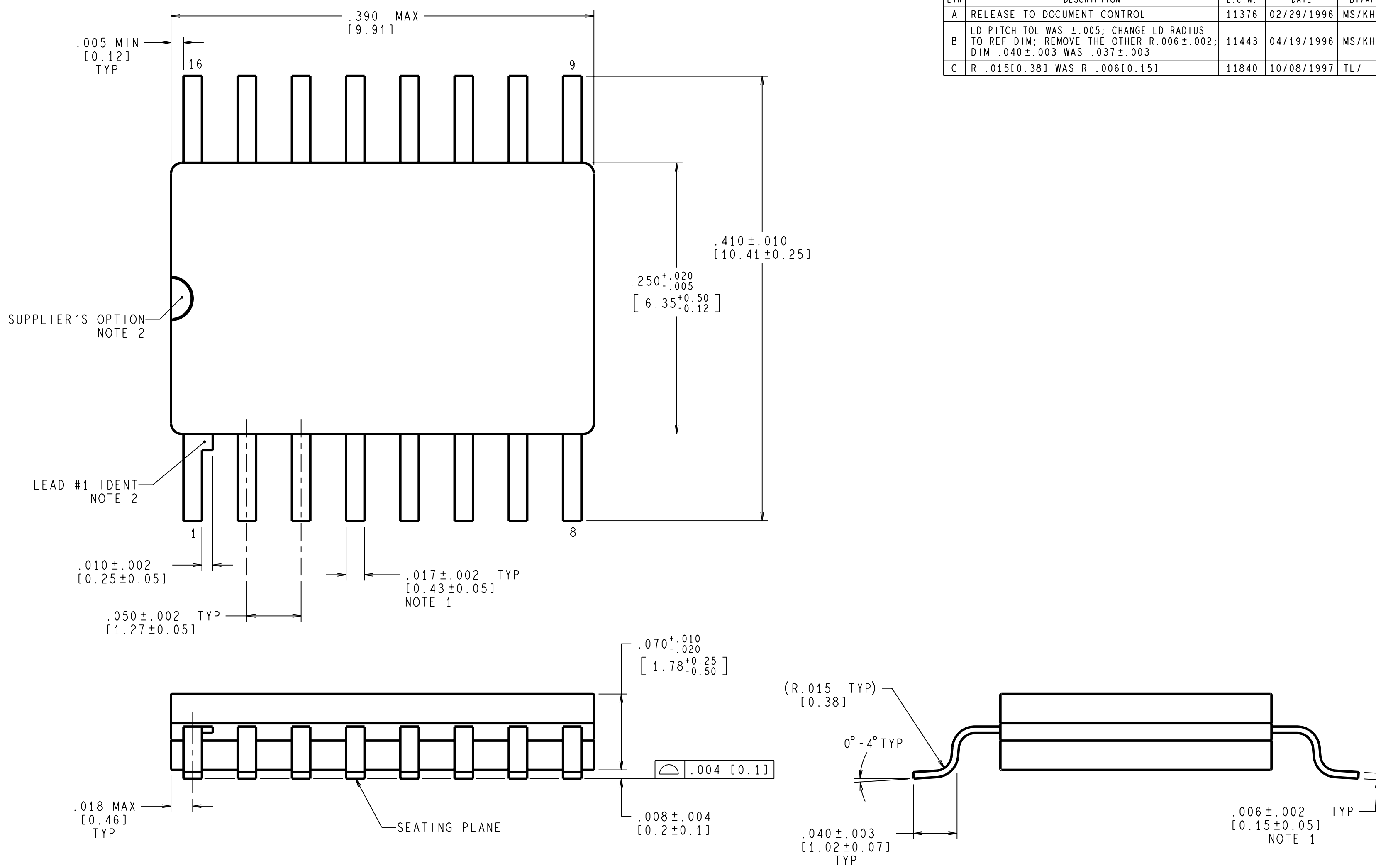
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM3940J
16 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000389A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE	National Semiconductor, 2900 Semiconductor dr., Santa Clara, CA 95052-8090
DRAWN MARTA SUCHY	02/29/96	CERPACK, 16 LEAD, GULL WING
DFTG. CHK.		
ENGR. CHK.		
PROJECTION INCH [MM]		SCALE N/A · SIZE C · DRAWING NUMBER (SC)MKT-WG16A · REV C
		DO NOT SCALE DRAWING · SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002963	11/18/98	Rose Malone	Initial Release of MDS: MNLM3940-3.3-X, Rev. 0A0.
0B0	M0003105	11/18/98	Rose Malone	Update MDS: MNLM3940-3.3-X, Rev. 0A0 to MNLM3940-3.3-X, Rev. 0B0.