

# Unidirectional Measurement Current-Shunt Monitor with Dual Comparators

## FEATURES

- **COMPLETE CURRENT SENSE SOLUTION**
- **DUAL COMPARATORS:**
  - Comparator 1 with Latch
  - Comparator 2 with Optional Delay
- **COMMON-MODE RANGE: –16V to +80V**
- **HIGH ACCURACY: 3.5% (max) OVER TEMP**
- **BANDWIDTH: 500kHz**
- **QUIESCENT CURRENT: 1.8mA**
- **PACKAGES: SO-14, TSSOP-14, MSOP-10**

## APPLICATIONS

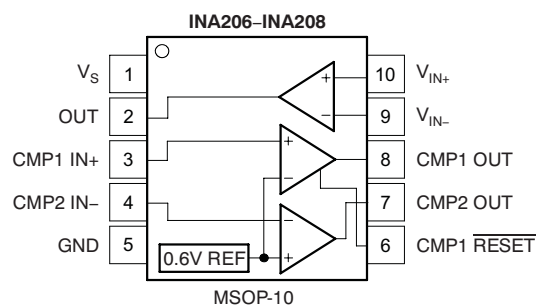
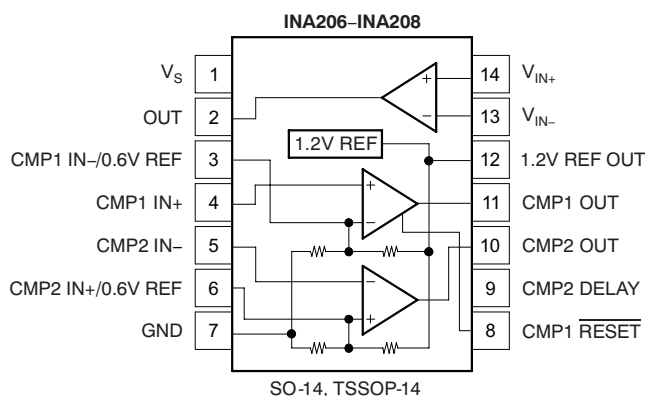
- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **TELECOM EQUIPMENT**
- **AUTOMOTIVE**
- **POWER MANAGEMENT**
- **BATTERY CHARGERS**
- **WELDING EQUIPMENT**

## DESCRIPTION

The INA206, INA207, and INA208 are a family of unidirectional current-shunt monitors with voltage output, dual comparators, and voltage reference. The INA206, INA207, and INA208 can sense drops across shunts at common-mode voltages from –16V to +80V. The INA206, INA207, and INA208 are available with three output voltage scales: 20V/V, 50V/V, and 100V/V, with up to 500kHz bandwidth.

The INA206, INA207, and INA208 also incorporate two open-drain comparators with internal 0.6V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay on 14-pin versions. 14-pin versions also provide a 1.2V reference output.

The INA206, INA207, and INA208 operate from a single +2.7V to +18V supply. They are specified over the extended operating temperature range of –40°C to +125°C.



## RELATED PRODUCTS

DEVICE	GAIN
INA206	20V/V
INA207	50V/V
INA208	100V/V

FEATURES	PRODUCT
Variant of INA206–INA208 Comparator 2 polarity	<a href="#">INA203–INA205</a>
Current-shunt monitor with single comparator and $V_{REF}$	<a href="#">INA200–INA202</a>
Current-shunt monitor only	<a href="#">INA193–INA198</a>
Current-shunt monitor with split stages for filter options	<a href="#">INA270–INA271</a>



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	GAIN	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	1.2V REF OUT	EXTERNAL COMP1 AND COMP2 REF INPUTS	INTERNAL COMP1 AND COMP2 0.6V REF	COMP2 DELAY PIN
INA206	20V/V	SO-14	D	INA206A	X	X	X	X
		MSOP-10	DGS	BQQ			X	
		TSSOP-14	PW	INA206A	X	X	X	X
INA207	50V/V	SO-14	D	INA207A	X	X	X	X
		MSOP-10	DGS	BQR			X	
		TSSOP-14	PW	INA207A	X	X	X	X
INA208	100V/V	SO-14	D	INA208A	X	X	X	X
		MSOP-10	DGS	BQS			X	
		TSSOP-14	PW	INA208A	X	X	X	X

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		INA206, INA207, INA208	UNIT
Supply Voltage, V+		18	V
Current-Shunt Monitor Analog Inputs, V <sub>IN+</sub> and V <sub>IN-</sub>	Differential (V <sub>IN+</sub> ) – (V <sub>IN-</sub> )	–18 to +18	V
	Common-Mode	–16 to +80	V
Comparator Analog Input and Reset Pins		GND – 0.3 to (V+) + 0.3	V
Analog Output, Out Pin		GND – 0.3 to (V+) + 0.3	V
Comparator Output, Out Pin		GND – 0.3 to 18	V
V <sub>REF</sub> and CMP2 Delay Pin		GND – 0.3 to 10	V
Input Current Into Any Pin		5	mA
Operating Temperature		–55 to +150	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

## ELECTRICAL CHARACTERISTICS: CURRENT-SHUNT MONITOR

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SENSE} = 100\text{mV}$ ,  $R_L = 10\text{k}\Omega$  to GND,  $R_{PULL-UP} = 5.1\text{k}\Omega$  each connected from CMP1 OUT and CMP2 OUT to  $V_S$ , and CMP1 IN+ = 1V and CMP2 IN– = GND, unless otherwise noted.

CURRENT-SHUNT MONITOR PARAMETERS		TEST CONDITIONS	INA206, INA207, INA208			UNIT
			MIN	TYP	MAX	
INPUT						
Full-Scale Sense Input Voltage	V <sub>SENSE</sub>	V <sub>SENSE</sub> = V <sub>IN+</sub> – V <sub>IN–</sub>		0.15	(V <sub>S</sub> – 0.25)/Gain	V
Common-Mode Input Range	V <sub>CM</sub>		–16		80	V
Common-Mode Rejection Ratio	CMRR	V <sub>IN+</sub> = –16V to +80V	80	100		dB
over Temperature		V <sub>IN+</sub> = +12V to +80V	100	123		dB
Offset Voltage RTI <sup>(1)</sup>	V <sub>OS</sub>			±0.5	±2.5	mV
+25°C to +125°C					±3	mV
–40°C to +25°C					±3.5	mV
vs Temperature	dV <sub>OS</sub> /dT	–40°C to +125°C		5		μV/°C
vs Power-Supply	PSR	V <sub>OUT</sub> = 2V, V <sub>IN+</sub> = 18V, 2.7V		2.5	100	μV/V
Input Bias Current, V <sub>IN–</sub> Pin	I <sub>B</sub>			±9	±16	μA
OUTPUT (V <sub>SENSE</sub> ≥ 20mV)						
Gain: INA206	G			20		V/V
Gain: INA207				50		V/V
Gain: INA208				100		V/V
Gain Error		V <sub>SENSE</sub> = 20mV to 100mV		±0.2	±1	%
over Temperature		V <sub>SENSE</sub> = 20mV to 100mV			±2	%
Total Output Error <sup>(2)</sup>		V <sub>SENSE</sub> = 120mV, V <sub>S</sub> = +16V		±0.75	±2.2	%
over Temperature		V <sub>SENSE</sub> = 120mV, V <sub>S</sub> = +16V			±3.5	%
Nonlinearity Error <sup>(3)</sup>		V <sub>SENSE</sub> = 20mV to 100mV		±0.002		%
Output Impedance	R <sub>O</sub>			1.5		Ω
Maximum Capacitive Load		No Sustained Oscillation		10		nF
OUTPUT (V <sub>SENSE</sub> < 20mV) <sup>(4)</sup>						
INA206, INA207, INA208		–16V ≤ V <sub>CM</sub> < 0V		300		mV
INA206		0V ≤ V <sub>CM</sub> ≤ V <sub>S</sub> , V <sub>S</sub> = 5V			0.4	V
INA207		0V ≤ V <sub>CM</sub> ≤ V <sub>S</sub> , V <sub>S</sub> = 5V			1	V
INA208		0V ≤ V <sub>CM</sub> ≤ V <sub>S</sub> , V <sub>S</sub> = 5V			2	V
INA206, INA207, INA208		V <sub>S</sub> < V <sub>CM</sub> ≤ 80V		300		mV
VOLTAGE OUTPUT <sup>(5)</sup>						
Output Swing to the Positive Rail		V <sub>IN–</sub> = 11V, V <sub>IN+</sub> = 12V		(V+) – 0.15	(V+) – 0.25	V
Output Swing to GND <sup>(6)</sup>		V <sub>IN–</sub> = 0V, V <sub>IN+</sub> = –0.5V		(V <sub>GND</sub> ) + 0.004	(V <sub>GND</sub> ) + 0.05	V
FREQUENCY RESPONSE						
Bandwidth: INA206	BW	C <sub>LOAD</sub> = 5pF		500		kHz
Bandwidth: INA207		C <sub>LOAD</sub> = 5pF		300		kHz
Bandwidth: INA208		C <sub>LOAD</sub> = 5pF		200		kHz
Phase Margin		C <sub>LOAD</sub> < 10pF		40		Degrees
Slew Rate				1		V/μs
Settling Time (1%)		V <sub>SENSE</sub> = 10mV <sub>PP</sub> to 100mV <sub>PP</sub> , C <sub>LOAD</sub> = 5pF		2		μs
NOISE, RTI						
Output Voltage Noise Density				40		nV/√Hz

(1) Offset is extrapolated from measurements of the output at 20mV and 100mV  $V_{SENSE}$ .

(2) Total output error includes effects of gain error and  $V_{OS}$ .

(3) Linearity is best fit to a straight line.

(4) For details on this region of operation, see the *Accuracy Variations as a Result of  $V_{SENSE}$  and Common-Mode Voltage* section in the [Applications Information](#).

(5) See Typical Characteristics curve *Output Swing vs Output Current*.

(6) Specified by design.

## ELECTRICAL CHARACTERISTICS: COMPARATOR

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{\text{IN}+} = 12\text{V}$ ,  $V_{\text{SENSE}} = 100\text{mV}$ ,  $R_L = 10\text{k}\Omega$  to GND,  $R_{\text{PULL-UP}} = 5.1\text{k}\Omega$  each connected from CMP1 OUT and CMP2 OUT to  $V_S$ , unless otherwise noted.

COMPARATOR PARAMETERS	TEST CONDITIONS	INA206, INA207, INA208			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Offset Voltage	Comparator Common-Mode Voltage = Threshold Voltage		2		mV
Offset Voltage Drift, Comparator 1			<b><math>\pm 2</math></b>		$\mu\text{V}/^{\circ}\text{C}$
Offset Voltage Drift, Comparator 2			<b><math>\pm 5.4</math></b>		$\mu\text{V}/^{\circ}\text{C}$
Threshold	$T_A = +25^{\circ}\text{C}$	590	608	620	mV
over Temperature		<b>586</b>		<b>625</b>	<b>mV</b>
Hysteresis <sup>(1)</sup> , CMP1	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		–8		mV
Hysteresis <sup>(1)</sup> , CMP2	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		8		mV
<b>INPUT BIAS CURRENT<sup>(2)</sup></b>					
CMP1 IN+, CMP2 IN–			0.005	10	nA
vs Temperature				<b>15</b>	<b>nA</b>
<b>INPUT IMPEDANCE</b>					
Pins 3 and 6 (14-pin packages only)			10		k $\Omega$
<b>INPUT RANGE</b>					
CMP1 IN+ and CMP2 IN–			0V to $V_S - 1.5\text{V}$		V
Pins 3 and 6 (14-pin packages only) <sup>(3)</sup>			0V to $V_S - 1.5\text{V}$		V
<b>OUTPUT</b>					
Large-Signal Differential Voltage Gain	CMP $V_{\text{OUT}}$ 1V to 4V, $R_L \geq 15\text{k}\Omega$ connected to 5V		200		V/mV
High-Level Output Current	$V_{\text{ID}} = 0.4\text{V}$ , $V_{\text{OH}} = V_S$		0.0001	1	$\mu\text{A}$
Low-Level Output Voltage	$V_{\text{ID}} = -0.6\text{V}$ , $I_{\text{OL}} = 2.35\text{mA}$		220	300	mV
<b>RESPONSE TIME<sup>(4)</sup></b>					
Comparator 1	$R_L$ to 5V, $C_L = 15\text{pF}$ , 100mV Input Step with 5mV Overdrive		1.3		$\mu\text{s}$
Comparator 2	$R_L$ to 5V, $C_L = 15\text{pF}$ , 100mV Input Step with 5mV Overdrive, $C_{\text{DELAY}}$ Pin Open		1.3		$\mu\text{s}$
<b>RESET</b>					
RESET Threshold <sup>(5)</sup>			1.1		V
Logic Input Impedance			2		M $\Omega$
Minimum RESET Pulse Width			1.5		$\mu\text{s}$
RESET Propagation Delay			3		$\mu\text{s}$
Comparator 2 Delay Equation <sup>(6)</sup>			$C_{\text{DELAY}} = t_D/5$		$\mu\text{F}$
Comparator 2 Delay	$t_D$		0.5		s

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator. Refer to [Figure 1](#).

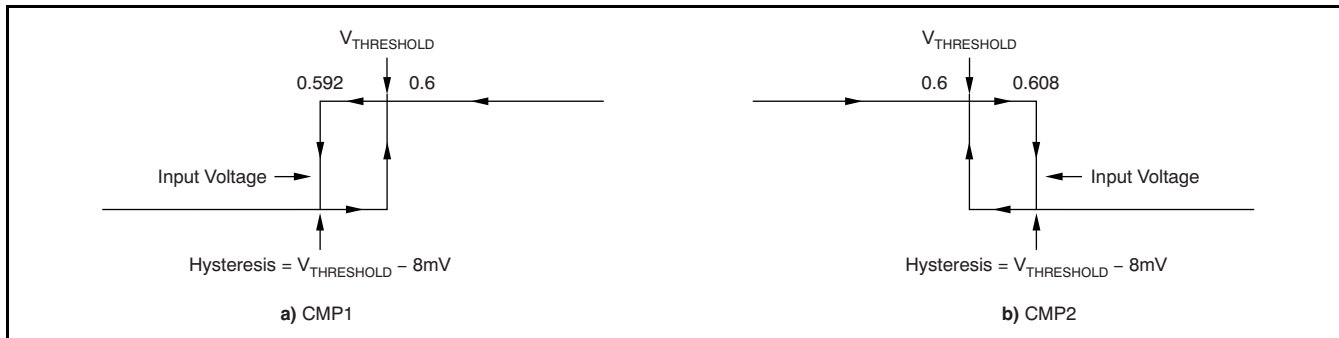
(2) Specified by design.

(3) See the [Comparator Maximum Input Voltage Range](#) section in the [Applications Information](#).

(4) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

(5) RESET input has an internal 2M $\Omega$  (typical) pull-down. Leaving RESET open results in a LOW state, with transparent comparator operation.

(6) The Comparator 2 delay applies to both rising and falling edges of the comparator output.



**Figure 1. Comparator Hysteresis**

## ELECTRICAL CHARACTERISTICS: REFERENCE

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SENSE} = 100\text{mV}$ ,  $R_L = 10\text{k}\Omega$  to GND,  $R_{PULL-UP} = 5.1\text{k}\Omega$  each connected from CMP1 OUT and CMP2 OUT to  $V_S$ , unless otherwise noted.

REFERENCE PARAMETERS	TEST CONDITIONS	INA206, INA207, INA208			UNIT
		MIN	TYP	MAX	
<b>REFERENCE VOLTAGE</b>					
1.2V <sub>REFOUT</sub> Output Voltage		1.188	1.2	1.212	V
Reference Drift $dV_{OUT}/dT$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		40	100	ppm/ $^{\circ}\text{C}$
0.6V <sub>REF</sub> Output Voltage (Pins 3 and 6 of 14-pin packages only)			0.6		V
Reference Drift $dV_{OUT}/dT$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		40	100	ppm/ $^{\circ}\text{C}$
<b>LOAD REGULATION</b> $dV_{OUT}/dI_{LOAD}$					
Sourcing	$0\text{mA} < I_{SOURCE} < 0.5\text{mA}$		0.4	2	mV/mA
Sinking	$0\text{mA} < I_{SINK} < 0.5\text{mA}$		0.4		mV/mA
<b>LOAD CURRENT</b> $I_{LOAD}$			1		mA
<b>LINE REGULATION</b> $dV_{OUT}/dV_S$	$2.7\text{V} < V_S < 18\text{V}$		30		$\mu\text{V/V}$
<b>CAPACITIVE LOAD</b>					
Reference Output Max. Capacitive Load	No Sustained Oscillations		10		nF
<b>OUTPUT IMPEDANCE</b>					
Pins 3 and 6 of 14-Pin Packages Only			10		k $\Omega$

## ELECTRICAL CHARACTERISTICS: GENERAL

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ ,  $V_{SENSE} = 100\text{mV}$ ,  $R_L = 10\text{k}\Omega$  to GND,  $R_{PULL-UP} = 5.1\text{k}\Omega$  each connected from CMP1 OUT and CMP2 OUT to  $V_S$ , and CMP1 IN+ = 1V and CMP2 IN– = GND, unless otherwise noted.

GENERAL PARAMETERS	TEST CONDITIONS	INA206, INA207, INA208			UNIT
		MIN	TYP	MAX	
<b>POWER SUPPLY</b>					
<b>Operating Power Supply</b> $V_S$		<b>+2.7</b>		<b>+18</b>	<b>V</b>
Quiescent Current $I_Q$	$V_{OUT} = 2\text{V}$		1.8	2.2	mA
<b>over Temperature</b>	<b><math>V_{SENSE} = 0\text{mV}</math></b>			<b>2.8</b>	<b>mA</b>
Comparator Power-On Reset Threshold <sup>(1)</sup>			1.5		V
<b>TEMPERATURE</b>					
Specified Temperature Range		–40		+125	$^{\circ}\text{C}$
Operating Temperature Range		–55		+150	$^{\circ}\text{C}$
Storage Temperature Range		–65		+150	$^{\circ}\text{C}$
Thermal Resistance $\theta_{JA}$					
MSOP-10 Surface-Mount			200		$^{\circ}\text{C/W}$
SO-14, TSSOP-14 Surface-Mount			150		$^{\circ}\text{C/W}$

- (1) The INA206, INA207, and INA208 are designed to power-up with the comparator in a defined reset state as long as CMP1 **RESET** is open or grounded. The comparator will be in reset as long as the power supply is below the voltage shown here. The comparator will assume a state based on the comparator input above this supply voltage. If CMP1 **RESET** is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

## TYPICAL CHARACTERISTICS

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ , and  $V_{SENSE} = 100\text{mV}$ , unless otherwise noted.

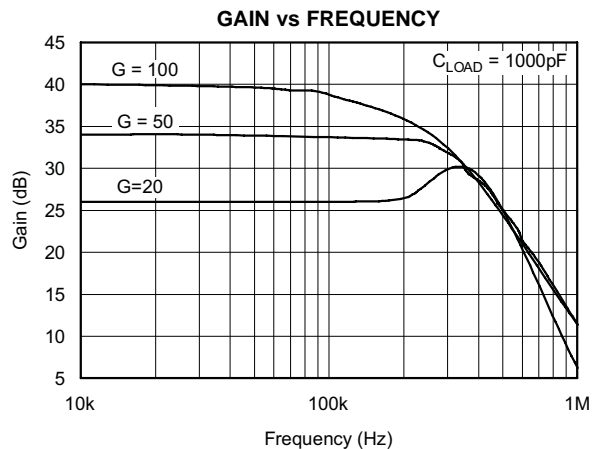


Figure 2.

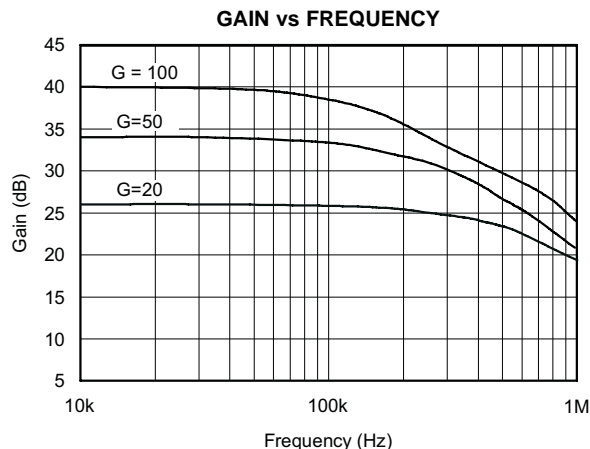


Figure 3.

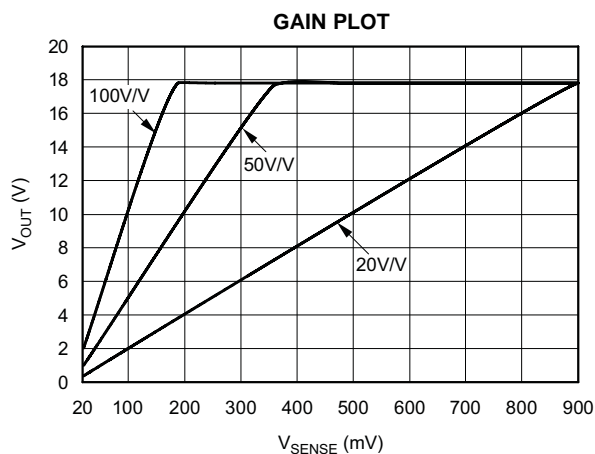


Figure 4.

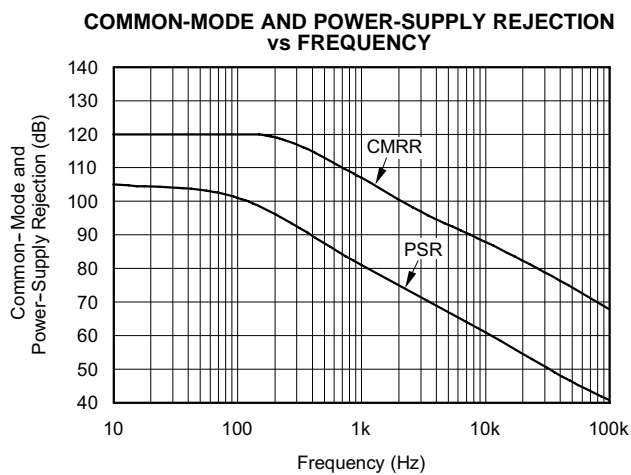


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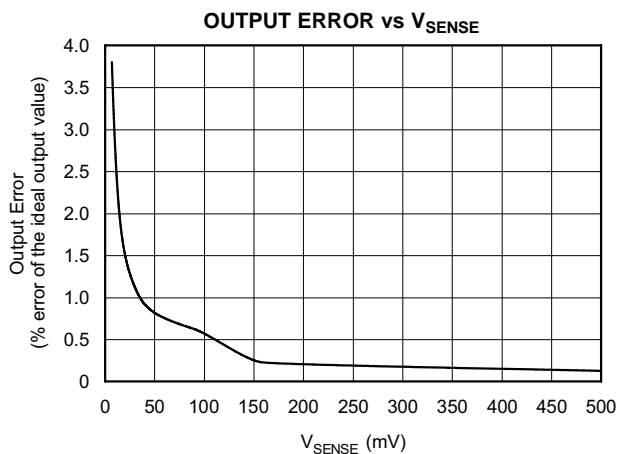


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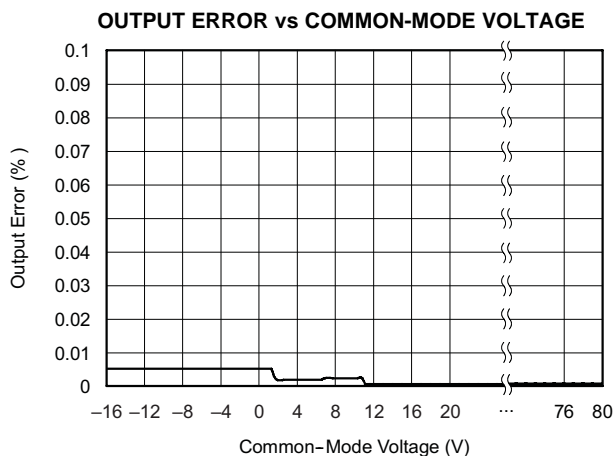


Figure 7.

## TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ , and  $V_{SENSE} = 100\text{mV}$ , unless otherwise noted.

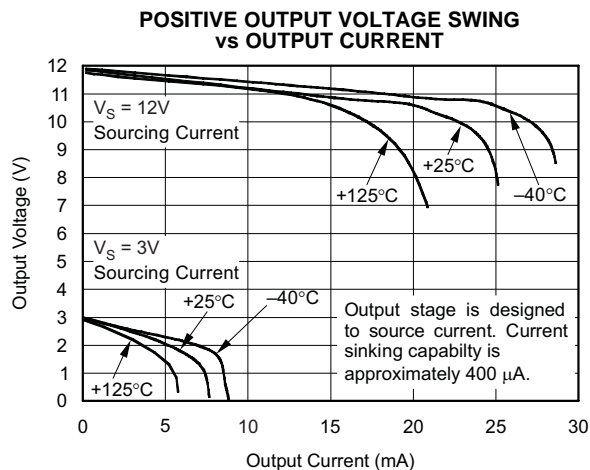


Figure 8.

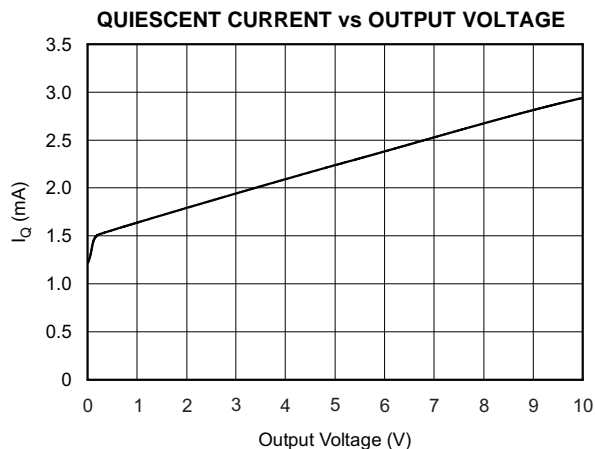


Figure 9.

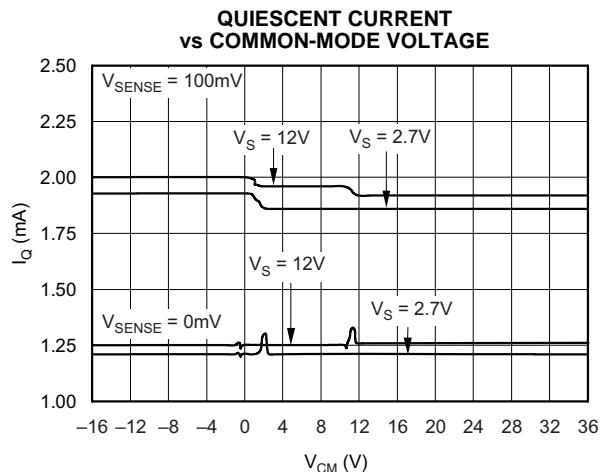


Figure 10.

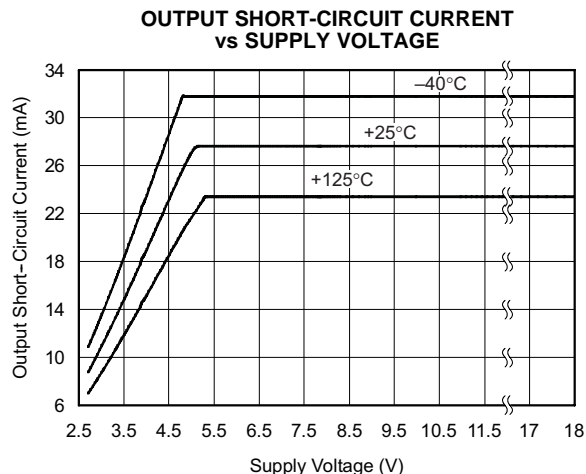


Figure 11.

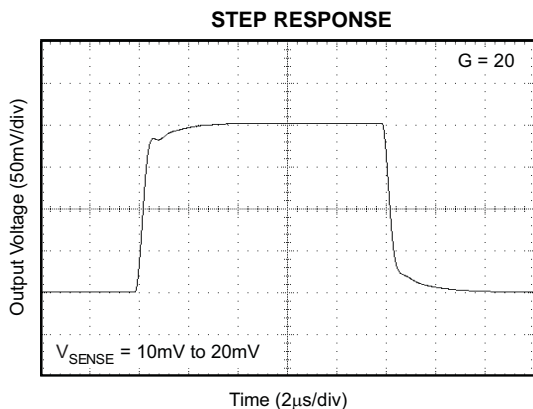


Figure 12.

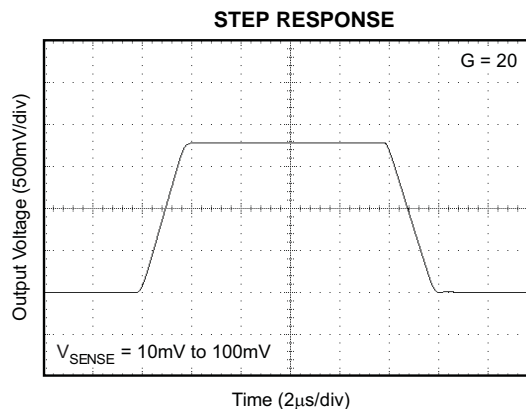
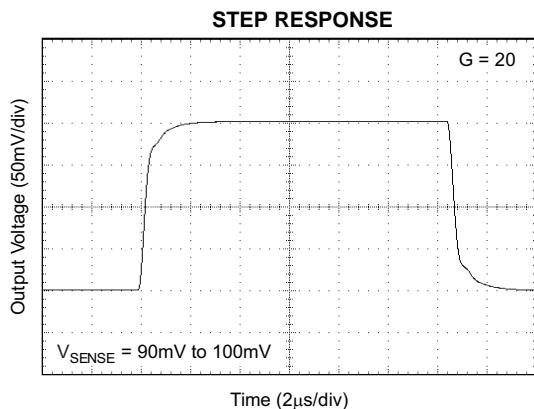


Figure 13.

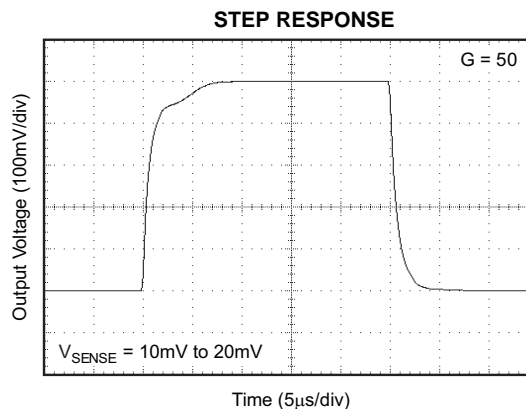


## TYPICAL CHARACTERISTICS (continued)

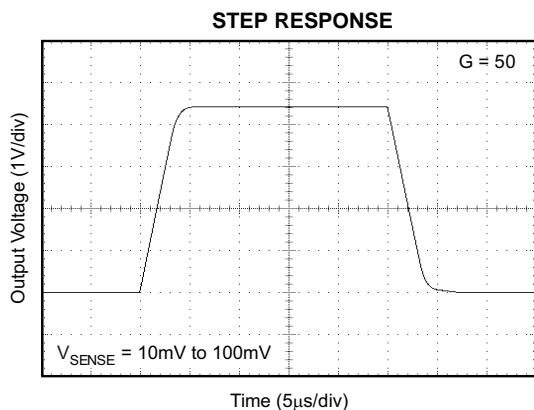
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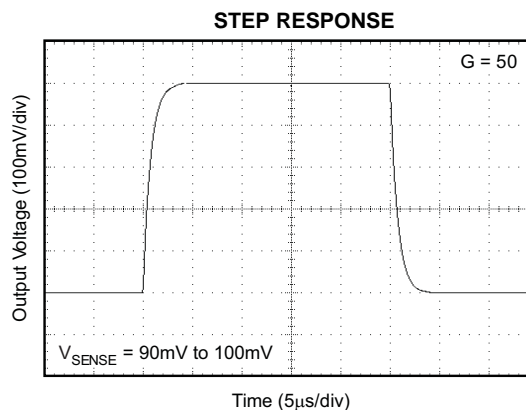
**Figure 14.**



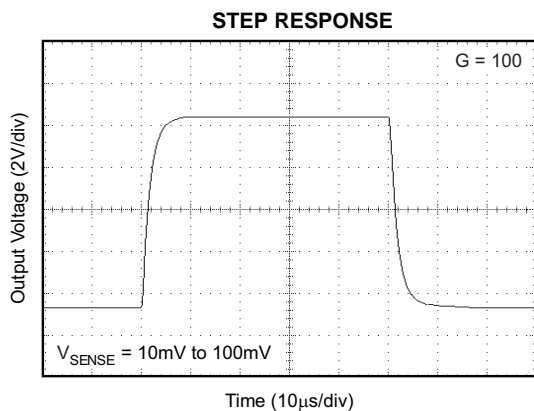
**Figure 15.**



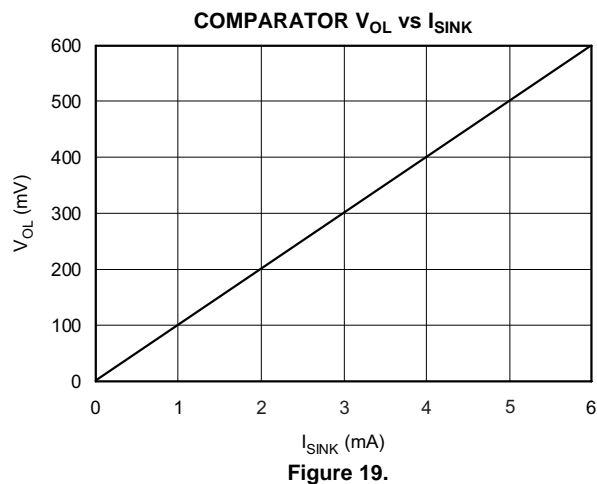
**Figure 16.**



**Figure 17.**



**Figure 18.**



**Figure 19.**

## TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ , and  $V_{SENSE} = 100\text{mV}$ , unless otherwise noted.

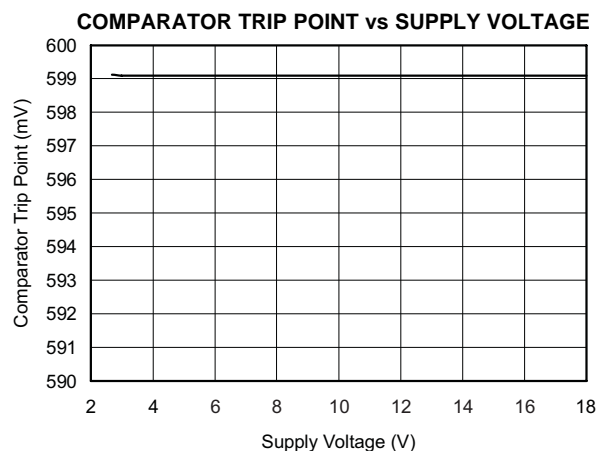


Figure 20.

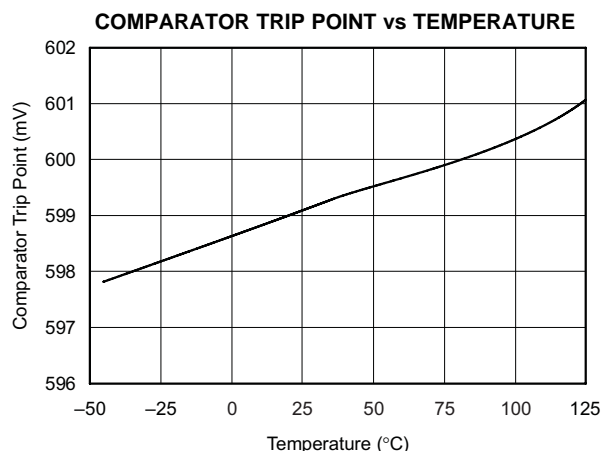


Figure 21.

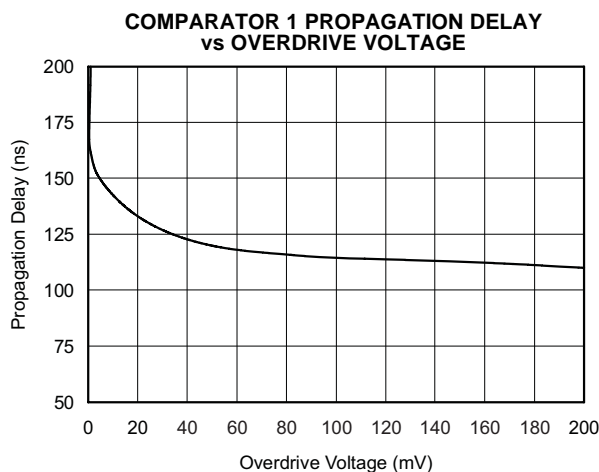


Figure 22.

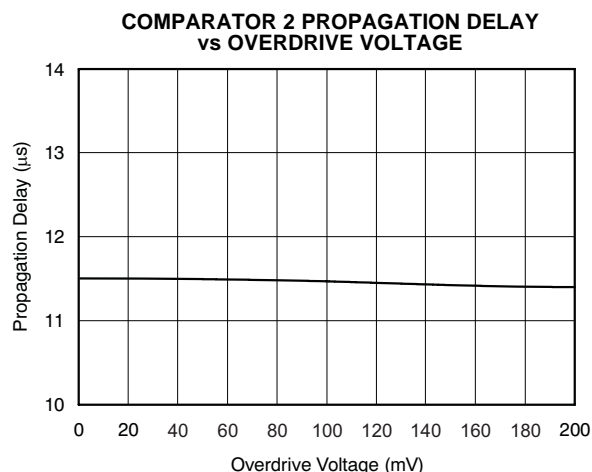


Figure 23.

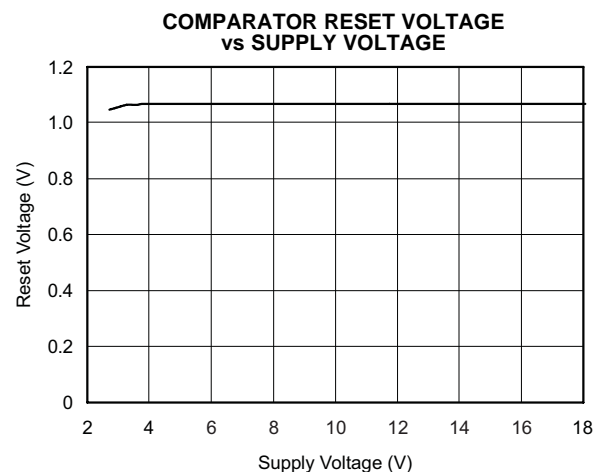


Figure 24.

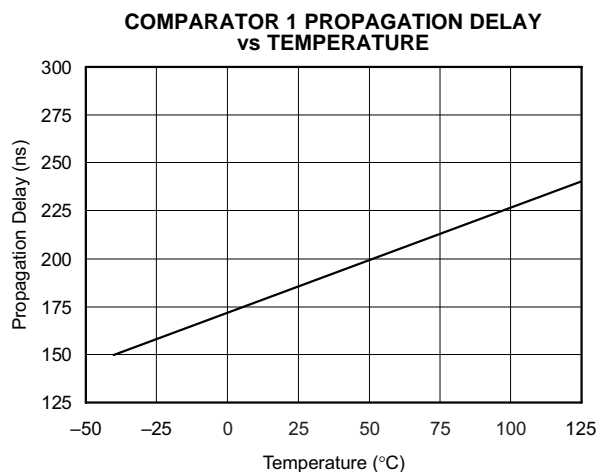


Figure 25.

## TYPICAL CHARACTERISTICS (continued)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_S = +12\text{V}$ ,  $V_{IN+} = 12\text{V}$ , and  $V_{SENSE} = 100\text{mV}$ , unless otherwise noted.

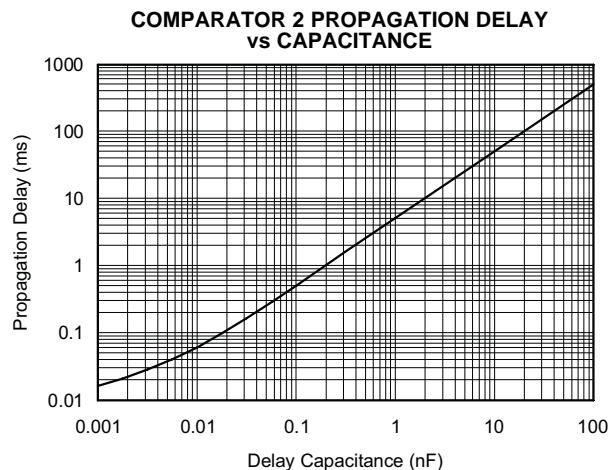


Figure 26.

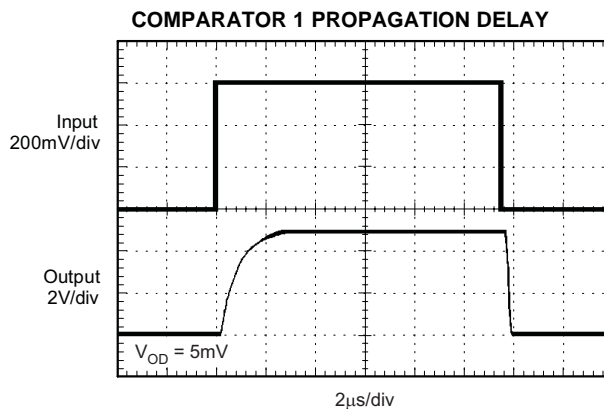


Figure 27.

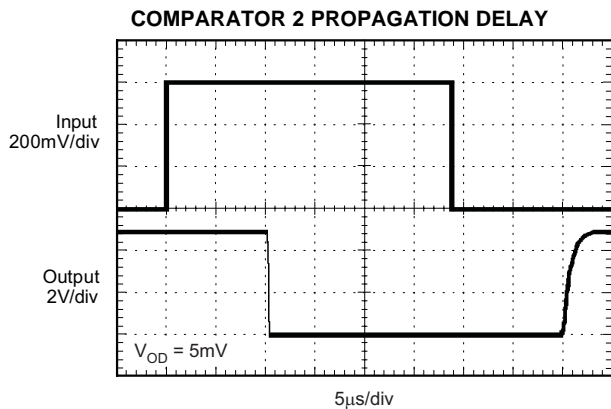


Figure 28.

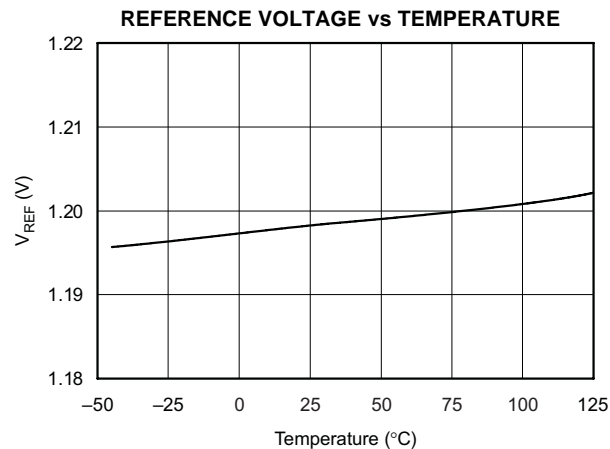


Figure 29.

## APPLICATIONS INFORMATION

### BASIC CONNECTION

Figure 30 shows the basic connection of the INA206, INA207, and INA208. The input pins,  $V_{IN+}$  and  $V_{IN-}$ , should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

### POWER SUPPLY

The input circuitry of the INA206, INA207, and INA208 can accurately measure beyond the power-supply voltage,  $V_+$ . For example, the  $V_+$  power supply can be 5V, whereas the load power-supply voltage is up to +80V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

### ACCURACY VARIATIONS AS A RESULT OF $V_{SENSE}$ AND COMMON-MODE VOLTAGE

The accuracy of the INA206, INA207, and INA208 current-shunt monitors is a function of two main variables:  $V_{SENSE}$  ( $V_{IN+} - V_{IN-}$ ) and common-mode voltage,  $V_{CM}$ , relative to the supply voltage,  $V_S$ .  $V_{CM}$  is expressed as  $(V_{IN+} + V_{IN-})/2$ ; however, in practice,  $V_{CM}$  is seen as the voltage at  $V_{IN+}$  because the voltage drop across  $V_{SENSE}$  is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1:

$$V_{SENSE} \geq 20\text{mV}, V_{CM} \geq V_S$$

Normal Case 2:

$$V_{SENSE} \geq 20\text{mV}, V_{CM} < V_S$$

Low  $V_{SENSE}$  Case 1:

$$V_{SENSE} < 20\text{mV}, -16\text{V} \leq V_{CM} < 0$$

Low  $V_{SENSE}$  Case 2:

$$V_{SENSE} < 20\text{mV}, 0\text{V} \leq V_{CM} \leq V_S$$

Low  $V_{SENSE}$  Case 3:

$$V_{SENSE} < 20\text{mV}, V_S < V_{CM} \leq 80\text{V}$$

**Normal Case 1:  $V_{SENSE} \geq 20\text{mV}, V_{CM} \geq V_S$**

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}} \quad (1)$$

where:

$V_{OUT1}$  = Output Voltage with  $V_{SENSE} = 100\text{mV}$

$V_{OUT2}$  = Output Voltage with  $V_{SENSE} = 20\text{mV}$

Then the offset voltage is measured at  $V_{SENSE} = 100\text{mV}$  and referred to the input (RTI) of the current-shunt monitor, as shown in Equation 2.

$$V_{OS\text{RTI}} (\text{Referred-To-Input}) = \left( \frac{V_{OUT1}}{G} \right) - 100\text{mV} \quad (2)$$

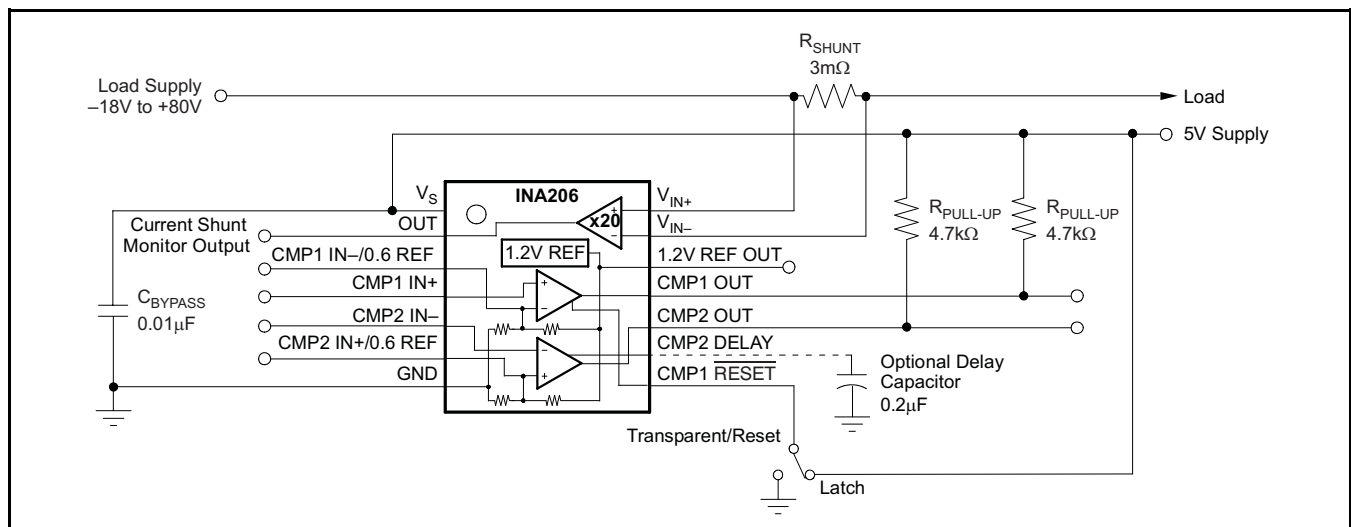


Figure 30. INA20x Basic Connection

In the Typical Characteristics, the [Output Error vs Common-Mode Voltage](#) curve shows the highest accuracy for the this region of operation. In this plot,  $V_S = 12\text{V}$ ; for  $V_{CM} \geq 12\text{V}$ , the output error is at its minimum. This case is also used to create the  $V_{SENSE} \geq 20\text{mV}$  output specifications in the [Electrical Characteristics](#) table.

#### Normal Case 2: $V_{SENSE} \geq 20\text{mV}$ , $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the [Output Error vs Common-Mode Voltage](#) curve. As noted, for this graph  $V_S = 12\text{V}$ ; for  $V_{CM} < 12\text{V}$ , the Output Error increases as  $V_{CM}$  becomes less than  $12\text{V}$ , with a typical maximum error of  $0.005\%$  at the most negative  $V_{CM} = -16\text{V}$ .

#### Low $V_{SENSE}$ Case 1:

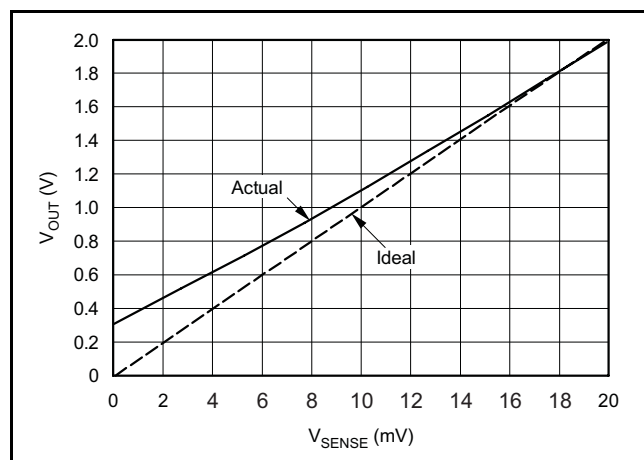
$V_{SENSE} < 20\text{mV}$ ,  $-16\text{V} \leq V_{CM} < 0$ ; and

#### Low $V_{SENSE}$ Case 3:

$V_{SENSE} < 20\text{mV}$ ,  $V_S < V_{CM} \leq 80\text{V}$

Although the INA206 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while  $V_S$  is still applied to the INA206, INA207, or INA208. It is important to know what the behavior of the devices will be in these regions.

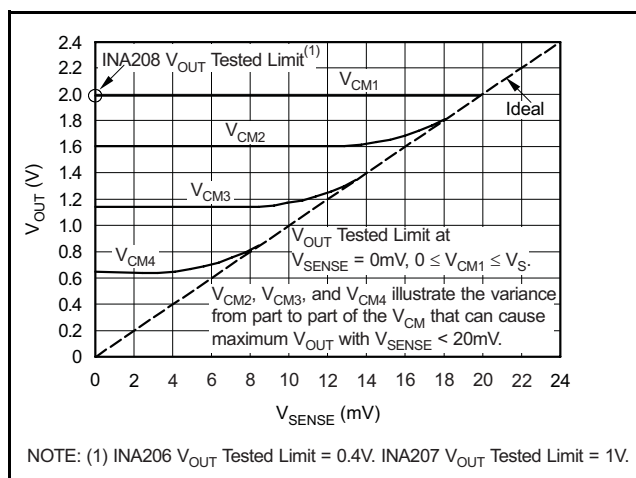
As  $V_{SENSE}$  approaches  $0\text{mV}$ , in these  $V_{CM}$  regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current-shunt monitor output with a typical maximum value of  $V_{OUT} = 300\text{mV}$  for  $V_{SENSE} = 0\text{mV}$ . As  $V_{SENSE}$  approaches  $20\text{mV}$ ,  $V_{OUT}$  returns to the expected output value with accuracy as specified in the Electrical Characteristics. [Figure 31](#) illustrates this effect using the INA208 (Gain = 100).



**Figure 31. Example for Low  $V_{SENSE}$  Cases 1 and 3 (INA208, Gain = 100)**

#### Low $V_{SENSE}$ Case 2: $V_{SENSE} < 20\text{mV}$ , $0\text{V} \leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA206 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region,  $V_{OUT}$  approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer  $V_{SENSE}$  approaches  $0\text{V}$ . Within this region, as  $V_{SENSE}$  approaches  $20\text{mV}$ , device operation is closer to that described by Normal Case 2. [Figure 32](#) illustrates this behavior for the INA208. The  $V_{OUT}$  maximum peak for this case is tested by maintaining a constant  $V_S$ , setting  $V_{SENSE} = 0\text{mV}$  and sweeping  $V_{CM}$  from  $0\text{V}$  to  $V_S$ . The exact  $V_{CM}$  at which  $V_{OUT}$  peaks during this test varies from part to part, but the  $V_{OUT}$  maximum peak is tested to be less than the specified  $V_{OUT}$  Tested Limit.



**Figure 32. Example for Low  $V_{SENSE}$  Case 2 (INA208, Gain = 100)**

#### SELECTING $R_S$

The value chosen for the shunt resistor,  $R_S$ , depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of  $R_S$  provide better accuracy at lower currents by minimizing the effects of offset, while low values of  $R_S$  minimize voltage loss in the supply line. For most applications, best performance is attained with an  $R_S$  value that provides a full-scale shunt voltage range of  $50\text{mV}$  to  $100\text{mV}$ . Maximum input voltage for accurate measurements is  $(V_S - 0.2)/\text{Gain}$ .

## TRANSIENT PROTECTION

The –16V to +80V common-mode range of the INA206, INA207, and INA208 is ideal for withstanding automotive fault conditions ranging from 12V battery reversal up to +80V transients, since no additional protective components are needed up to those levels. In the event that the INA206, INA207, and INA208 are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (zeners or *Transzorbs*) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA206, INA207, and INA208 to be exposed to transients greater than +80V (that is, allow for transient absorber tolerance, as well as additional voltage due to transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA206, INA207, and INA208 do not lend themselves to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30% but are closely matched. (If gain accuracy is not important, then resistors can be added in series with the INA206, INA207, and INA208 inputs with two equal resistors on each input.)

## OUTPUT VOLTAGE RANGE

The output of the INA206, INA207, and INA208 is accurate within the output voltage swing range set by the power supply pin, V<sub>S</sub>. This performance is best illustrated when using the INA208 (a gain of 100 version), where a 100mV full-scale input from the shunt resistor requires an output voltage swing of +10V, and a power-supply voltage sufficient to achieve +10V on the output.

## INPUT FILTERING

An obvious and straightforward location for filtering is at the output of the INA206, INA207, and INA208 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA206, INA207, and INA208, which is complicated by the internal 5kΩ + 30% input impedance; this is shown in Figure 33. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. The effect on initial gain is given by Equation 3:

$$\text{Gain Error\%} = 100 - \left( 100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{\text{FILT}}} \right) \quad (3)$$

Total effect on gain error can be calculated by replacing the 5kΩ term with 5kΩ – 30%, (or 3.5kΩ) or 5kΩ + 30% (or 6.5kΩ). The tolerance extremes of R<sub>FILT</sub> can also be inserted into the equation. If a pair of 100Ω 1% resistors are used on the inputs, the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5kΩ resistor (3.5kΩ), and the higher excursion of R<sub>FILT</sub> – 3% in this case.

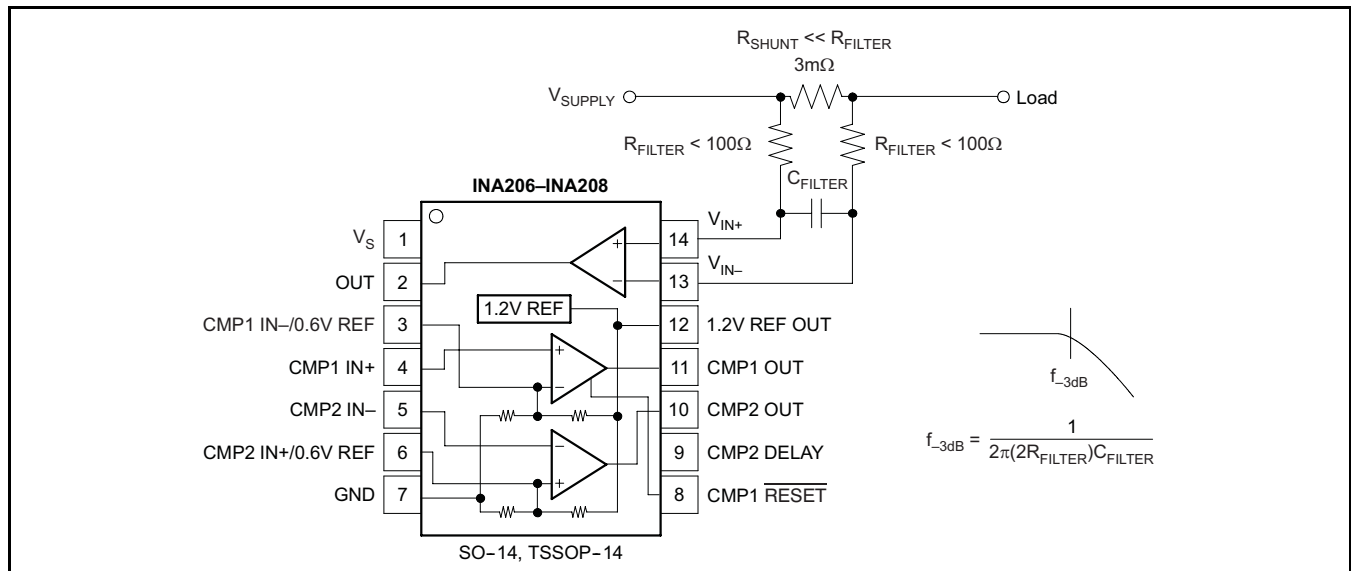


Figure 33. Input Filter (Gain Error –1.5% to –2.2%)

Note that the specified accuracy of the INA206, INA207, and INA208 must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

## REFERENCE

The INA206, INA207, and INA208 include an internal voltage reference that has a load regulation of 0.4mV/mA (typical), and not more than 100ppm/°C of drift. Only the 14-pin package allows external access to reference voltages, where voltages of 1.2V and 0.6V are both available. Output current versus output voltage is illustrated in the [Typical Characteristics](#) section.

## COMPARATOR

The INA206, INA207, and INA208 devices incorporate two open-drain comparators. These comparators typically have 2mV of offset and a 1.3μs (typical) response time. The output of Comparator 1 latches and is reset through the CMP1 RESET pin, as shown in [Figure 35](#). This configuration applies to both the 10- and 14-pin versions. [Figure 34](#) illustrates the comparator delay.

The 14-pin versions of the INA206, INA207, and INA208 include additional features for comparator functions. The comparator reference voltage of both Comparator 1 and Comparator 2 can be overridden by external inputs for increased design flexibility. Comparator 2 has a programmable delay.

## COMPARATOR DELAY (14-Pin Version Only)

The Comparator 2 programmable delay is controlled by a capacitor connected to the CMP2 Delay Pin; see [Figure 30](#). The capacitor value (in μF) is selected by using [Equation 4](#):

$$C_{\text{DELAY}} \text{ (in } \mu\text{F)} = \frac{t_D}{5} \quad (4)$$

A simplified version of the delay circuit for Comparator 2 is shown in [Figure 34](#). The delay comparator consists of two comparator stages with the delay between them. Note that I1 and I2 cannot be turned on simultaneously; I1 corresponds to a U1 low output and I2 corresponds to a U1 high output. Using an initial assumption that the U1 output is low, I1 is on, then U2 +IN is zero. If U1 goes high, I2 supplies 120nA to C<sub>DELAY</sub>. The voltage at U2 +IN begins to ramp toward a 0.6V threshold. When the voltage crosses this threshold, the U2 output goes high while the voltage at U2 +IN continues to ramp up to a maximum of 1.2V when given sufficient time (twice the value of the delay specified for C<sub>DELAY</sub>). This entire sequence is reversed when the comparator outputs go low, so that returning to low exhibits the same delay.

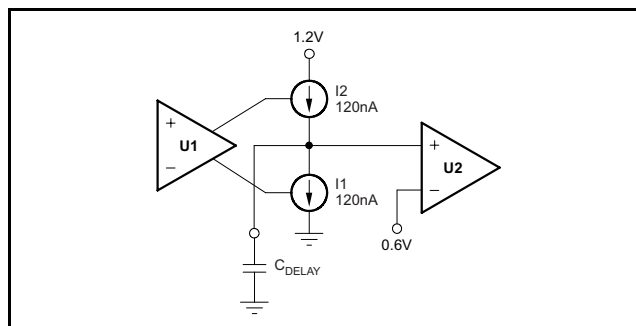


Figure 34. Simplified Model of the Comparator 2 Delay Circuit

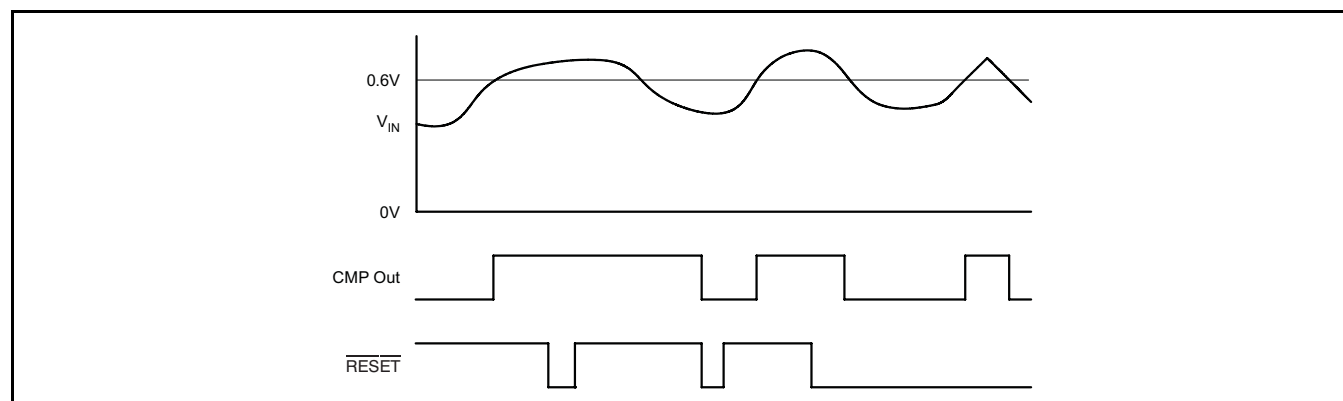


Figure 35. Comparator 1 Latching Capability



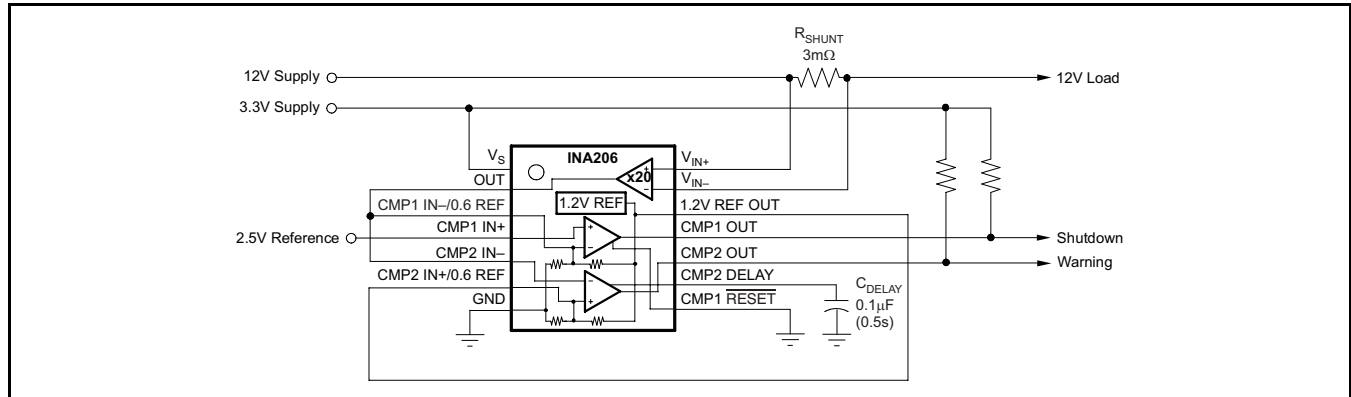


Figure 36. Server 12V Supply Current Monitor

It is important to note what will happen if events occur more rapidly than the delay timeout; for example, when the U1 output goes high (turning on I2), but returns low (turning I1 back on) prior to reaching the 0.6V transition for U2. The voltage at U2 +IN ramps back down at a rate determined by the value of  $C_{DELAY}$ , and only returns to zero if given sufficient time.

In essence, when analyzing Comparator 2 for behavior with events more rapid than its delay setting, use the model shown in Figure 34.

### COMPARATOR MAXIMUM INPUT VOLTAGE RANGE

The maximum voltage at the comparator input for normal operation is up to  $(V+) - 1.5V$ . There are special considerations when overdriving the reference inputs (pins 3 and 6). Driving either or both inputs high enough to drive 1mA back into the reference introduces errors into the reference. Figure 37 shows the basic input structure. A general guideline is to

limit the voltage on both inputs to a total of 20V. The exact limit depends on the available voltage and whether either or both inputs are subject to the large voltage. When making this determination, consider the 20kΩ from each input back to the comparator. Figure 38 shows the maximum input voltage that avoids creating a reference error when driving both inputs (an equivalent resistance back into the reference of 10kΩ).

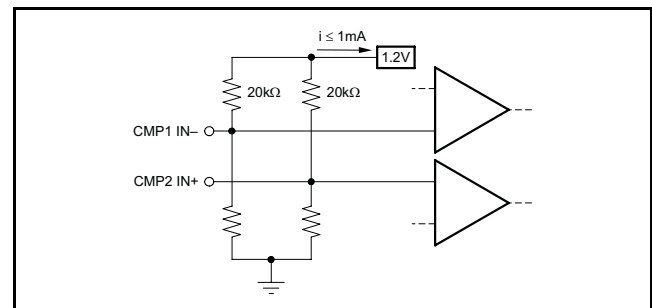


Figure 37. Limit Current Into Reference  $\leq 1mA$

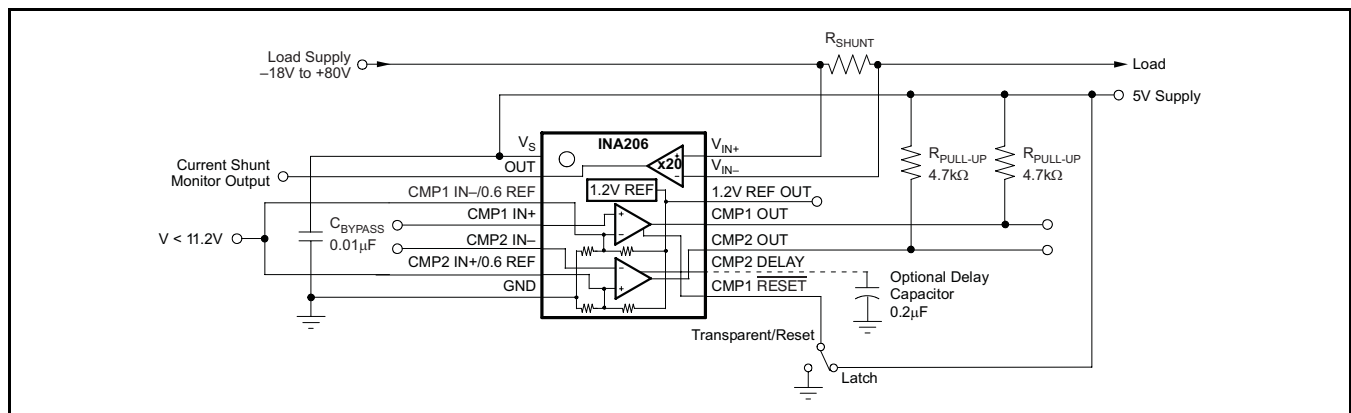


Figure 38. Overdriving Comparator Inputs Without Generating a Reference Error



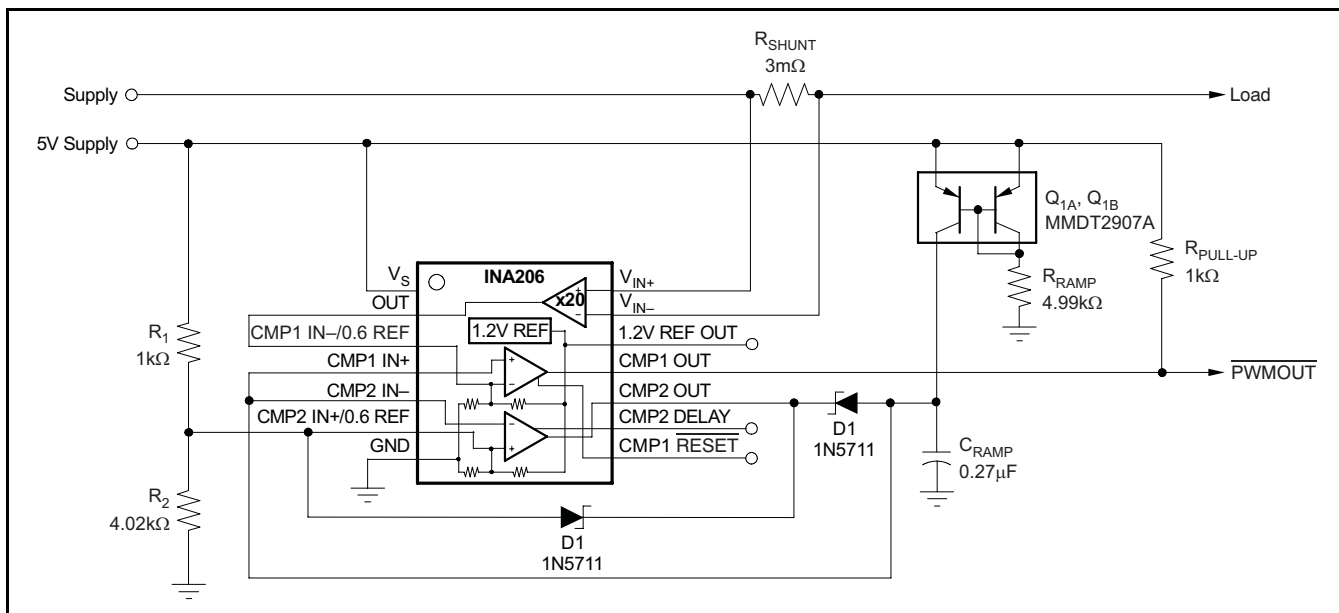


Figure 39. PWM Output Current-Shunt Monitor

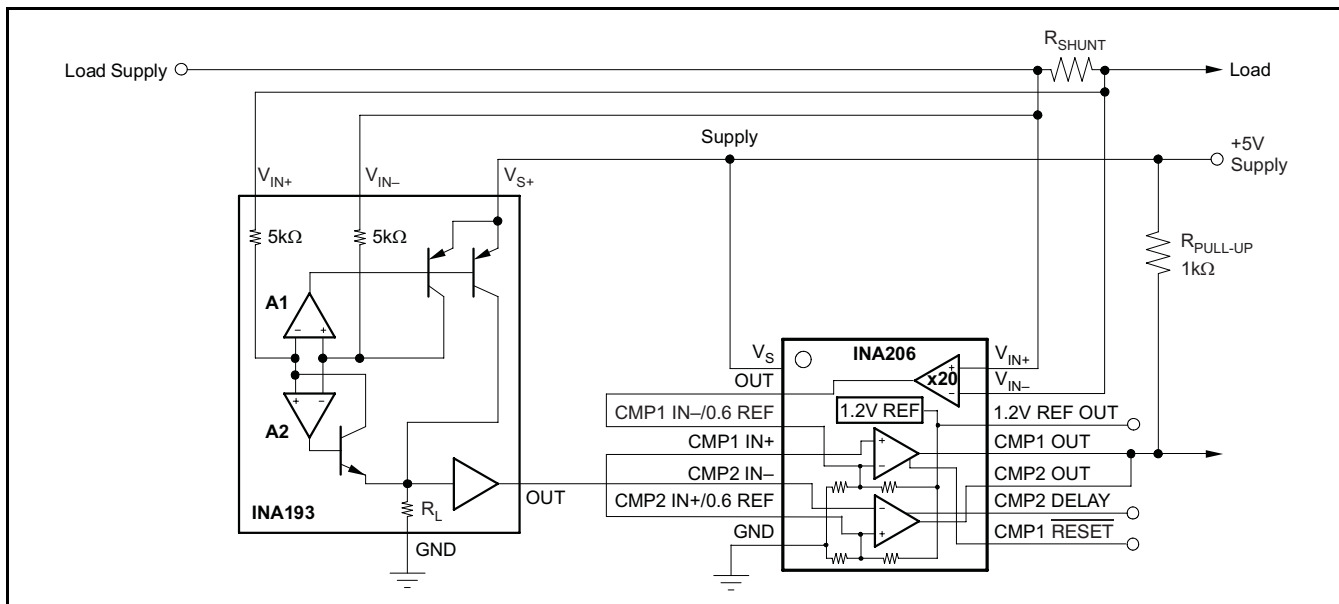
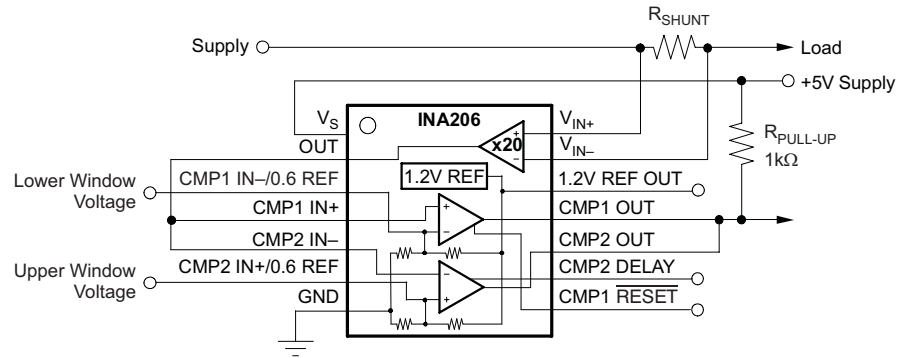
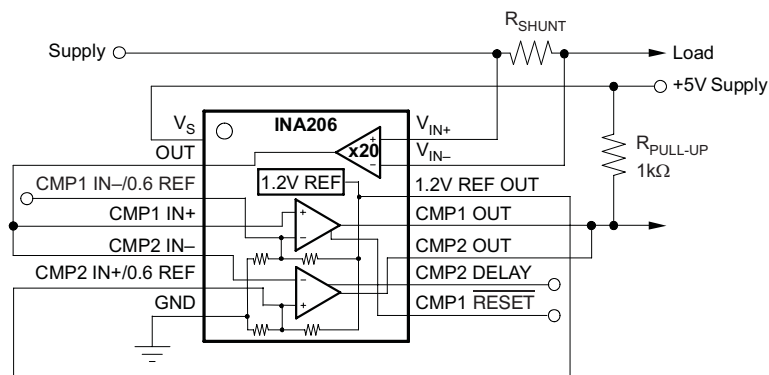


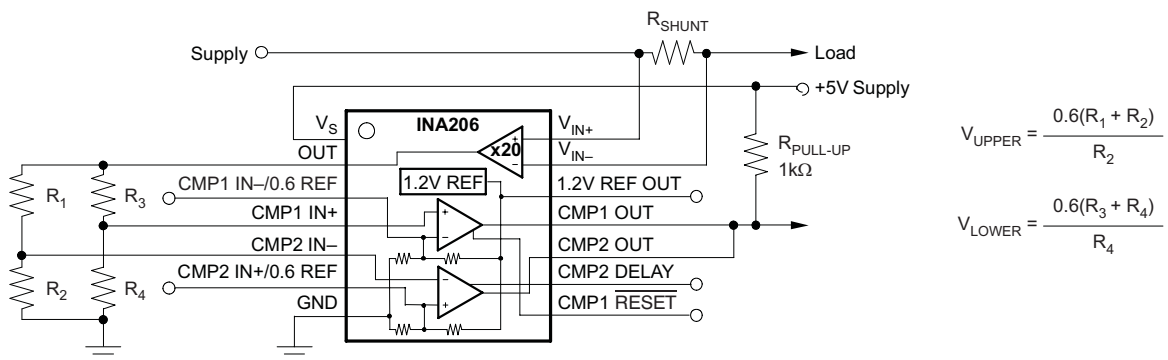
Figure 40. Bi-Directional Current Comparator



a) Generic Window Comparator

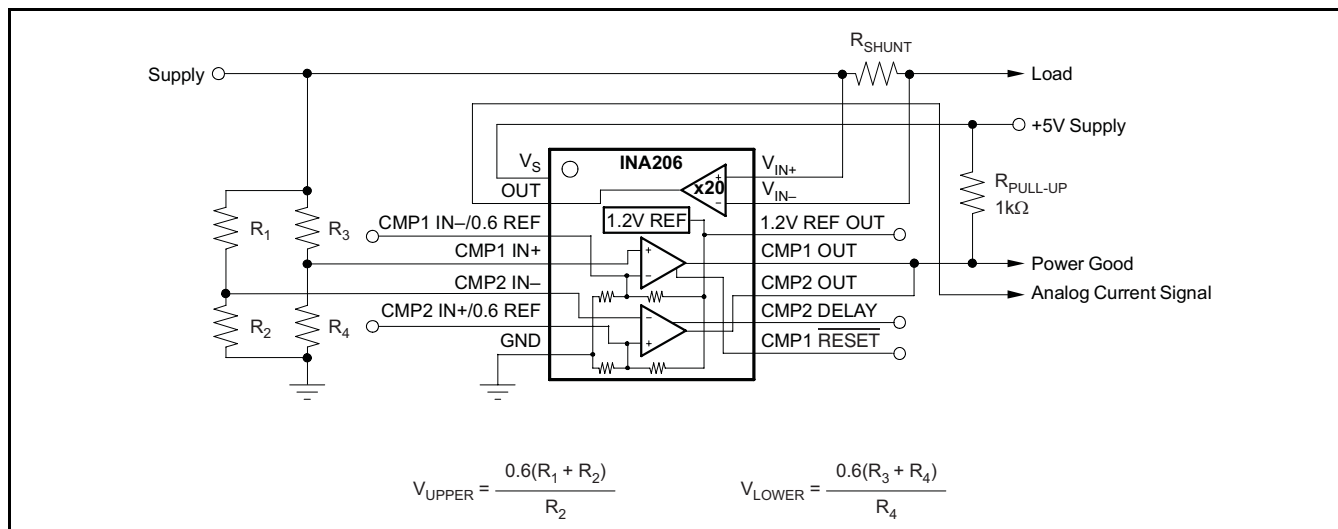


b) Window Comparator with +1.2V Upper Limit and +0.6V Lower Limit



c) Window Comparator with Individual Dividers

Figure 41. Using the INA206, INA207, and INA208 as Window Comparators



**Figure 42. Analog Output Current-Shunt Monitor with Comparators Used as Power-Supply Under-Limit/Over-Limit or Power-Good Detector**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA206AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA206AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA206AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQQ	<a href="#">Samples</a>
INA206AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQQ	<a href="#">Samples</a>
INA206AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQQ	<a href="#">Samples</a>
INA206AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA206AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA206AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA206AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA206A	<a href="#">Samples</a>
INA207AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A	<a href="#">Samples</a>
INA207AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A	<a href="#">Samples</a>
INA207AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQR	<a href="#">Samples</a>
INA207AIDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQR	<a href="#">Samples</a>
INA207AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQR	<a href="#">Samples</a>
INA207AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQR	<a href="#">Samples</a>
INA207AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A	<a href="#">Samples</a>
INA207AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA207A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA208AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A	<a href="#">Samples</a>
INA208AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A	<a href="#">Samples</a>
INA208AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQS	<a href="#">Samples</a>
INA208AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQS	<a href="#">Samples</a>
INA208AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQS	<a href="#">Samples</a>
INA208AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A	<a href="#">Samples</a>
INA208AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A	<a href="#">Samples</a>
INA208AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA208A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA206AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA206AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA206AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA206AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA207AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA207AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA207AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA208AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA208AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA208AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
INA208AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA206AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA206AIDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA206AIDR	SOIC	D	14	2500	367.0	367.0	38.0
INA206AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA207AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
INA207AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
INA207AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
INA208AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
INA208AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
INA208AIDR	SOIC	D	14	2500	367.0	367.0	38.0
INA208AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0



## DGS (S-PDSO-G10)

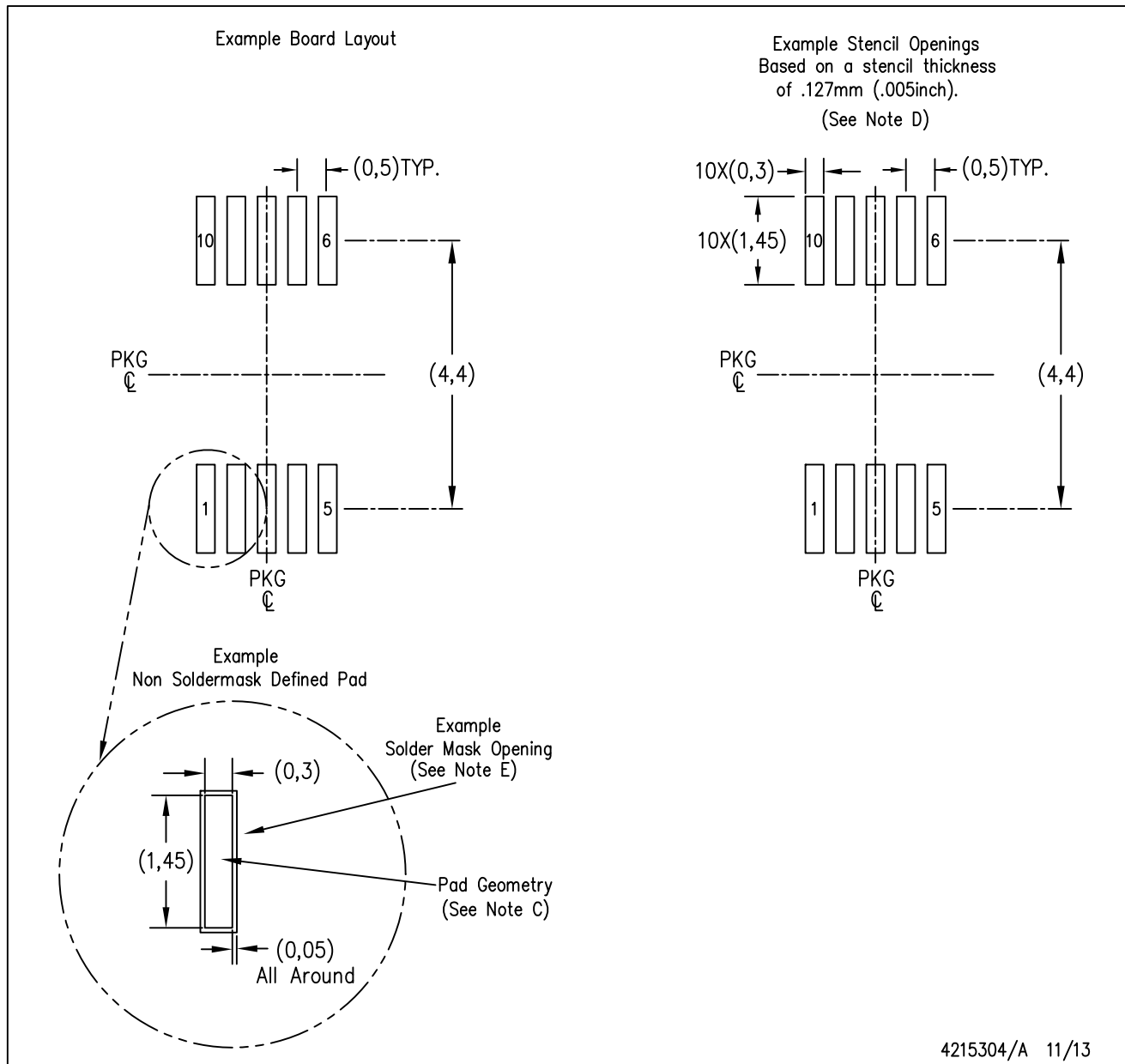
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

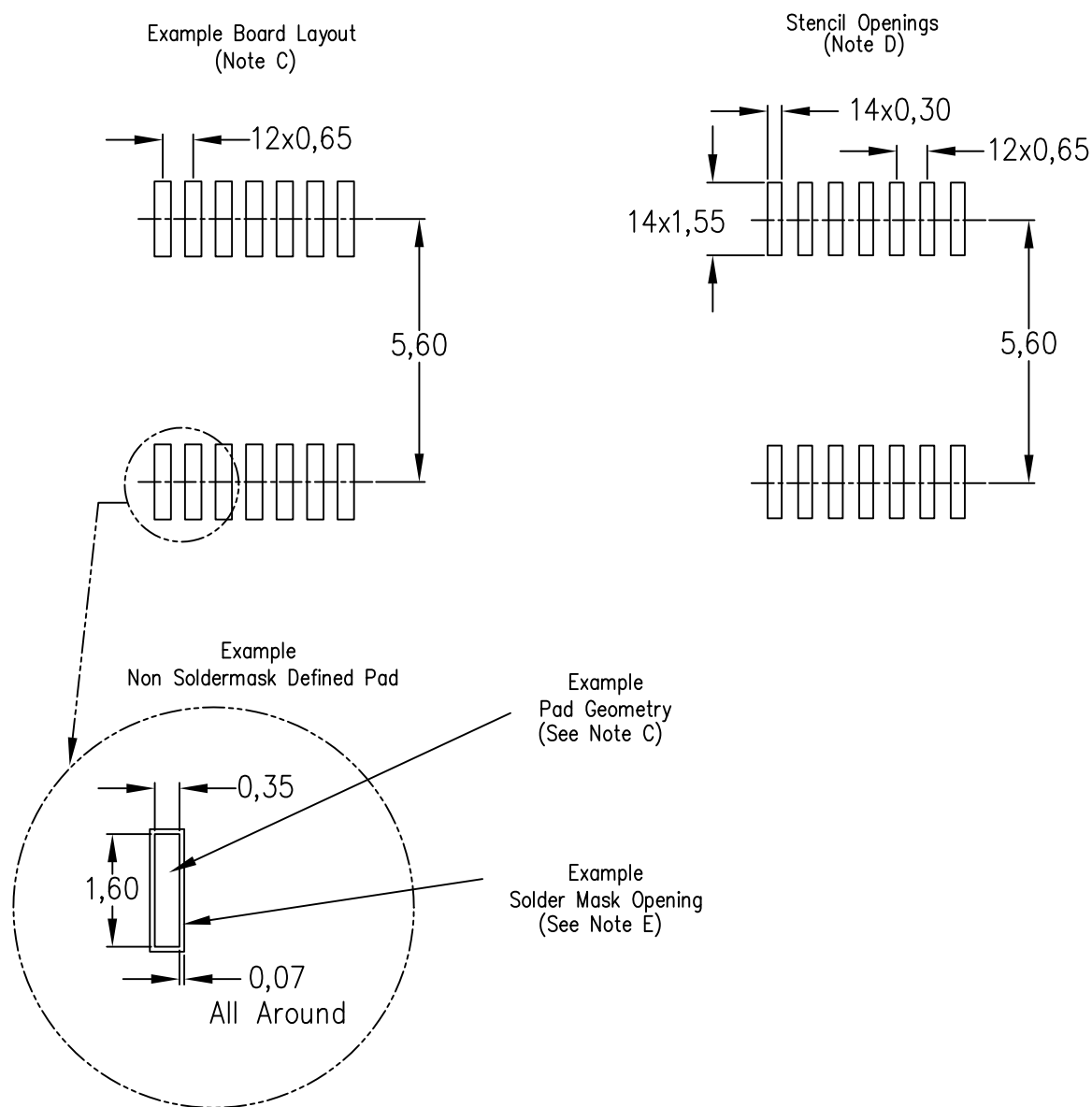
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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