Dynamic Shift Registers

MM4001A/MM5001A dual 64-bit dynamic shift register
MM4010A/MM5010A dual 64-bit accumulator

general description

The MM4001A/MM5001A dual 64-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of two 64-bit registers with independent two phase clocks and is guaranteed to operate at a 2.5 MHz operating frequency for CRT display applications.

The MM4010A/MM5010A is a dual accumulator function capable of operating at very high frequency. The device is also constructed on a single silicon chip utilizing MOS P-channel enhancement transistors. With the recirculate control line at an MOS logic "0" state, the device functions as an accumulator. A logic "1" state at the recirculate control line allows external information to enter the register serially. It is important to note that recirculation of data is performed internally, independent of the output circuit thus making it insensitive to output loading.

features

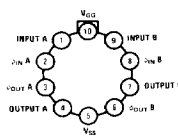
- High frequency operation — 3.3 MHz typ
- Low power consumption — 0.4 mW/bit at 1 MHz
- DTL/TTL compatibility — +5V, −12V power supplies, push-pull output stage
- Minimum operating frequency — guaranteed 250 Hz at 25°C
- Application versatility — "Split clock" operation, independent control of each register for MM4001A/MM5001A

applications

- Business machine
- CRT refresh memory
- Delay line memory
- Arithmetic operations

connection diagrams

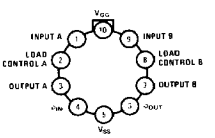
Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4001AH or MM5001AH
See Package 24

Metal Can Package



Note: Pin 5 connected to case.
TOP VIEW

Order Number MM4010AH or MM5010AH
See Package 24

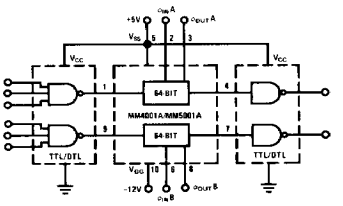
load control truth table

MM4010A/MM5010A

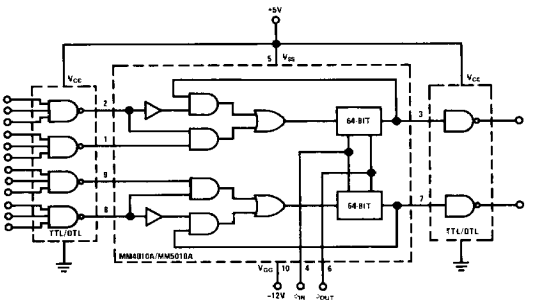
LOGICAL HIGH LEVEL (V_{LCH})	LOGICAL LOW LEVEL (V_{LCL})
Recirculates "old" data	Loads "new" data

typical applications

MM4001A/MM5001A TTL/MOS Interface



MM4010A/MM5010A TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range	
MM4010A/MM4001A	−55°C to +125°C
MM5010A/MM5001A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{LCH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{LCL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Load Control Input Leakage	V_{IN} = −20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND				
	MM4001A/MM5001A Note 2		17	20	pF
	MM4010A/MM5010A		34	40	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
	ϕ_f = 1 MHz		3.0	4.5	mA
	ϕ_f = 2.5 MHz		5.0	7.0	mA
Clock Frequency (ϕ_f)	ϕt_r = ϕt_f = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	ϕt_f + ϕ_{PW} + ϕt_r ≤ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	ϕt_f + ϕ_{PW} + ϕt_r < 10.5 μs			1	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Control Input Setup Time (t_{LCS})		80	30		ns
Load Control Input Hold Time (t_{LCh})		20	0		ns
Data Output Propagation Delay From ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

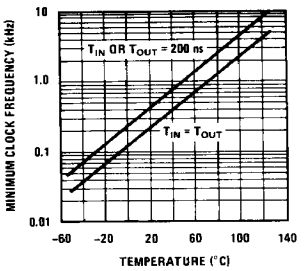
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

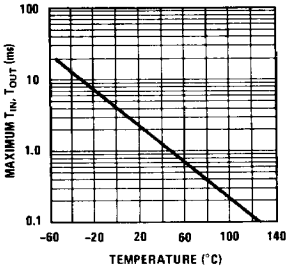
Note 2: Capacitance is guaranteed by lot sample testing.

performance characteristics

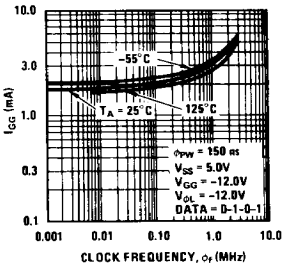
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



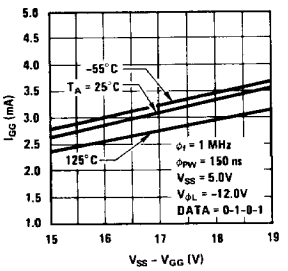
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



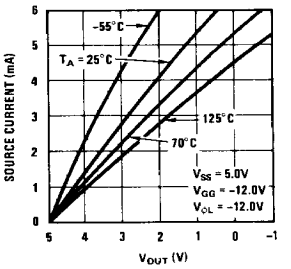
Typical Power Supply Current vs Clock Frequency



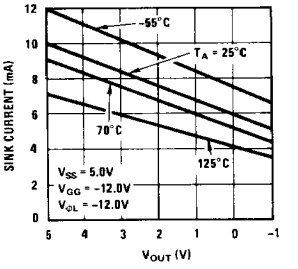
Typical Power Supply Current vs Voltage



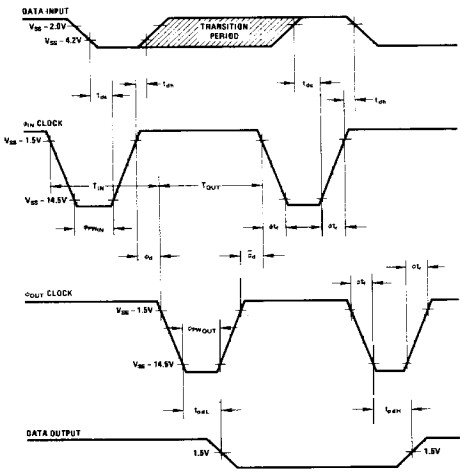
Typical Data Output Source Current vs Data Output Voltage



Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit