ANALOG DEVICES

LC²MOS
Complete 12-Bit DAC with DSP Interface
AD7848

FEATURES

Complete DAC with DSP Interface, Comprising:
- **12-Bit Voltage Mode DAC**
- **3 V Zener Reference**
- **Output Buffer Amplifier with 4 μs Settling Time**
- **8 Word FIFO and Interface Logic**

72 dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS320C25, TMS32010
42 ns min $\overline{WR}$ Pulse Width
Low Power −60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Synthesis
High Speed Modems
DSP Servo Control When Used with AD7878

GENERAL DESCRIPTION

The AD7848 is a fast, complete, 12-bit, voltage output D/A converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

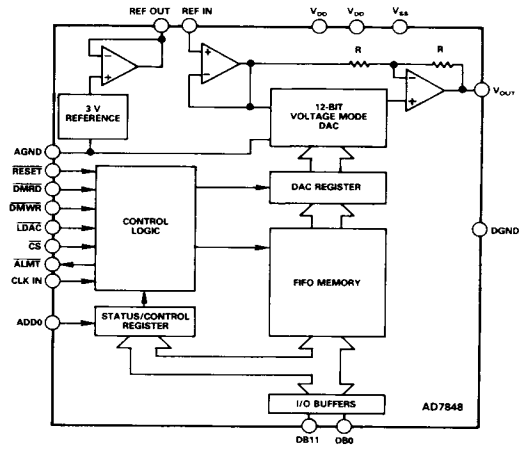
The FIFO memory allows up to eight samples to be loaded to the AD7848 at full microprocessor speed. The samples are then loaded to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 20 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains FIFO empty, FIFO full and FIFO word count information.

The analog output from the AD7848 provides a bipolar output range of ±3 V. Full power output signals up to 20 kHz can be created and the AD7848 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion.

The AD7848 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology, process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic and hermetic dual-in-line package (DIP) and in a 28-terminal plastic leaded chip carrier (PLCC).

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Complete D/A Function with DSP Interface
   The AD7848 provides the complete function for creating ac signals to 12-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 12-bit D/A converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing peripherals in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7848 is fully specified and tested for ac parameters, including signal-to-noise ratio and harmonic distortion.
3. Fast Microprocessor Interface
   Data setup times of 20 ns and write pulse widths of 42 ns make the AD7848 compatible with all modern 16-bit microprocessors and digital signal processors. Key digital timing parameters are also tested and specified over the full operating temperature range.

AD7848—SPECIFICATIONS

(V_{DD} = 5 V±5%, V_{SS} = −5 V±5%, AGND = DGND = 0V, REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF, f_{CLK} = 10 MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions[1]	K, B Versions	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to Noise Ratio[3] (SNR) @ +25°C	70	72	dB min	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	70	dB min	Typically 72 dB at +25°C for 0<f_{OUT}<20 kHz[4]
Total Harmonic Distortion (THD)	−80	−80	dB typ	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
				Typically −80 dB at +25°C for 0<f_{OUT}<20 kHz[4]
Peak Harmonic or Spurious Noise	−80	−80	dB typ	f_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
				Typically −80 dB at +25°C for 0<f_{OUT}<20 kHz[4]
DC ACCURACY				
Resolution	12	12	Bits	
Relative Accuracy	±1	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	LSB typ	Guaranteed Monotonic
Bipolar Zero Error	±4	±4	LSB max	
Positive Full-Scale Error [5]	±4	±4	LSB max	
Negative Full-Scale Error[5]	±4	±4	LSB max	
REFERENCE OUTPUT[6]				
REF OUT	3	3	V nom	
REF OUT Error @ +25°C	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT				
REF IN	2.85	2.85	V min	
	3.15	3.15	V max	
Input Current	±1	±1	μA max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V±5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V±5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	pF max	
Input Coding	2s Complement			
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	2.7	2.7	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating State Leakage Current	10	10	μA max	
Floating State Output Capacitance[7]	15	15	pF max	
ANALOG OUTPUT				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.2	0.2	Ω typ	
Short Circuit Current	25	25	mA typ	
AC CHARACTERISTICS[7]				
Voltage Output Settling Time[8]				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	μs max	
Negative Full-Scale Change	4	4	μs max	
Digital-to-Analog Glitch Impulse[8]	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough[8]	2	2	nV secs typ	
CLK IN Feedthrough	2	2	mV typ	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = Data Inputs = 5 V; Output Unloaded
I_{SS}	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = Data Inputs = 5 V; Output Unloaded
Power Dissipation	95	95	mW max	Typically 60 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions, 0 to +70°C; A, B Versions, −25°C to +85°C.
[2]V_{OUT} = ±3 V.
[3]SNR includes distortion and noise components.
[4]Using external sample-and-hold (see Testing the AD7848).
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Sample tested @ +25°C to ensure compliance.
[8]Measured with CLK IN stopped.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V±5%, V_{SS} = −5 V±5%, AGND=DGND=0 V)

Parameter	Limit at T_{min}, T_{max} (J, A, Versions)	Limit at T_{min}, T_{max} (K, B Versions)	Units	Conditions/Comments
t_1	42	42	ns min	INTERNAL WRITE Pulse Width
t_2	5	5	ns min	ADD0 to INTERNAL WRITE Setup Time
t_3	0	0	ns min	ADD0 to INTERNAL WRITE Hold Time
t_4	t_1−12 or 50[2]	t_1−22 or 50[2]	ns min	Data Valid to INTERNAL WRITE Setup Time
t_5	10	10	ns min	Data Valid to INTERNAL WRITE Hold Time
t_6	1.5 CLK IN Cycles	1.5 CLK IN Cycles	min	$\overline{LDAC}$ Pulse Width
t_7	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Setup Time
t_8	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Hold Time
t_9	60	45	ns min	$\overline{DMRD}$ Pulse Width
t_{10}[3]	57	41	ns max	Data Access Time after $\overline{DMRD}$
t_{11}[4]	5	5	ns min	Bus Relinquish Time
	45	45	ns max	

NOTES
[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]The smaller number of these two is the required data setup time, i.e., for narrower write pulses a shorter setup time is required.
[3] t_{10} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4] t_{11} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

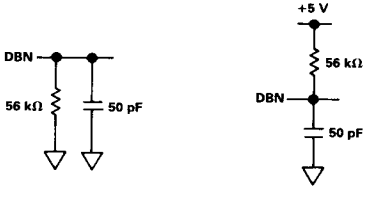
V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD}+0.3 V
V_{OUT} to AGND . . . . . V_{SS}−0.3 V to V_{DD}+0.3 V
REF IN to AGND . . . . . −0.3 V to V_{DD}+0.3 V
REF OUT to AGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

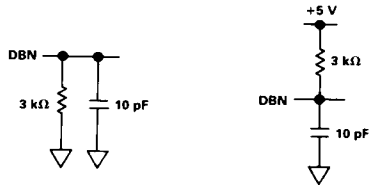
ORDERING GUIDE

Model	Temperature Range	SNR (dBs)	Package Option*
AD7848JN	0°C to +70°C	70 min	N-28
AD7848KN	0°C to +70°C	72 min	N-28
AD7848JP	0°C to +70°C	70 min	P-28A
AD7848KP	0°C to +70°C	72 min	P-28A
AD7848AQ	−25°C to +85°C	70 min	Q-28
AD7848BQ	−25°C to +85°C	72 min	Q-28

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information, see Package Information section.



a. High-Z to V_{OH} *b. V_{OL} to High-Z*
Figure 1. Load Circuits for Access Time

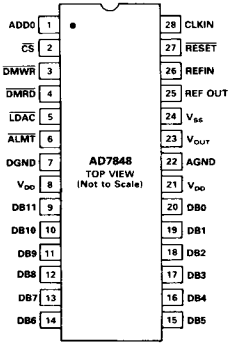


a. V_{OH} to High-Z *b. V_{OL} to High-Z*
Figure 2. Load Circuits for Output Float Delay

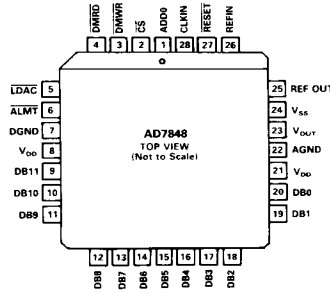
CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	ADD0	Address Input. This input determines whether the word on the data bus during a write operation is loaded to the FIFO RAM or to the status/control register. A logic low selects the FIFO memory, while a logic high selects the status/control register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ to write data to either the FIFO memory or the status/control register. Corresponds directly to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS320C25), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory Read. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to access data from the status/control register. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded to the DAC register from FIFO memory Location 0 on the falling edge of this signal. The $\overline{LDAC}$ input is asynchronous to CLK IN and is independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$. A software $\overline{LDAC}$ can be performed by writing to the control register (see STATUS/ CONTROL REGISTER section).
6	$\overline{ALMT}$	FIFO Almost Empty. A logic low indicates that the word count (i.e., number of data words in the FIFO) has reached the programmed almost empty word count in the status/control register. $\overline{ALMT}$ is updated after every $\overline{LDAC}$ operation. The $\overline{ALMT}$ output can be disabled (i.e., set to a logic high) by writing a Logic 1 to DB7 ($\overline{ENAL}$) of the status/control register. The $\overline{ALMT}$ status can also be obtained by reading the status register (see STATUS/CONTROL REGISTER section).
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{DD}	Positive Supply Voltage, +5 V±5%.
9–20	DB11–DB0	Data Bit 11 (MSB) to DB0 (LSB). Three-state TTL input/outputs. Coding for data words is 2s complement.
21	V_{DD}	Positive Supply Voltage, +5 V±5%. Same as Pin 8; both pins must be tied together at the package.
22	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
23	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3 V with REF IN = +3 V).
24	V_{SS}	Negative Supply Voltage, −5 V±5%.
25	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. To operate the AD7848 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500 μA.
26	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7848 is 3 V.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low clears the words in the FIFO memory and the contents of the DAC register to 0000 0000 0000 and resets the status/control register and control logic.
28	CLK IN	Clock Input. TTL compatible logic input. Used as the clock source for all internal dynamic logic and provides synchronization during bus transactions. The mark/space ratio of this clock can vary from 35/65 to 65/35 provided the INTERNAL WRITE timing is obeyed (see READ/WRITE Operations section).

Table I. Status/Control Bit Function Description

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{ALMT}$	AEC2	AEC1	AEC0	$\overline{ENAL}$	$\overline{FFUL}$	0	FEMP	FUND	FC2	FC1	FC0
CONTROL FUNCTION (WRITE)	X	AEC2	AEC1	AEC0	$\overline{ENAL}$	RESET	$\overline{LDAC}$	X	X	X	X	X
RESET STATUS	0	0	0	0	0	1	0	1	0	0	0	0

X = DON'T CARE

STATUS/ CONTROL REGISTER

The AD7848 contains two on-chip registers – a status register for monitoring the status of the FIFO memory and a control register to provide control for the FIFO memory functions. Because both registers reside at the same address and much of the information is common to both they are treated here as a common status/control register. Read operations from the status/control register access data from the status register, while write operations are to the control register.

The register is directly accessible through the data bus (DB11–DB0) with a read or a write operation when ADD0 is high. A write operation provides control for the $\overline{ALMT}$ output, DAC register updates and FIFO word count reset. This is normally done on power-up initialization. The FIFO memory address pointer is decremented after every DAC register update and this pointer is compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{ALMT}$ output is asserted if the $\overline{ENAL}$ control bit is set to 0. This $\overline{ALMT}$ can be used to interrupt the microprocessor after any predetermined number of DAC register updates (between 1 and 8). The status of the address pointer, along with FIFO underflow, FIFO empty and $\overline{ALMT}$ status can be accessed at any time by reading the status/control register. Note, reading from the status/control register does not cause any internal movement in the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 (ALMT)

Almost Empty Flag. Read only. This is the same as the Pin 6 ($\overline{ALMT}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed word count in bit locations DB10–DB8. $\overline{ALMT}$ is updated at the end of an $\overline{LDAC}$ operation. $\overline{ALMT}$ is active following a device reset because both the FIFO word count and the almost empty word count are 000.

DB10–DB8 (AEC2–AEC0)

Almost Empty Word Count. Read/Write. The count value determines the number of words in the FIFO memory which will cause $\overline{ALMT}$ to be set. When the FIFO word count equals the programmed count in these three bits, then both the $\overline{ALMT}$ output and DB11 of the status/control register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{ALMT}$ is set when only Location 0 through Location 3 of the FIFO memory contain valid data. AEC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{ENAL}$)

Enable Almost Empty. Read/Write. Writing a 1 to this bit disables the $\overline{ALMT}$ output and status/control register bit DB11.

DB6 (FFUL/RESET)

FIFO Full/Reset. Read/Write. Reading a 0 from this bit indicates that there are 8 words in the FIFO memory (i.e. the FIFO is full). Writing a 1 to this bit location will cause a system reset as per the $\overline{RESET}$ input (Pin 27).

DB5 ($\overline{LDAC}$)

Load DAC. Write only. Writing a 0 to this location causes the sample in Location 0 of the FIFO to be loaded into the DAC register. The function of this bit is the same as the $\overline{LDAC}$ input (Pin 5).

DB4 (FEMP)

FIFO Empty. Read only. Reading a 1 indicates that there are no words in FIFO memory. When the FIFO is empty, any further $\overline{LDAC}$ operations will continue to update the DAC register with the contents of Location 0 of the FIFO.

DB3 (FUND)

FIFO Underflow. Read only. If the FIFO memory is empty and further DAC register updates occur, then this bit is set to a 1. It will remain set until an $\overline{LDAC}$ operation occurs with valid data in FIFO Location 0.

DB2–DB0 (FC2–FC0)

FIFO Word Count. Read only. The value read from these bits indicates the number of words in FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contain valid data. Note, reading all 0s indicates that there is either one word or no word in the FIFO memory; in this case, the FIFO Empty determines if there is no word in memory. FC2 is the most significant bit.

D/A SECTION

The AD7848 contains a 12-bit voltage output D/A converter consisting of highly stable thin film resistors and high speed NMOS single pole, double throw switches. The simplified circuit diagram for the DAC section is shown in Figure 3. The three MSBs of the data word are decoded to drive the seven switches A-G. The 9 LSBs switch a 9-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

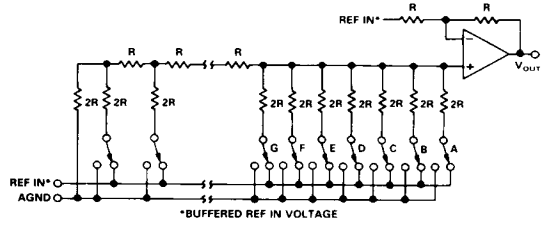


Figure 3. DAC Ladder Structure

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3 V reference and the device is tested with 3 V applied to REF IN. Operating the AD7848 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

INTERNAL REFERENCE

The AD7848 has an on-chip temperature compensated buried Zener reference (see Figure 4) which is factory trimmed to 3 V± 10 mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

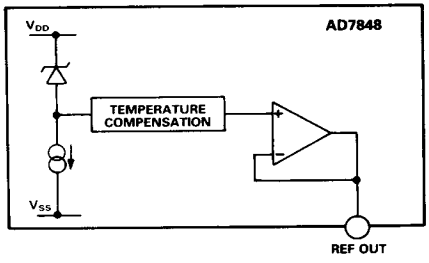


Figure 4. Internal Reference

The reference voltage can also be used as a reference for other components in the system and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

EXTERNAL REFERENCE

In some applications the user may require a system reference or some other external reference to drive the AD7848 reference input. Figure 5 shows how the AD586 5 V reference can be conditioned to provide the 3 V reference required by the AD7848 REF IN. An alternate source of reference voltage for the AD7848 in systems which use both a DAC and an ADC is to use the REF OUT voltage of an ADC such as the AD7878. A circuit showing this arrangement is outlined in Figure 16.

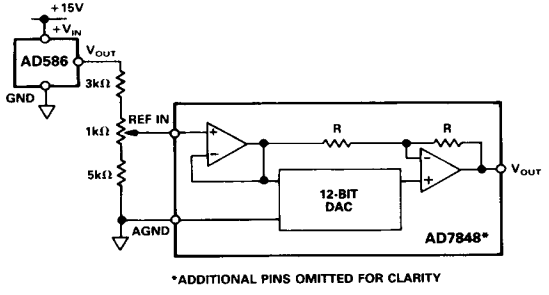


Figure 5. AD586 Driving AD7848 REF IN

OP AMP SECTION

The output from the converter is buffered by a noninverting amplifier. Internal scaling resistors on the AD7848 configure the output voltage for ±3 V from an input reference voltage of +3 V. Figure 5 shows the arrangement of these resistors around the output op amp. The buffer amplifier is capable of developing ±3 V across a 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals up to a frequency of 20 kHz.

The output is updated on the falling edge of the $\overline{LDAC}$ input. For a software DAC update, the output is updated on the next rising clock edge after receiving a software $\overline{LDAC}$. The amplifier settles to within 1/2 LSB of its final value in typically less than 2 μs for a full-scale output change.

TRANSFER FUNCTION

The basic circuit configuration for the AD7848 is shown in Figure 6. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1 LSB = FS/4096 = 6 V/4096 = 1.465 mV. The output voltage, V_{OUT}, can be expressed in terms of the input code, N, using the following relationship:

$$V_{OUT} = \frac{2 \cdot N \cdot REF\ IN}{4096} \quad -2048 \leq N \leq +2047$$

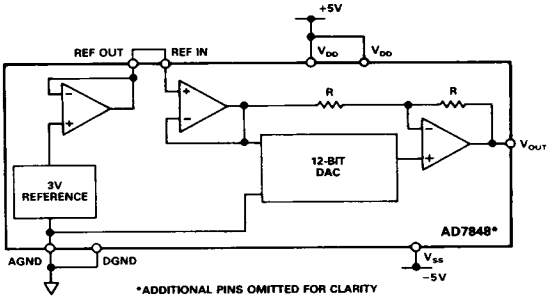


Figure 6. Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0111 1111 1111	+2.998535 V
0111 1111 1110	+2.99707 V
0000 0000 0001	+0.001465 V
0000 0000 0000	0 V
1111 1111 1111	−0.001465 V
1000 0000 0001	−2.998535 V
1000 0000 0000	−3 V

*Assuming REF IN = +3 V.

Table II. Ideal Input/Output Code Table

INTERNAL FIFO MEMORY

The internal FIFO memory of the AD7848 consists of eight memory locations, each memory location 12 bits wide. A block diagram of the AD7848 FIFO architecture is shown in Figure 7.

Data is loaded to the FIFO under control of $\overline{CS}$ and $\overline{DMWR}$. The FIFO Address Pointer always points to the top of memory i.e., the uppermost location which contains valid data. This pointer is incremented when a new word is loaded to the FIFO

from the data bus. Data is loaded from the FIFO to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. When $\overline{LDAC}$ is asserted, the data contained in the bottom location of the FIFO (Location 0) is transferred to the DAC register. On completion of this transfer operation, each word in the FIFO moves down one location and the Address Pointer is decremented by one. Therefore, each data word enters at the top of memory, propagates down with successive $\overline{LDAC}$ operations until it reaches Location 0 from where it can be transferred to the DAC register.

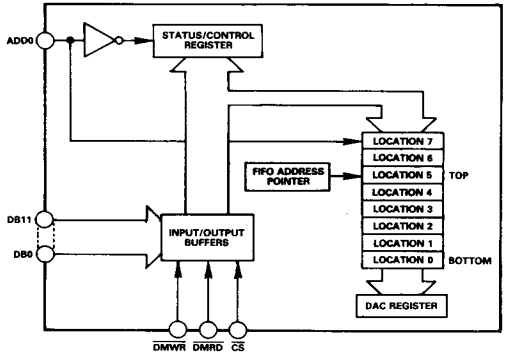


Figure 7. Internal FIFO Architecuture

The propagation of data words down the FIFO occurs in synchronization with the AD7848 input clock (CLK IN). As a result, a write operation to the FIFO memory must also be synchronous with CLK IN. If the write operation is not synchronous with a CLK IN cycle or if the $\overline{DMWR}$ line goes low within 20 ns prior to a rising edge of CLK IN, the AD7848 logic will stop operating correctly. This means that in systems where the AD7848 CLK IN is not derived from the microprocessor clock, the CLK IN and $\overline{DMWR}$ signals will have to be synchronized externally.

The updating of the status register following data movements in the FIFO also occurs in synchronization with CLK IN. The status register is updated on the next rising CLK IN edge after $\overline{DMWR}$ goes low. A setup time of 70 ns is required between the falling edge of $\overline{DMWR}$ and the rising edge of CLK IN to ensure that the status register update takes place on that rising edge; otherwise the update will slip to the next rising edge of CLK IN. If the AD7848 is operated with a $\overline{DMWR}$ to CLK IN setup time of less than 70 ns, the updating of the status register does not take place on the same clock cycle but data is written correctly to the FIFO. This means that in these situations the status register should not be read during the CLK IN cycle following the write operation. To get the correct information, the user will have to allow one clock cycle between the write and read operations.

READ/WRITE OPERATIONS

The AD7848 read/write operations consist of writing to the FIFO memory and status/control register and reading from the status/control register. These operations are controlled by the $\overline{CS}$, $\overline{DMWR}$, $\overline{DMRD}$ and ADD0 logic inputs.

Write Operation

A write operation to the AD7848 FIFO memory consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 low. Internally, these signals are gated with CLK IN to provide an INTERNAL WRITE signal (see Figure 8). The pulse width of this INTERNAL WRITE signal is effectively the overlap between the CLK IN low time and the $\overline{CS}$ and $\overline{DMWR}$ pulses. This may result in shorter write pulse widths, setup times and data hold times than those given by a microprocessor. The timing on the AD7848 timing diagram of Figure 9 is therefore given with respect to the INTERNAL WRITE signal rather than the $\overline{DMWR}$ signal. A similar situation exists for writing information to the AD7848 status/control register. A write operation to the status/control register consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 high.

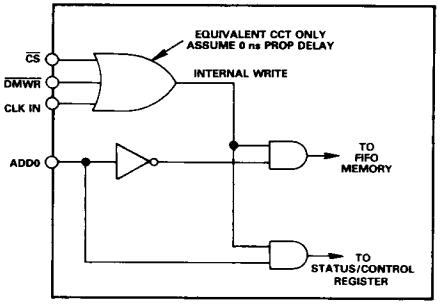


Figure 8. $\overline{DMWR}$ Internal Logic

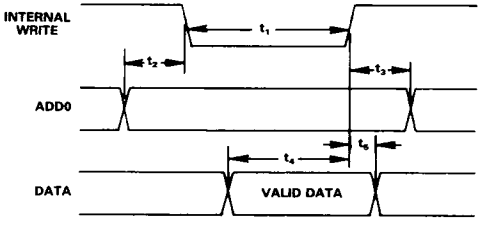


Figure 9. AD7848 Write Operation

Data is internally latched to the FIFO memory on the rising edge of CLK IN after $\overline{DMWR}$ goes low. Keeping $\overline{DMWR}$ low for numerous CLK IN cycles does not result in numerous FIFO write operations. Data is written on the first rising CLK IN edge after $\overline{DMWR}$ goes low.

Read Operation

Figure 10 shows the timing diagram for a read operation from the status/control register of the AD7848. $\overline{CS}$ and $\overline{DMRD}$ going low accesses data from the status/control register. The ADD0 line can either be high or low for a read from the status/control register.

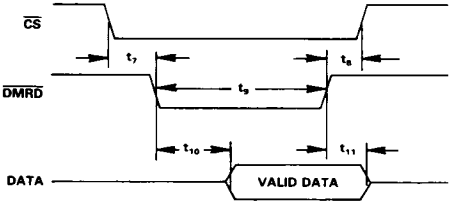


Figure 10. AD7848 Read Operation

UPDATING THE DAC OUTPUT

The DAC output on the AD7848 can be updated under software or hardware control. For hardware control, the output is updated by asserting the $\overline{LDAC}$ input; for software control, writing a 0 to DB5 of the status/control register updates the output.

The $\overline{LDAC}$ input is an asynchronous input which is independent of CLK IN. This is essential for applications where precise sampling in time is important. In these applications, the signal update must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases, the $\overline{LDAC}$ input is driven from a timer or some precise clock source.

In applications where precise sampling is not critical, the $\overline{LDAC}$ pulse can be generated from a microprocessor $\overline{WR}$ line gated with a decoded address (different to the AD7848 $\overline{CS}$ address). Note, the $\overline{LDAC}$ input must stay low for at least 1.5 CLK IN cycles.

The updating of the DAC output occurs directly after the $\overline{LDAC}$ input goes low. However, the shifting of data words down the FIFO occurs a number of CLK IN cycles later. If a write operation occurs before the shifting of words has happened then the FIFO shifting will be delayed until the write operation is completed. Care must be taken in this situation because since no FIFO shift has occurred the word is still in the FIFO. For example, if the FIFO contained eight words before the $\overline{LDAC}$ operation, it would continue to contain eight words until the FIFO shift occurred, and in this case no new words could be written to the FIFO.

The alternative method for updating the DAC output is a software update which is achieved by writing a 0 to DB5 of the status/control register. In this case, the DAC register is updated on the next rising clock edge of CLK IN. Continuous $\overline{LDAC}$ operations do not take place when there is a 0 in DB5. The update only occurs on the next CLK IN rising edge after the 0 is written to DB5. The $\overline{LDAC}$ input (Pin 5) should be tied high for software control of the DAC update.

AD7848 DYNAMIC SPECIFICATIONS

The AD7848 is specified and 100% tested for dynamic performance specifications rather than traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as Speech Synthesis, Servo Control and High Speed Modems. These applications require information on the DAC's effect on the spectral content of the signal it is creating. Hence, the parameters for which the AD7848 is specified include Signal-to-Noise Ratio, Harmonic Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave output is given by

$$SNR = (6.02\,N + 1.76)\,dB \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

Figure 11 shows a typical 2048 point Fast Fourier Transform (FFT) plot of the AD7848KN with an output frequency of 1 kHz and an update rate of 100 kHz. The SNR obtained from this graph is 73.3 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

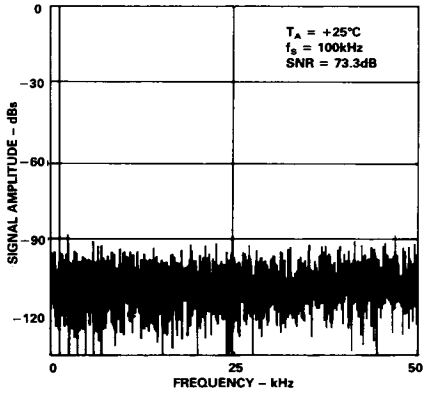


Figure 11. AD7848 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N_{EFF}).

$$N_{EFF} = \frac{SNR - 1.76}{6.02} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7848, THD is defined as

$$THD = 20\,Log\,\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the 2048-point FFT plot.

Peak Harmonic or Spurious Noise

Peak Harmonic or Spurious Noise is defined as the ratio of the rms value of the next largest component in the DAC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

Testing the AD7848

The method used to test the dynamic performance specifications is outlined in Figure 12. Data is loaded to the AD7848 under control of the microcontroller and associated logic. The output of the AD7848 is applied to a 9th order low-pass filter. The output of the filter is in turn applied to a 14-bit accurate digitizer. The digitizer samples the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7848 can be evaluated.

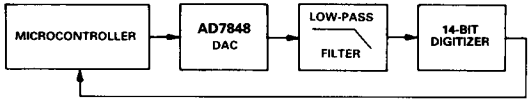


Figure 12. AD7848 Dynamic Performance Test Circuit

The digitizer's sampling is synchronized with the AD7848 update rate to ease FFT calculations. The digitizer samples the AD7848 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly; it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7848 would not be measured correctly, giving better results than the actual performance of the AD7848. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7848 is measured.

Some applications will require improved performance versus frequency from the AD7848. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 13 will extend the very good performance of the AD7848 to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7848. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance of the AD7848.

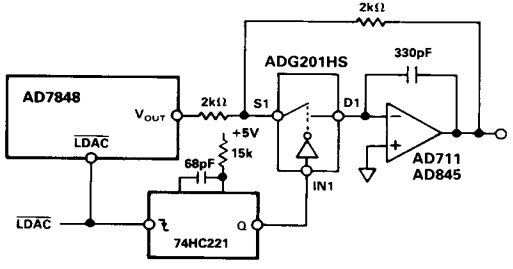


Figure 13. Sample-and-Hold Circuit

Performance versus Frequency

The typical performance plots of Figures 14 and 15 show the performance of the AD7848 over a wide range of input frequencies. The plot of Figure 14 is without a sample-and-hold on the output while the plot of Figure 15 is generated with the sample-and-hold circuit of Figure 13 on the output.

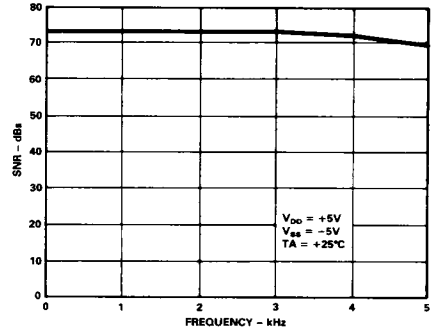


Figure 14. Performance vs. Frequency (No Sample-and-Hold)

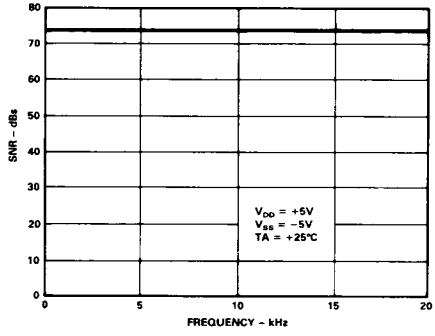


Figure 15. Performance vs. Frequency (with Sample-and-Hold)

MICROPROCESSOR INTERFACING

The AD7848 high speed bus timing allows direct interfacing to DSP processors. Due to the complexity of the AD7848 internal logic, only synchronous interfacing is allowed. This means that the AD7848 CLK IN must be the same as or a derivative of the processor clock. In applications where this is not possible, the CLK IN and $\overline{DMWR}$ signals must be externally gated. Suitable processor interfaces are shown in Figures 16 to 19.

AD7848 – ADSP-2100 Interface

Figure 16 shows an interface between the AD7848 and the ADSP-2100 DSP processor. Also included in the interface is the AD7878, a 12-bit A/D converter which also contains an on-chip FIFO and has dynamic performance specifications. An interface like this is suitable for applications such as modems and servo control.

Conversion is initiated on the ADC using an external timer. This timer is also used to control the updating of the AD7848 output. The $\overline{ALFL}$ output interrupts the microprocessor when the FIFO word count of the AD7878 has reached its preprogrammed value. The processor then reads the conversion results from the AD7878's internal FIFO memory. Similarly, the $\overline{ALMT}$ output interrupts the microprocessor when the AD7848's preprogrammed word count is reached. The processor then loads another batch of samples to the AD7848's internal FIFO memory.

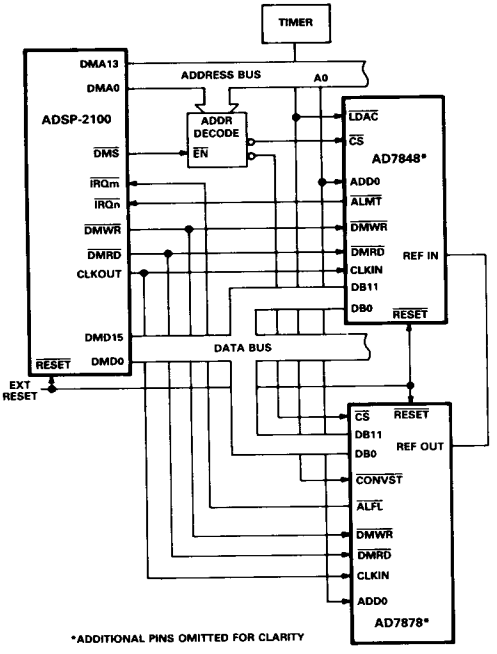


Figure 16. AD7848/AD7878 – ADSP-2100 Interface

AD7848 – TMS320C25 Interface

An interface between the AD7848 and the TMS320C25 DSP processor is shown in Figure 17. As in the previous interface, the updating of the AD7848 output is controlled by an external timer. The $\overline{ALMT}$ output of the AD7848 provides an interrupt signal to the TMS320C25. The TMS320C25 CLKOUT2 signal must be inverted before being applied to the AD7848 CLK IN pin. A single WAIT state is inserted in a read cycle to the AD7848 status/control register via the TMS320C25 READY input.

The TMS320C25 does not have separate $\overline{RD}$ and $\overline{WR}$ outputs to drive the AD7848 $\overline{DMWR}$ and $\overline{DMRD}$ inputs. These are generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

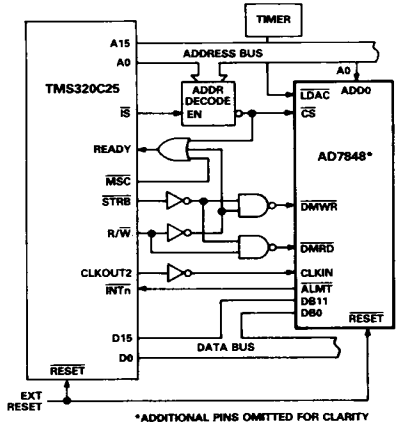


Figure 17. AD7848 – TMS320C25 Interface

AD7848 – TMS32010 Interface

Figure 18 shows an interface between the AD7848 and the TMS32010 DSP processor. Once again, an external timer is used to update the DAC output. The TMS32010 CLKOUT signal must be inverted before being applied to the AD7848 CLK IN pin.

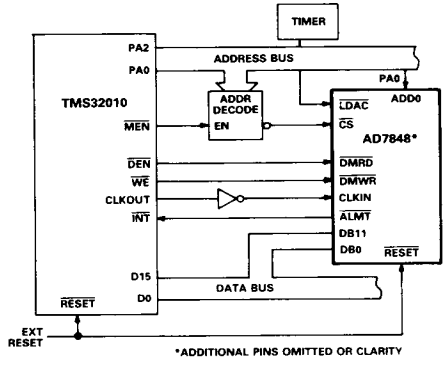


Figure 18. AD7848 – TMS32010 Interface

AD7848 – MC68000 Interface

This interface also uses an external timer for updating the analog output as described in the previous three interfaces. It differs from the other interfaces because it needs extra logic due to the nature of its interrupts. The MC 68000 has eight levels of external interrupt. When interrupting this processor one of these levels (0 to 7) has to be encoded onto the IPL2–IPL0 inputs. This is achieved with a 74148 encoder in Figure 19, (interrupt level 1 is taken for example purposes only). The $\overline{ALMT}$ output drives the appropriate input of the 74148 for the required interrupt level. The MC68000 places this interrupt level on address bits A3 to A1 at the start of the interrupt service routine. Additional logic is used to decode this interrupt level on the address bus and the FC2–FC0 outputs to generate a VPA signal for the MC68000. This results in an autovectored interrupt; the start address for the service routine must be loaded into the appropriate auto vector location during initialization. For further information on the 68000 interrupts consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate separate $\overline{DMWR}$ and $\overline{DMRD}$ inputs for the the AD7848. Since the $\overline{UDS}$ line is used to decode the $\overline{DMWR}$ and $\overline{DMRD}$ signals, the AD7848 is memory-mapped at an even address.

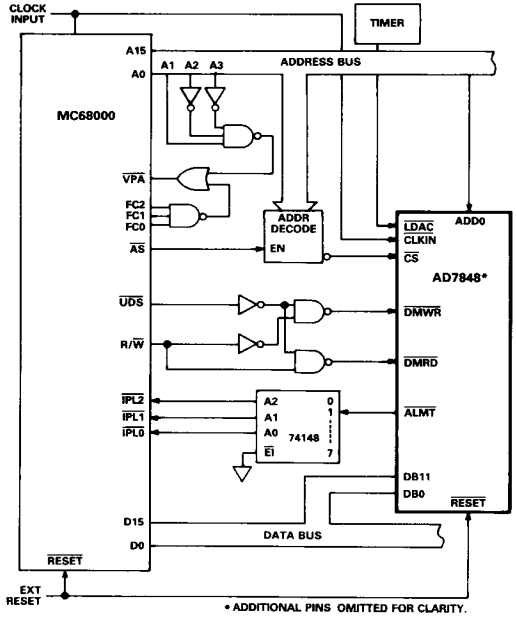


Figure 19. AD7848 – MC68000 Interface

APPLYING THE AD7848

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7848 works on an LSB size of 1.465 mV. Therefore, the designer has to be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feedthrough to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7848 as shown in Figure 20. Connect all analog grounds to this star ground and also connect the AD7848 DGND pin to this ground. Do not connect any other digital grounds to this analog ground point.

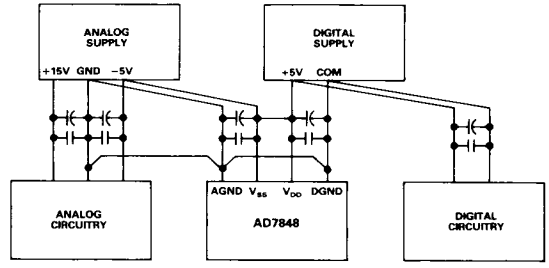


Figure 20. Power Supply Grounding Practice

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the signal leads on the V_{OUT} signal and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC output and its destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

FEEDTHROUGH

The CLK IN feedthrough to the analog output is 2 mV typical. This occurs at 10 MHz and since almost all applications will have a low pass filter on the output to remove the update frequency, the CLK IN feedthrough should not be a problem.