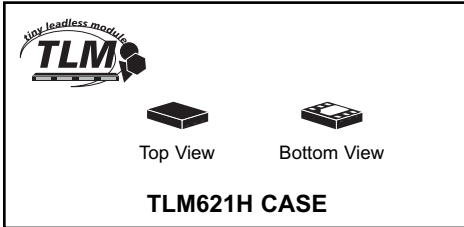




CTLDM8002A-M621H
SURFACE MOUNT TLM™
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET



MARKING CODE: CMA

Central™

Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8002A-M621H is a very low profile (0.4mm) P-Channel enhancement-mode MOSFET in a small, thermal efficient, 1.5mm x 2mm TLM™ package.

FEATURES:

- Low $R_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small, Very Low Profile, TLM™

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS ($T_A=25^\circ\text{C}$)

Drain-Source Voltage
Drain-Gate Voltage
Gate-Source Voltage
Continuous Drain Current
Continuous Source Current (Body Diode)
Maximum Pulsed Drain Current
Maximum Pulsed Source Current
Power Dissipation (Note 1)
Operating and Storage
Junction Temperature
Thermal Resistance (Note 1)

SYMBOL		UNITS
V_{DS}	50	V
V_{DG}	50	V
V_{GS}	20	V
I_D	280	mA
I_S	280	mA
I_{DM}	1.5	A
I_{SM}	1.5	A
P_D	1.6	W
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
θ_{JA}	75	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0\text{V}$		1.0	μA
I_{DSS}	$V_{DS}=50\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$		500	μA
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=10\text{V}$	500		mA
BV_{DSS}	$V_{GS}=0\text{V}, I_D=10\mu\text{A}$	50		V

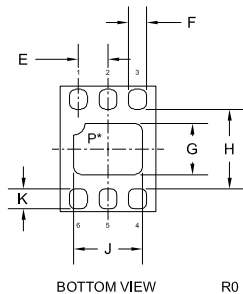
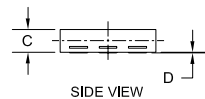
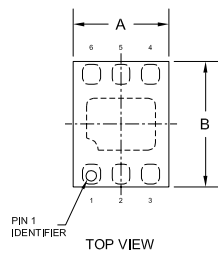
Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

R0 (15-June 2006)

ELECTRICAL CHARACTERISTICS - Continued ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$		1.5	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$		0.15	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$		2.5	Ω
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$, $T_J=125^\circ\text{C}$		4.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$		3.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$, $T_J=125^\circ\text{C}$		5.0	Ω
τ_{fs}	$V_{DS}=10\text{V}$, $I_D=200\text{mA}$	200		msec
C_{rss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		7.0	pF
C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		70	pF
C_{oss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		15	pF
t_{on}	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=200\text{mA}$		20	ns
t_{off}	$R_G=25\Omega$, $R_L=150\Omega$		20	ns
V_{SD}	$V_{GS}=0\text{V}$, $I_S=115\text{mA}$		1.3	V

TLM621H CASE - MECHANICAL OUTLINE



* Exposed pad P Internally connected to pins 3 and 4

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

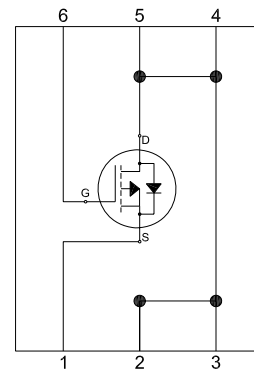
TLM621H (REV:R0)

LEAD CODE:

- 1) SOURCE
- 2) DRAIN
- 3) DRAIN
- 4) DRAIN
- 5) DRAIN
- 6) GATE

MARKING CODE: CMA

PIN CONFIGURATION:



R0 (15-June 2006)