

## SN74LVC10A Triple 3-Input Positive-NAND Gate

### 1 Features

- Operates from 1.65V to 3.6V
- Specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs accept voltages to 5.5V
- Max  $t_{pd}$  of 4.9ns at 3.3V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114-A)

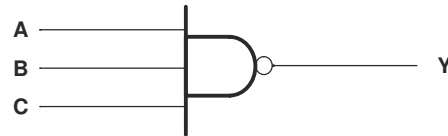
### 2 Description

This triple 3-input positive-NAND gate is designed for 1.65V to 3.6V  $V_{CC}$  operation.

#### Package Information

PART NUMBER	PACKAGE SIZE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN74LVC10A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.5mm × 3.5mm

- For more information, see [Section 10](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



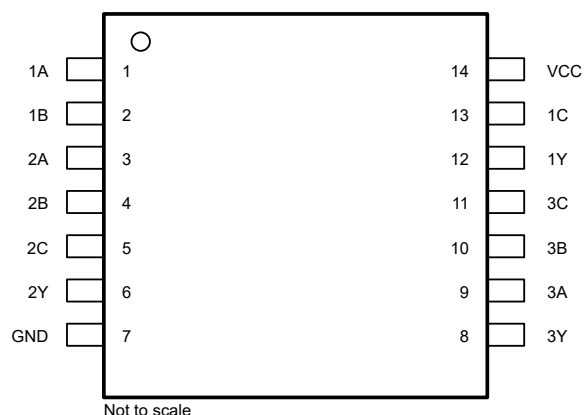
Logic Diagram, Each Gate (Positive Logic)



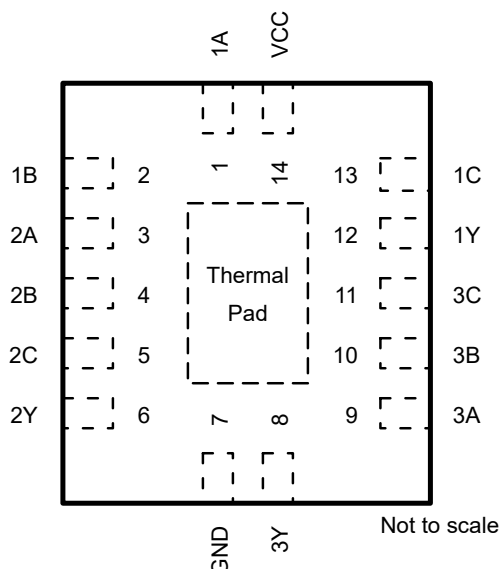
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## 3 Pin Configuration and Functions



**Figure 3-1. SN74LVC10A D, DB, NS, or PW Packages; 14-Pin SOIC, SSOP, SOP, or TSSOP (Top View)**



**Figure 3-2. SN74LVC10A BQA Package, 14-Pin WQFN (Top View)**

**Table 3-1. Pin Functions**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3C	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V <sub>CC</sub>	14	—	Positive Supply
Thermal pad		—	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(1)</sup>	-0.5	6.5	V
$V_O$	Output voltage range <sup>(1) (2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature range	-65	150	°C
$P_{tot}$	Power dissipation	$T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ <sup>(3) (4)</sup>		500 mW

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of  $V_{CC}$  is provided in the recommended operating conditions table.

(3) For the D package: above  $70^{\circ}\text{C}$ , the value of  $P_{tot}$  derates linearly with 8 mW/K.

(4) For the DB, NS, and PW packages: above  $60^{\circ}\text{C}$ , the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

### 4.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

			T <sub>A</sub> = 25°C		−40 TO 85°C		−40 TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V	0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V	1.7		1.7		1.7		
		V <sub>CC</sub> = 2.7V to 3.6V	2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V	0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V	0.7		0.7		0.7		
		V <sub>CC</sub> = 2.7V to 3.6V	0.8		0.8		0.8		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65V	−4		−4		−4		mA
		V <sub>CC</sub> = 2.3V	−8		−8		−8		
		V <sub>CC</sub> = 2.7V	−12		−12		−12		
		V <sub>CC</sub> = 3V	−24		−24		−24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65V	4		4		4		mA
		V <sub>CC</sub> = 2.3V	8		8		8		
		V <sub>CC</sub> = 2.7V	12		12		12		
		V <sub>CC</sub> = 3V	24		24		24		

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC10A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.3	127.8	96	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Not recommended for air temperature range (unless otherwise noted)										
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100μA	1.65V to 3.6V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.3		V
	I <sub>OH</sub> = –4mA	1.65V	1.29			1.2		1.05		
	I <sub>OH</sub> = –8mA	2.3 V	1.9			1.7		1.55		
	I <sub>OH</sub> = –12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
	I <sub>OH</sub> = –24mA	3V	2.3			2.2		2		
V <sub>OL</sub>	I <sub>OL</sub> = 100μA	1.65V to 3.6V	0.1			0.2		0.3		V
	I <sub>OL</sub> = 4mA	1.65V	0.24			0.45		0.6		
	I <sub>OL</sub> = 8mA	2.3V	0.3			0.7		0.75		
	I <sub>OL</sub> = 12mA	2.7V	0.4			0.4		0.6		
	I <sub>OL</sub> = 24mA	3V	0.55			0.55		0.8		
I <sub>I</sub>	V <sub>I</sub> = 5.5V or GND	3.6V	±1			±5		±20		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6V	1			10		40		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V <sub>I</sub> , Other inputs at V <sub>CC</sub> or GND	2.7V to 3.6V	500			500		5000		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V	5							pF

## 4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	1.8V ± 0.15V	1	4.2	10.1	1	10.6	1	12.1	ns
			2.5V ± 0.2V	1	2.9	7.3	1	7.8	1	9.9	
			2.7V	1	3.1	5.6	1	5.8	1	7.4	
			3.3V ± 0.3V	1	2.7	4.7	1	4.9	1	6	
t <sub>sk(o)</sub>			3.3V ± 0.3V				1		1.5		ns

## 4.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

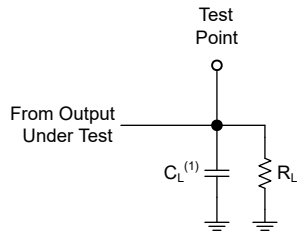
PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per gate	$f = 10\text{ MHz}$	1.8V	9	pF
			2.5V	10	
			3.3V	11	

## 5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f \leq 2.5\text{ns}$ .

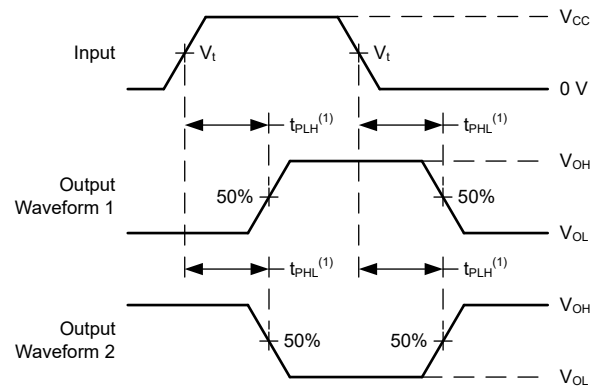
The outputs are measured individually with one input transition per measurement.

$V_{CC}$	$V_t$	$R_L$	$C_L$	$\Delta V$
$1.8\text{V} \pm 0.15\text{V}$	$V_{CC}/2$	$1\text{k}\Omega$	$30\text{pF}$	$0.15\text{V}$
$2.5\text{V} \pm 0.2\text{V}$	$V_{CC}/2$	$500\Omega$	$30\text{pF}$	$0.15\text{V}$
$2.7\text{V}$	$1.5\text{V}$	$500\Omega$	$50\text{pF}$	$0.3\text{V}$
$3.3\text{V} \pm 0.3\text{V}$	$1.5\text{V}$	$500\Omega$	$50\text{pF}$	$0.3\text{V}$



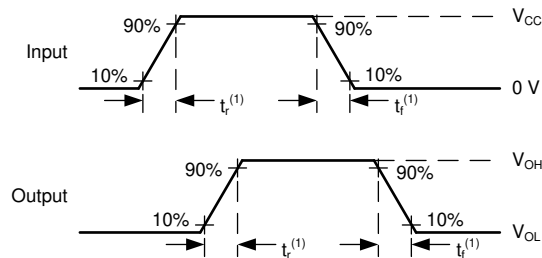
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 5-1. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 5-2. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 5-3. Voltage Waveforms, Input and Output Transition Times**

## 6 Detailed Description

### 6.1 Overview

The SN74LVC10A performs the Boolean function  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

### 6.2 Functional Block Diagram

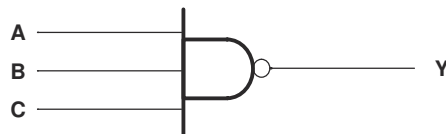


Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

### 6.3 Device Functional Modes

Table 6-1. Function Table  
(Each Gate)

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H



## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating in the [Recommended Operating Conditions](#).

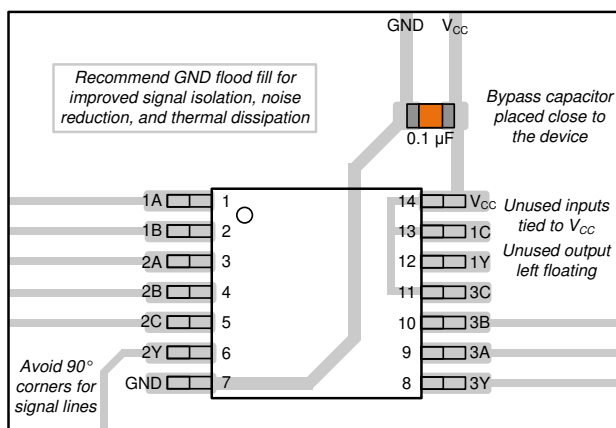
Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

#### 7.2.2 Layout Example



**Figure 7-1. Example layout for the SN74LVC10A**

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 8-1. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LVC10A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

#### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision P (May 2024) to Revision Q (August 2024) Page

- Updated RθJA values: D = 86 to 127.8, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1, all values in °C/W..... [5](#)

### Changes from Revision O (July 2005) to Revision P (May 2024) Page

- Added BQA package to *Package Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table..... [1](#)
- Added *Applications* section, *Package Information* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... [1](#)

- 
- Deleted machine model from *Features* section..... [1](#)
- 

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVC10ABQAR</a>	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ABQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10AD</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10AD.B	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10ADBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADBR.B	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10ADG4	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10ADR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADR.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10ADT</a>	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ADT.B	Active	Production	SOIC (D)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10ANSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
SN74LVC10ANSR.B	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC10A
<a href="#">SN74LVC10APW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APW.B	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
<a href="#">SN74LVC10APWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWR.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWRG4.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
<a href="#">SN74LVC10APWT</a>	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
SN74LVC10APWT.B	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC10A
<a href="#">SN74LVC10ARGYR</a>	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A
SN74LVC10ARGYR.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A
SN74LVC10ARGYR.B	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC10A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC10ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC10ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC10ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC10ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC10ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC10APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC10ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC10ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC10ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC10ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC10ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC10ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC10APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC10APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC10APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC10ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVC10AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC10APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC10APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5



## GENERIC PACKAGE VIEW

**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

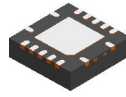
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

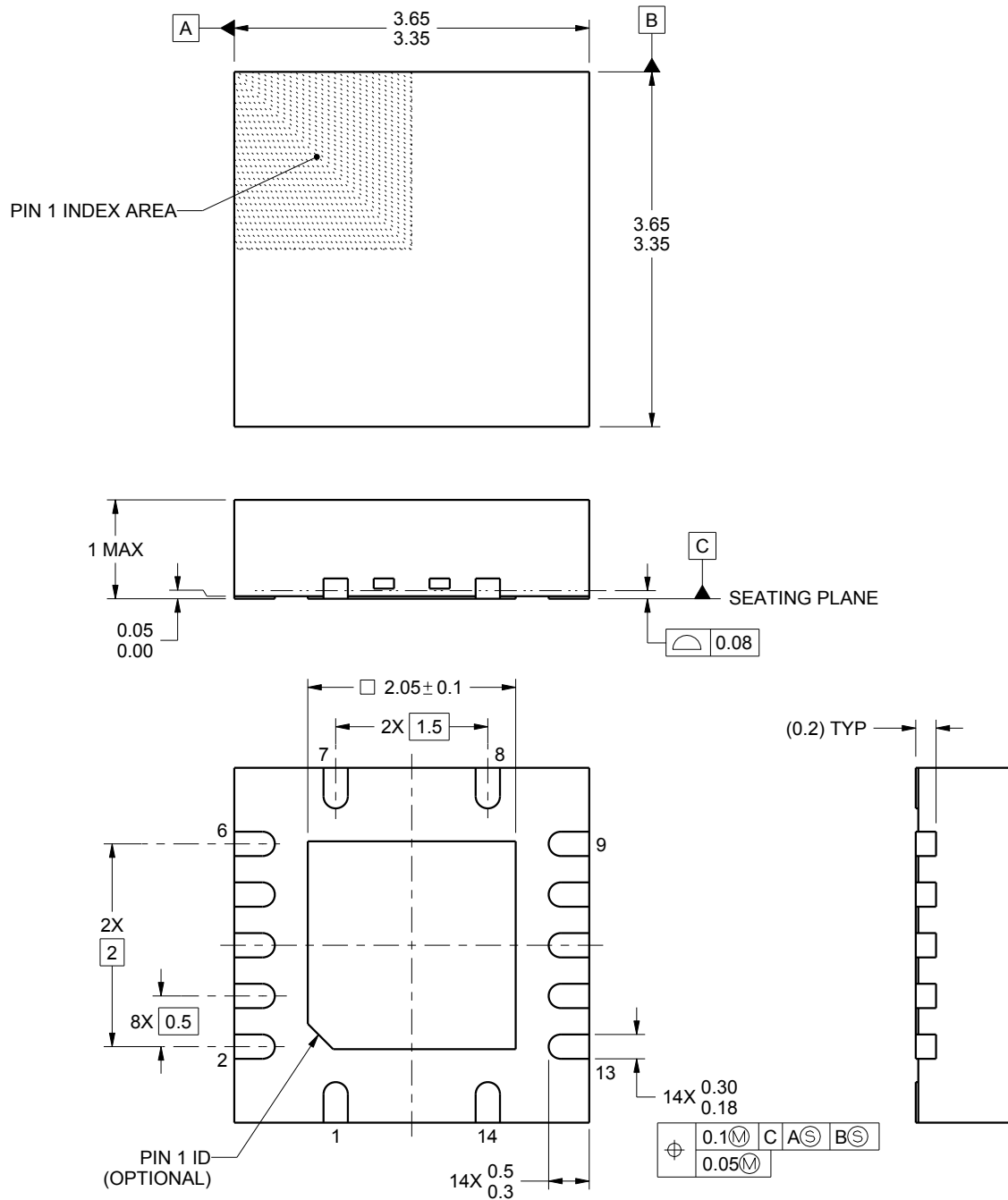
RGY0014A



## PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

### NOTES:

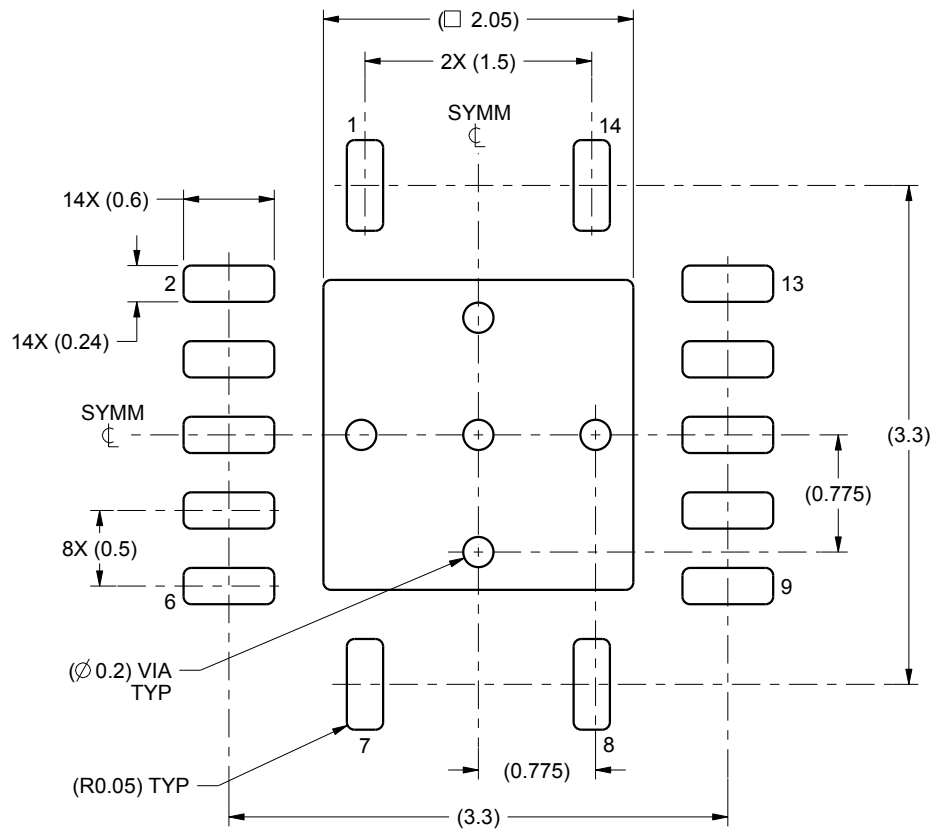
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

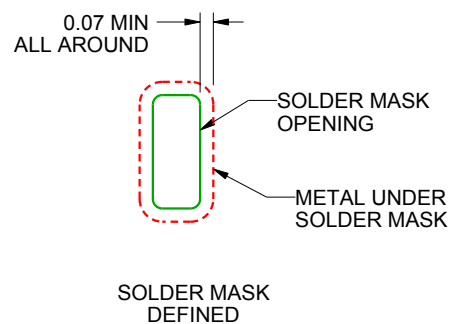
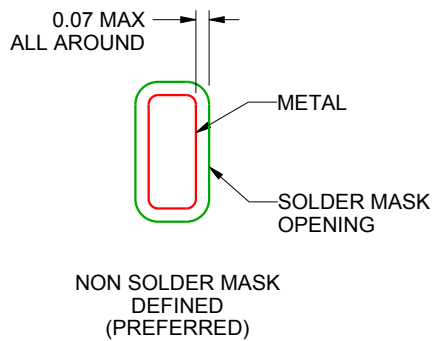
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

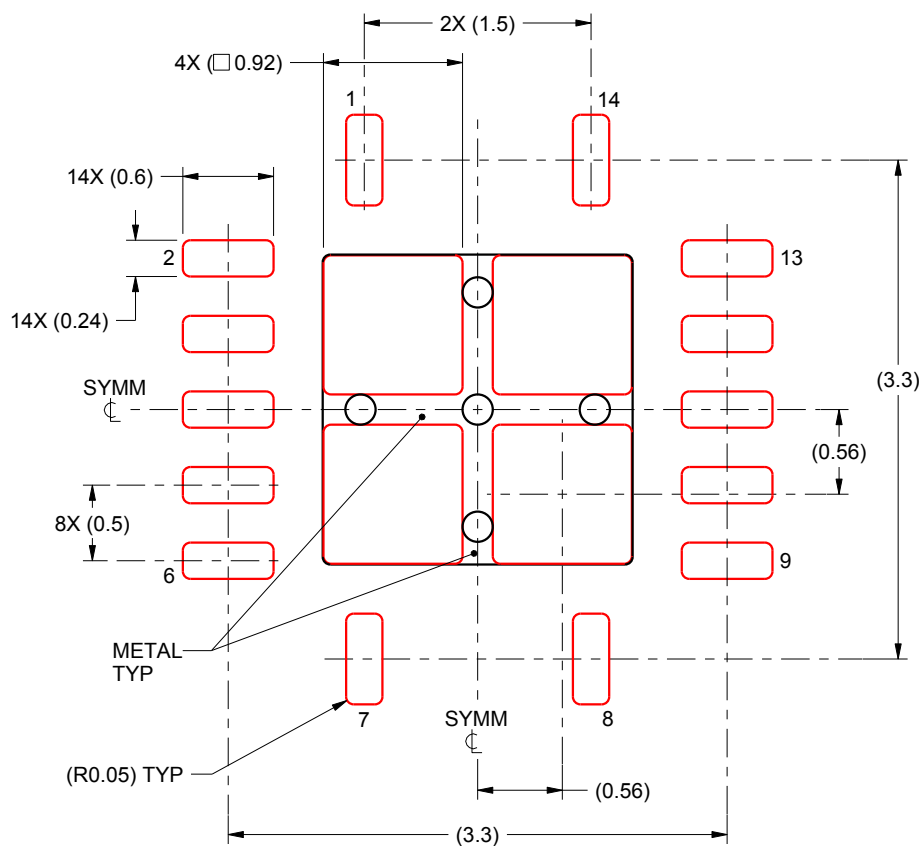
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 EXPOSED PAD  
 80% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:20X

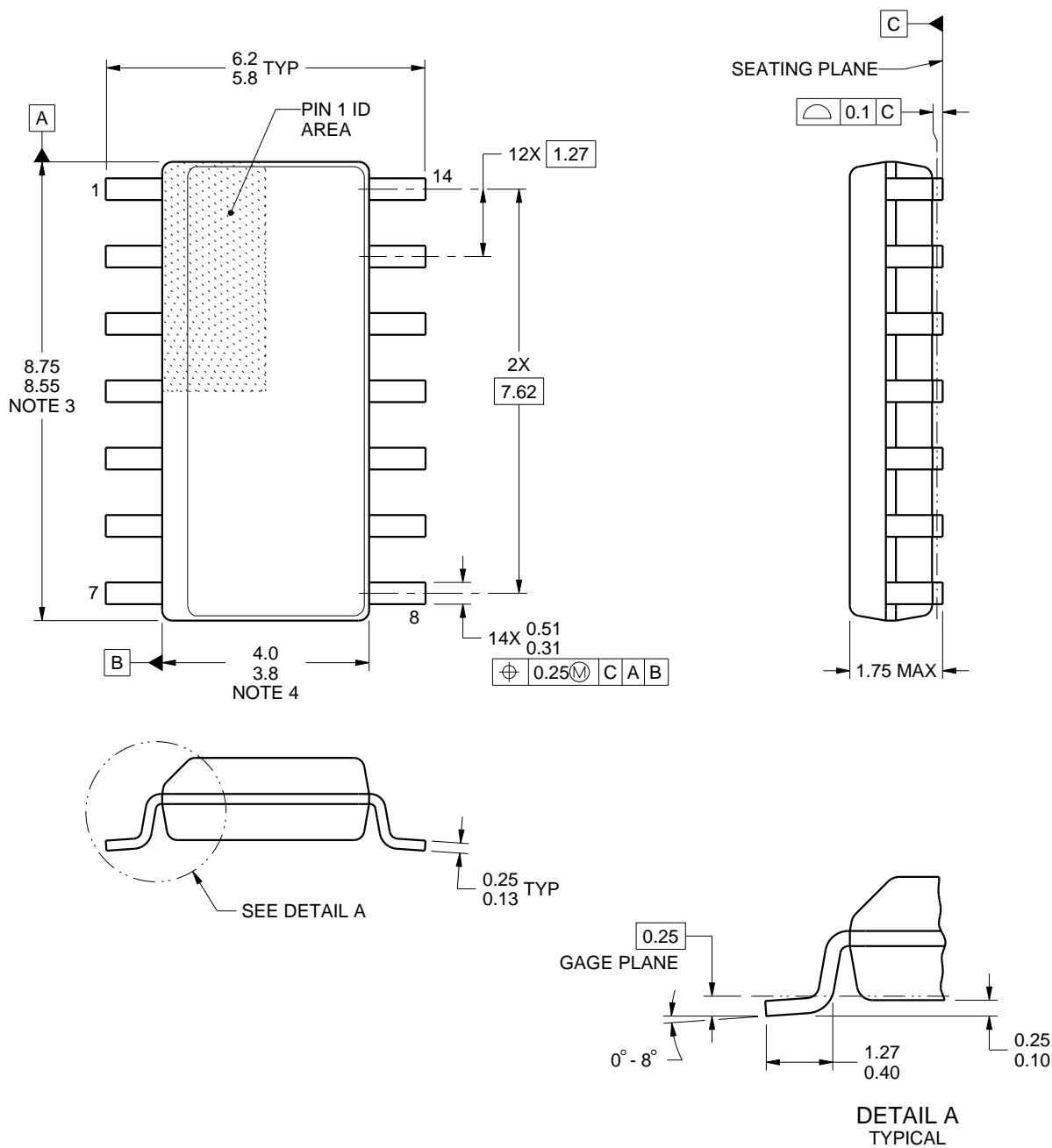
4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

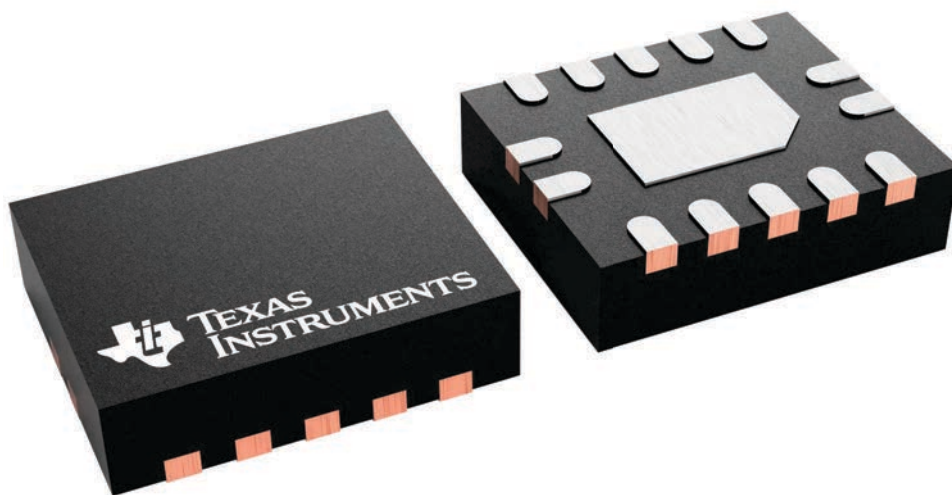
**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

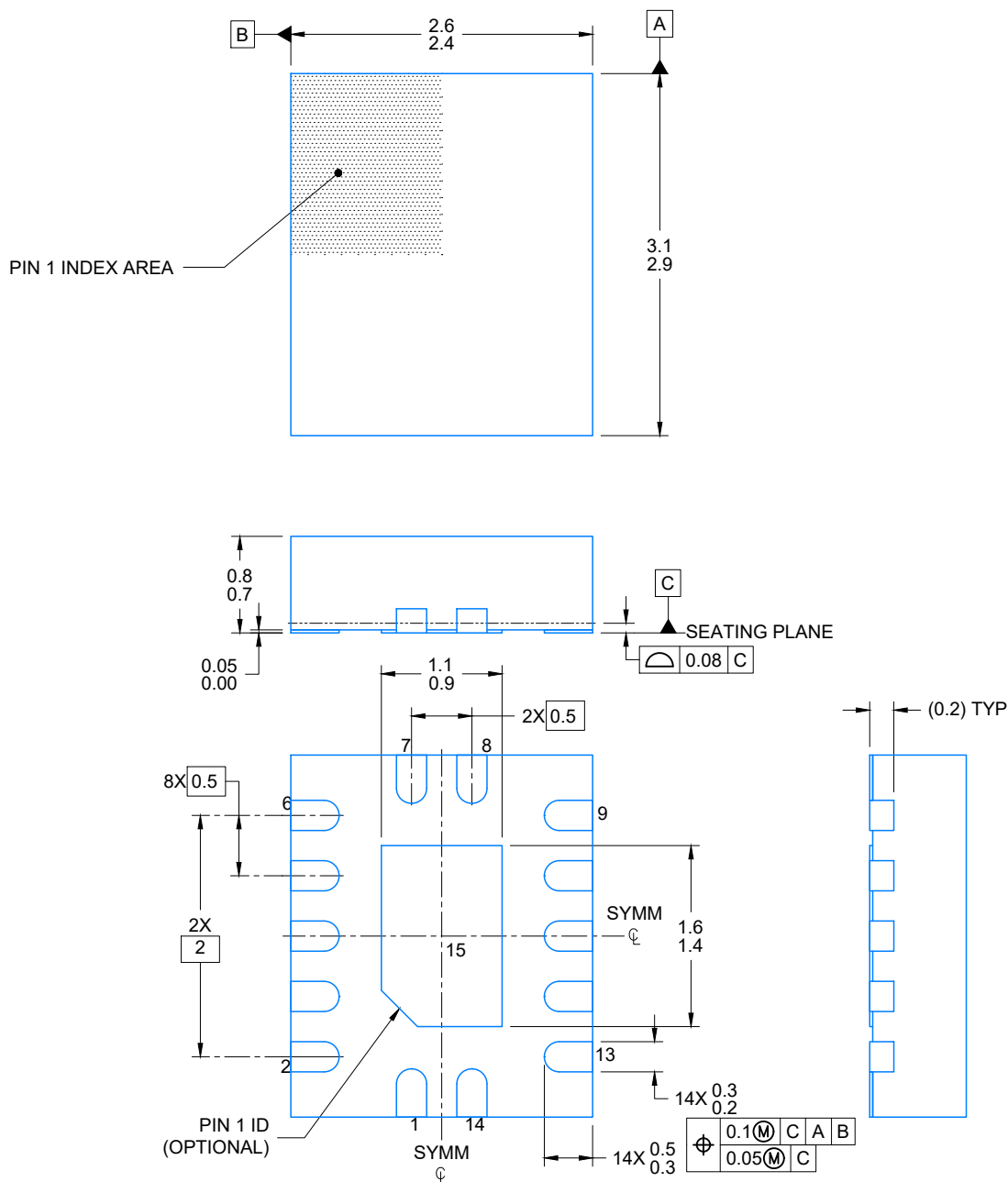


4227145/A



**WQFN - 0.8 mm max height**

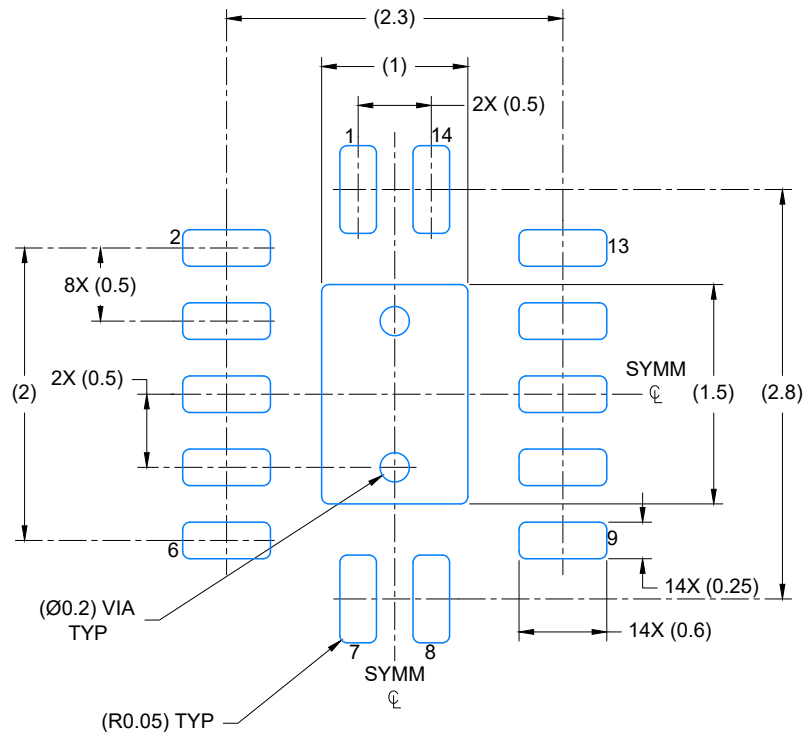
PLASTIC QUAD FLAT PACK-NO LEAD



4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220762/A 05/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

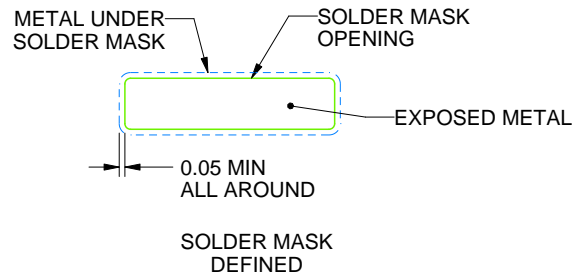
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## TSSOP - 1.2 mm max height



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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