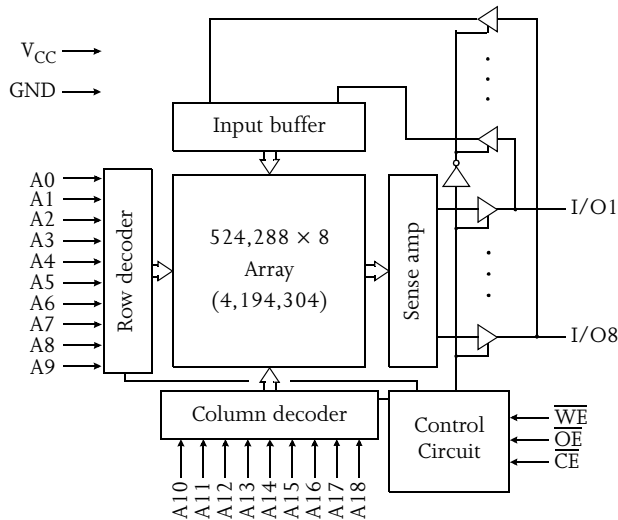
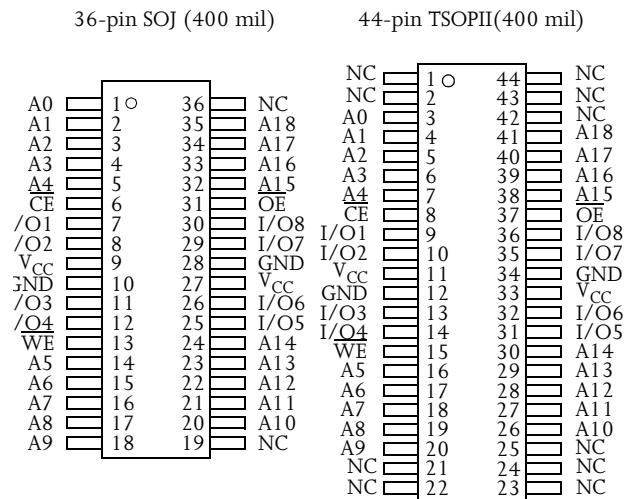



5V/3.3V 512K × 8 CMOS SRAM
Features

- AS7C4096 (5V version)
- AS7C34096 (3.3V version)
- Industrial and commercial temperature
- Organization: 524,288 words × 8 bits
- Center power and ground pins
- High speed
 - 10/12/15/20 ns address access time
 - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
 - 1375 mW (AS7C4096) / max @ 12 ns
 - 468 mW (AS7C34096) / max @ 12 ns
- Low power consumption: STANDBY
 - 110 mW (AS7C4096) / max CMOS
 - 72 mW (AS7C34096) / max CMOS
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
 - 400 mil 36-pin SOJ
 - 400 mil 44-pin TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram

Pin arrangement

Selection guide

		AS7C4096 AS7C34096 -10	AS7C4096 AS7C34096 -12	AS7C4096 AS7C34096 -15	AS7C4096 AS7C34096 -20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		5	6	7	9	ns
Maximum operating current	AS7C4096	—	250	220	180	mA
	AS7C34096	160	130	110	100	mA
Maximum CMOS standby current	AS7C4096	—	20	20	20	mA
	AS7C34096	20	20	20	20	mA



Functional description

The AS7C4096 and AS7C34096 are high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) devices organized as 524,288 words $\times$ 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The AS7C4096 is guaranteed not to exceed 110 mW power consumption in CMOS standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O8 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single supply voltage. Both devices are available in the industry standard 400-mil 36-pin SOJ and 44-pin TSOP II packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	AS7C4096	V_{t1}	–1	+7.0	V
	AS7C34096	V_{t1}	–0.5	+5.0	V
Voltage on any pin relative to GND		V_{t2}	–0.5	$V_{CC} + 0.5$	V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	–65	+150	°C
Temperature with V_{CC} applied		T_{bias}	–55	+125	°C
DC current unto output (low)		I_{OUT}	–	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = Don't care, L = Low, H = High



Recommended operating condition

Parameter	Device	Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C4096	$V_{CC}(12/15/20)$	4.5	5.0	5.5	V
	AS7C34096	$V_{CC}(-10)$	3.15	3.30	3.6	V
	AS7C34096	$V_{CC}(12/15/20)$	3.0	3.3	3.6	V
Input voltage	AS7C4096	V_{IH}	2.2	—	$V_{CC} + 0.5$	V
	AS7C34096	V_{IH}	2.0	—	$V_{CC} + 0.5$	V
		V_{IL}	$-0.5^{\dagger}$	—	0.8	V
Ambient operating temperature	commercial	T_A	0	—	70	°C
	industrial	T_A	-40	—	85	°C

$^{\dagger} V_{IL} \text{ min} = -3.0V$ for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)¹

Parameter	Symbol	Test conditions	Device	-10		-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$		—	1	—	1	—	1	—	1	μA
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}$ $V_{OUT} = \text{GND to } V_{CC}$		—	1	—	1	—	1	—	1	μA
Operating power supply current	I_{CC}	$V_{CC} = \text{Max}, \overline{CE} < V_{IL}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	AS7C4096	—	—	—	250	—	220	—	180	mA
			AS7C34096	—	160	—	130	—	110	—	100	
Standby power supply current	I_{SB}	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	AS7C4096	—	—	—	60	—	60	—	60	mA
			AS7C34096	—	60	—	60	—	60	—	60	
	I_{SB1}	$V_{CC} = \text{Max},$ $\overline{CE} \geq V_{CC} - 0.2V, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V, f = 0$	AS7C4096	—	—	—	20	—	20	—	20	mA
			AS7C34096	—	20	—	20	—	20	—	20	
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$		—	0.4	—	0.4	—	0.4	—	0.4	V
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$		2.4	—	2.4	—	2.4	—	2.4	—	V

Capacitance ($f = 1\text{MHz}, T_a = 25^{\circ}\text{C}, V_{CC} = \text{NOMINAL}$)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	$V_{IN} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF

Parameter	Symbol	−10		−12		−15		−20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	10	—	12	—	15	—	20	—	ns	
Address access time	t _{AA}	—	10	—	12	—	15	—	20	ns	3
Chip enable ($\overline{\text{CE}}$) access time	t _{ACE}	—	10	—	12	—	15	—	20	ns	3
Output enable ($\overline{\text{OE}}$) access time	t _{OE}	—	5	—	6	—	7	—	8	ns	
Output hold from address change	t _{OH}	3	—	3	—	3	—	3	—	ns	5
$\overline{\text{CE}}$ Low to output in low Z	t _{CLZ}	3	—	3	—	0	—	0	—	ns	4, 5
$\overline{\text{CE}}$ High to output in high Z	t _{CHZ}	—	5	—	6	—	7	—	9	ns	4, 5
$\overline{\text{OE}}$ Low to output in low Z	t _{OLZ}	0	—	0	—	0	—	0	—	ns	4, 5
$\overline{\text{OE}}$ High to output in high Z	t _{OHZ}	—	5	—	6	—	7	—	9	ns	4, 5
Power up time	t _{PU}	0	—	0	—	0	—	0	—	ns	4, 5
Power down time	t _{PD}	—	10	—	12	—	15	—	20	ns	4, 5

 Rising input
 Falling input
 Undefined/don't care

The timing diagram illustrates the relationship between the $\overline{\text{CE}}$, $\overline{\text{OE}}$, D_{OUT} , and Supply current signals. Key timing parameters are defined as follows:

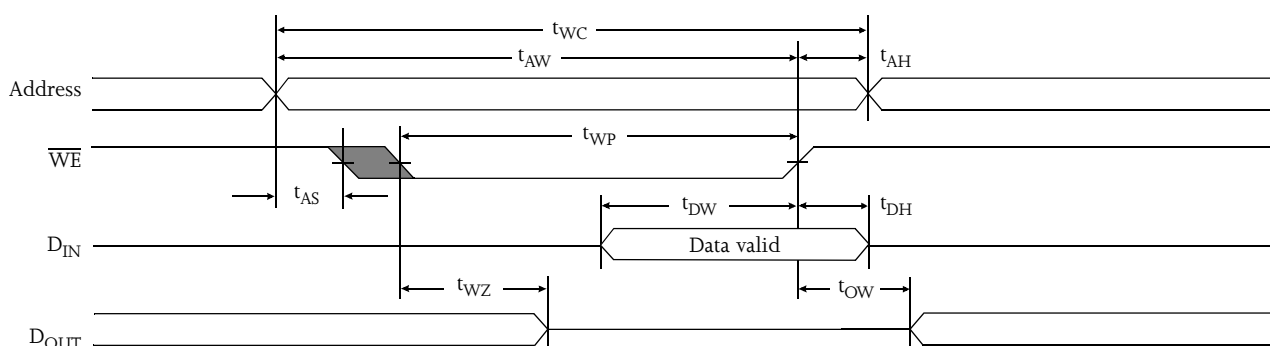
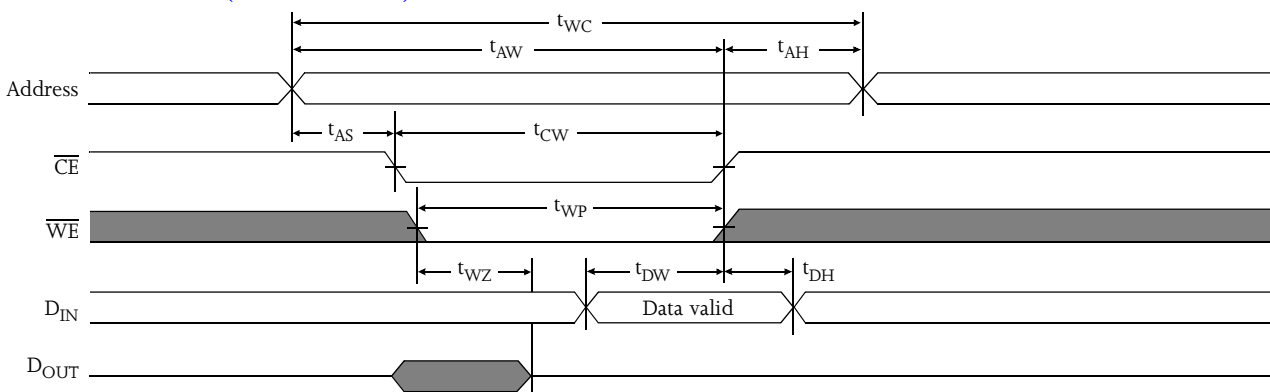
- t_{RC1} : Delay from $\overline{\text{CE}}$ falling edge to D_{OUT} becoming valid.
- t_{OE} : Delay from $\overline{\text{OE}}$ falling edge to D_{OUT} becoming valid.
- t_{OLZ} : Delay from $\overline{\text{OE}}$ falling edge to D_{OUT} entering high-impedance state.
- t_{ACE} : Delay from $\overline{\text{CE}}$ rising edge to D_{OUT} entering high-impedance state.
- t_{OHZ} : Delay from $\overline{\text{OE}}$ rising edge to D_{OUT} entering high-impedance state.
- t_{CHZ} : Delay from $\overline{\text{OE}}$ rising edge to D_{OUT} becoming valid.
- t_{CLZ} : Delay from $\overline{\text{CE}}$ falling edge to D_{OUT} entering high-impedance state.
- t_{PU} : Delay from $\overline{\text{CE}}$ falling edge to D_{OUT} becoming valid.
- t_{PD} : Delay from D_{OUT} becoming valid to D_{OUT} entering high-impedance state.

The Supply current signal shows a transition from I_{CC} to I_{SB} at 50% of the t_{PD} delay.

Parameter	Symbol	−10		−12		−15		−20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t _{WC}	10	—	12	—	15	—	20	—	ns	
Chip enable ($\overline{\text{CE}}$) to write end	t _{rw}	7	—	8	—	10	—	12	—	ns	



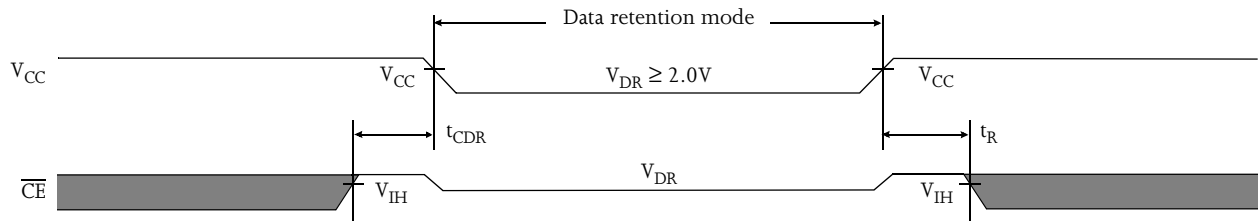
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Address setup to write end	t_{AW}	7	—	8	—	10	—	12	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Write pulse width ($\overline{OE} = \text{high}$)	t_{WP1}	7	—	8	—	10	—	12	—	ns	
Write pulse width ($\overline{OE} = \text{low}$)	t_{WP2}	10	—	12	—	15	—	20	—	ns	
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	ns	
Data valid to write end	t_{DW}	5	—	6	—	7	—	9	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	ns	4, 5
Write enable to output in high Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	—	3	—	3	—	3	—	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)^{10,11}

Write waveform 2 ($\overline{CE}$ controlled)^{10,11}

Data retention characteristics (over the operating range)¹³

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0V$ $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	V
Data retention current	I_{CCDR}		—	500	μA
Chip deselect to data retention time	t_{CDR}		0	—	ns
Operation recovery time	t_R		t_{RC}	—	ns
Input leakage current	$ I_{LI} $		—	1	μA



Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figures A, B, and C.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

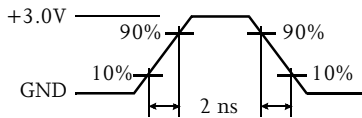


Figure A: Input pulse

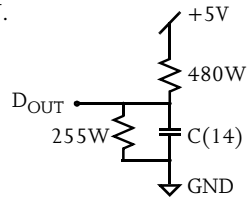


Figure B: 5V Output load

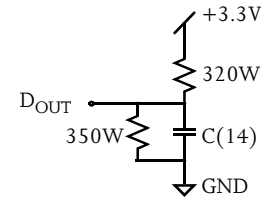
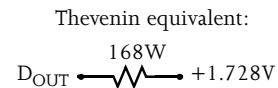


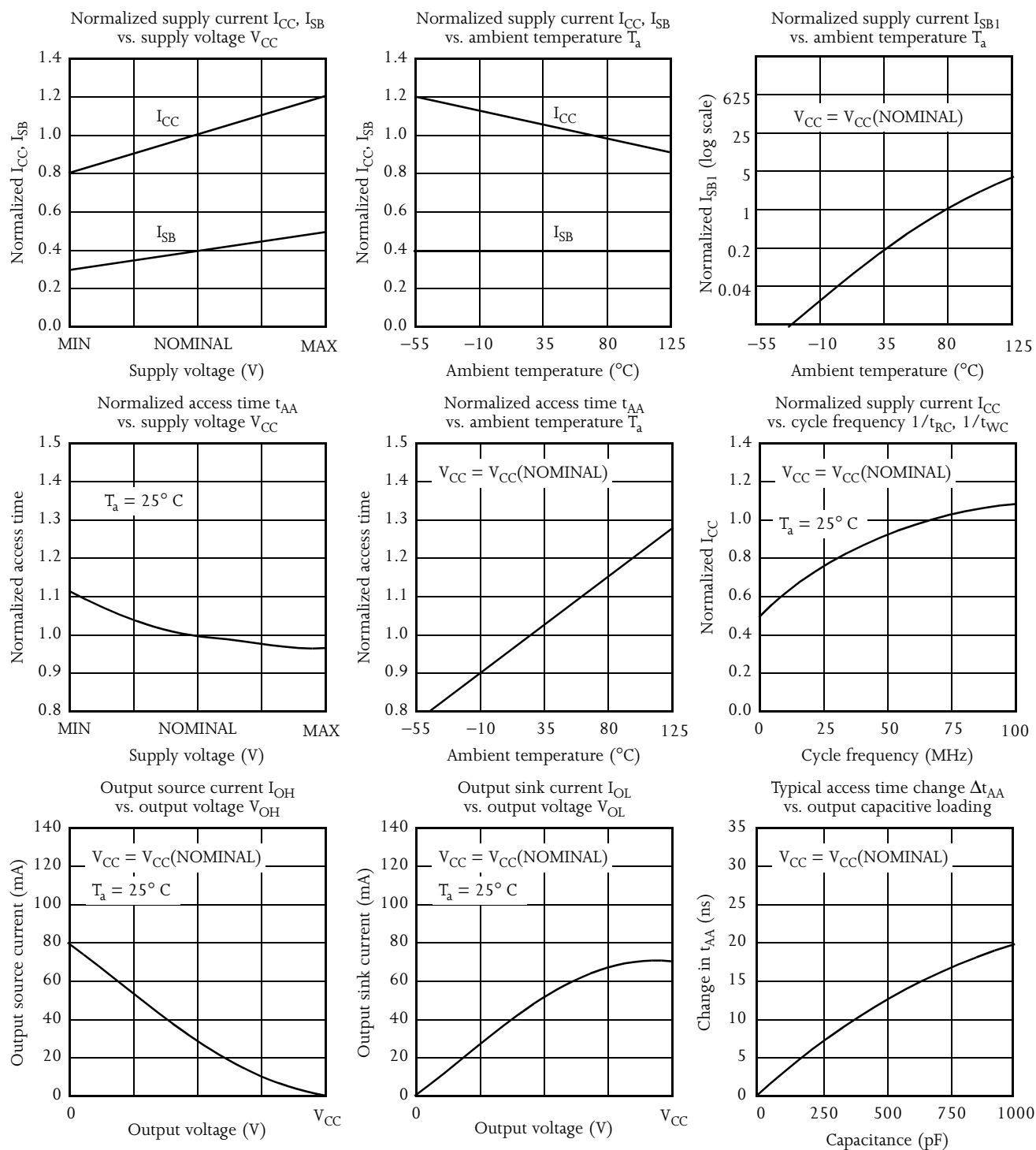
Figure C: 3.3V Output load

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions.
- 4 t_{CLZ} and t_{CHZ} are specified with $C_L = 5pF$ as in Figure C. Transition is measured ± 500 mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6 $\overline{WE}$ is HIGH for read cycle.
- 7 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
- 8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 2V data retention applies to commercial temperature range operation only.
- 14 $C = 30pF$, except at high Z and low Z parameters, where $C = 5pF$.

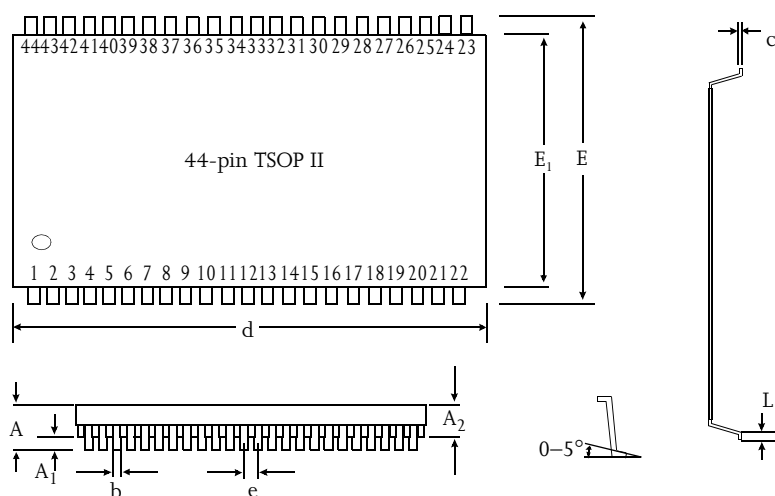


Typical DC and AC characteristics 12

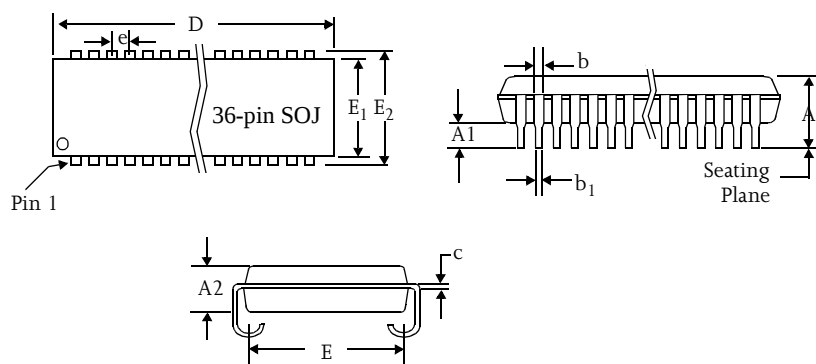




Package dimensions



	44-pin TSOP II	
	Min(mm)	Max(mm)
A		1.2
A_1	0.05	0.15
A_2	0.95	1.05
b	0.30	0.45
c	0.15 (typical)	
d	18.28	18.54
E_1	10.03	10.16
E	11.56	11.96
e	0.80 (typical)	
L	0.40	0.60



	36-pin SOJ 400	
	Min(mils)	Max(mils)
A	.128	0.148
A_1	0.027	—
A_2	0.102 NOM	
b	0.015	0.020
b_1	0.026	0.032
c	0.007	0.013
D	.920	.930
e	0.045	0.055
E	0.400 NOM	
E	0.435	0.445

Ordering codes

Package	Version	10 ns	12 ns	15 ns	20 ns
SOJ	5V commercial	NA	AS7C4096-12JC	AS7C4096-15JC	AS7C4096-20JC
	5V industrial	NA	AS7C4096-12JI	AS7C4096-15JI	AS7C4096-20JI
	3.3V commercial	AS7C4096-10JC	AS7C34096-12JC	AS7C34096-15JC	AS7C34096-20JC
	3.3V industrial	NA	AS7C34096-12JI	AS7C34096-15JI	AS7C34096-20JI
TSOP II	5V commercial	NA	AS7C4096-12TC	AS7C4096-15TC	AS7C4096-20TC
	5V industrial	NA	AS7C4096-12TI	AS7C4096-15TI	AS7C4096-20TI
	3.3V commercial	AS7C4096-10TC	AS7C34096-12TC	AS7C34096-15TC	AS7C34096-20TC
	3.3V industrial	NA	AS7C34096-12TI	AS7C34096-15TI	AS7C34096-20TI

NA: not available.



Part numbering system

AS7C	X	4096	-XX	J, T	X
SRAM prefix	Blank: 5V CMOS 3: 3.3V CMOS	Device number	Access time	Package: J: 400-mil SOJ T: 400-mil TSOP II	Temperature ranges: C: Commercial, 0° C to 70° C I: Industrial, -40° C to 85° C

