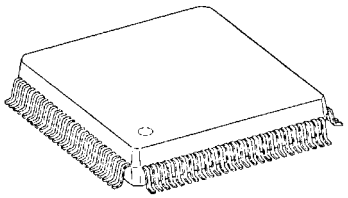
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC94A15F

Single-Chip Digital Servo Processor Incorporating CD Head Amplifier

The TC94A15F is a single chip processor which incorporates the following functions: CD system synchronous separation protection and interpolation, EFM demodulation, error system and correction, microcontroller interface, servo-use digital equalizer and servo control circuit, and 1-bit DA converter.

In addition, the TC94A15FG incorporates a head amplifier, which makes it possible to configure a CD player quite easily on an adjustment-free basis.



LQFP100-P-1414-0.50C

Weight: 0.65 g (typ.)

Features

Common to all sections

- Supports the ×1, ×2, and ×4 speeds for CD playback.
  - CD-DA mode: ×1, ×2, and ×4 speeds are supported.
    - (×4 speed in CD-DA mode is supported only for analog slicing.)
  - CD-RW mode: ×1 and ×2 speeds are supported.
- Built-in microcontroller interface circuit
- Operates at high speed with low power consumption because of a CMOS silicon structure.
- Packed in a flat package having 100 pins (0.5 mm pitch).

Head amplifier section

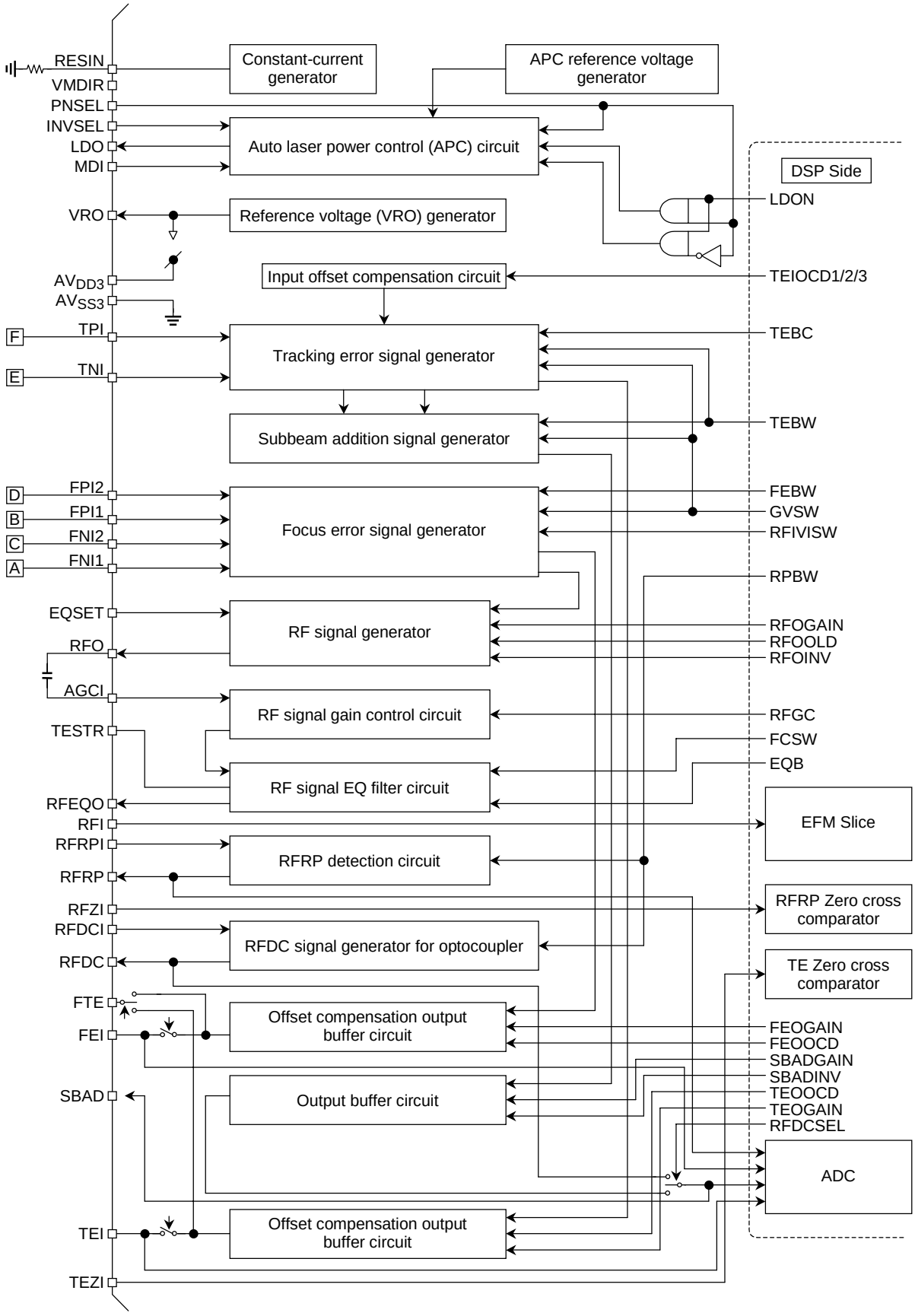
- Built-in reference voltage (VRO) generation circuit
- Built-in APC (auto laser power control) circuit
- Enables either NPN or PNP transistors, whichever are selected, to be used in the APC circuit (LDO).
- Enables the input polarity of the monitor diode (MDI) to be switched.
- Built-in RF signal generation circuit
- Enables the polarity of the offset voltage correction of the RF signal to be switched.
- Built-in AGC (auto gain control) circuit for the RF signal (gain adjustment range of ±6 dB)
- Built-in RF equalizer correction circuit
- Built-in focus error signal and tracking error signal circuits
- Built-in signal generation circuit for track counting
- Built-in circuit for generating a subbeam addition signal or an RFDC signal, whichever is selected, as a defect detection signal.
  (Note that the RFDC signal is supported only when the RFO signal is positive.)
- Supports DC offset correction functions (for focus, tracking, and RF sections).
- Supports both CD-DA and CD-R/RW modes.
- Supports a voltage output type pickup.

Digital servo processor section

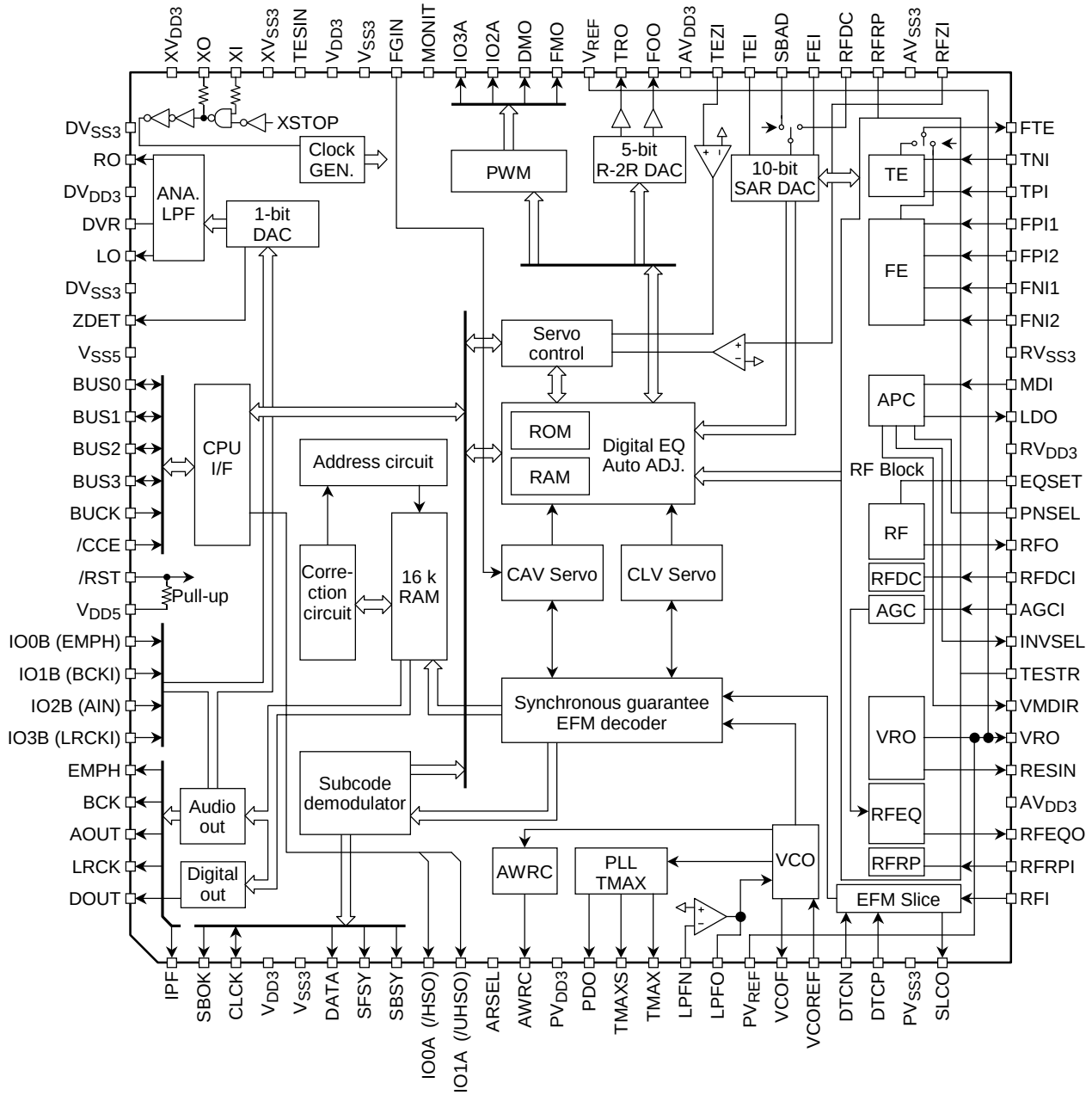
- Capable of decoding text data (CD-TEXT).
- Capable of performing sync pattern detection, sync signal protection and interpolation securely.
- Built-in EFM demodulation circuit and subcode demodulation circuit
- Has a jitter absorbing capacity of ±6 frames.
- Capable of making double C1 correction and quadruple C2 correction, using CIRC correction logical expressions.
- Built-in 16-KB RAM

- Built-in digital-out circuit
  (supporting up to ×2 speed, or 16.9344 MHz, and up to ×4 speed, or 33.8688 MHz, in the CLV mode)
- Built-in independent left and right digital attenuators
- Supports bilingual audio outputs.
- Enables audio outputs to be switched among 32 fs, 48 fs, and 64 fs.
- Capable of reading subcode Q data at any time and outputting it in synchronization with audio data.
- Built-in data slice circuit (switchable between analog and digital slicing)
- Built-in analog PLL (with an adjustment-free VCO)
- Uses an active wide-range PLL system.
- Supports variable-speed playback.
- Built-in CAV control circuit, supporting switching between the CAV and CLV modes
- Supporting automatic loop gain, offset, and balance adjustments for focus and tracking servo sections.
- Built-in RF gain automatic adjustment circuit
- Built-in digital equalizer
- Built-in digital equalizer coefficient RAM, supporting various pickup types
- Built-in focus and tracking servo control circuits
- Supports all search control modes, thus realizing high-speed stable searches.
- Uses speed-controlled lens kick and feed kick.
- Built-in AFC and APC circuits for disc motor CLV servo control
- Built-in anti-defect and anti-shock circuits
- Built-in ×8 over-sampling digital filter and 1-bit DA converter (for up to ×2 speed)
- Built-in analog filter for a 1-bit DA converter (for up to ×2 speed)
- Supports externally input BCK, LRCK, AOUT, and EMPH signals (for up to ×2 speed).

Head amplifier block diagram



Block diagram (top view)



Pin Function

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Functional Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>IPF</td><td>O
3-5I/F</td><td>Correction flag output pin.
"H" if the AOUT output is an uncorrectable symbol in C2 correction.</td><td>—</td></tr>
<tr><td>2</td><td>SBOK</td><td>O
3-5I/F</td><td>CRCC check result output pin for subcode Q data.
“H” if the check result is OK.</td><td>—</td></tr>
<tr><td>3</td><td>CLCK</td><td>I/O
3-5I/F</td><td>Clock input/output pin for reading subcode P to W data.
The polarity of the input/output can be selected with a command.</td><td>—</td></tr>
<tr><td>4</td><td>V_{DD3}</td><td>—</td><td>Power supply pin for 3.3 V digital circuits.</td><td>—</td></tr>
<tr><td>5</td><td>V_{SS3}</td><td>—</td><td>Grounding pin for digital circuits.</td><td>—</td></tr>
<tr><td>6</td><td>DATA</td><td>O
3-5I/F</td><td>Subcode P to W data output pin.</td><td>—</td></tr>
<tr><td>7</td><td>SFSY</td><td>O
3-5I/F</td><td>Playback section frame sync signal output pin.</td><td>7.35 kHz</td></tr>
<tr><td>8</td><td>SBSY</td><td>I/O
3-5I/F</td><td>Subcode block sync output pin.
"H" in the S1 position when a subcode sync is detected.</td><td>—</td></tr>
<tr><td>9</td><td>IO0A
(/HSO)</td><td>I/O
3-5I/F</td><td rowspan="2">Input/output pin for general-purpose I/O devices.
(Playback speed mode flag output pin.)
<table><tr><th>/UHSO</th><th>/HSO</th><th>Playback speed</th></tr><tr><td>H</td><td>H</td><td>×1 speed</td></tr><tr><td>H</td><td>L</td><td>×2 speed</td></tr><tr><td>L</td><td>H</td><td>×4 speed</td></tr></table></td><td rowspan="2">Command bits can be used to select which function of the dual function pin to use (general-purpose input or output (input is selected upon a reset) or speed mode flag).</td></tr>
<tr><td>10</td><td>IO1A
(/UHSO)</td><td>I/O
3-5I/F</td></tr>
<tr><td>11</td><td>ARSEL</td><td>I
3I/F</td><td>Usually fixed at "H" level.</td><td>—</td></tr>
<tr><td>12</td><td>AWRC</td><td>O
3AI/F</td><td>VCO control pin for active wide-range PLL.</td><td>Controllable in CLV/CAV mode.</td></tr>
<tr><td>13</td><td>PV_{DD3}</td><td>—</td><td>3.3 V power supply pin dedicated to the PLL section.</td><td>—</td></tr>
<tr><td>14</td><td>PDO</td><td>O
3AI/F</td><td>Signal output pin for phase difference between EFM and PLCK signals.</td><td>4-value output.
(PV_{DD3}, HiZ, PV_{SS}, PV_{REF})</td></tr>
<tr><td>15</td><td>TMAXS</td><td>O
3AI/F</td><td rowspan="2">TMAX detection result output pin.
The same signal is output from the TMAX and TMAXS pins.</td><td rowspan="2">3-value output.
(PV_{DD3}, PV_{SS}, HiZ)</td></tr>
<tr><td>16</td><td>TMAX</td><td>O
3AI/F</td></tr>
<tr><td>17</td><td>LPFN</td><td>I
3AI/F</td><td>Inversion input pin for PLL section low-pass filter amplifier.</td><td>To be connected on the resistor side.
See the application circuit diagram.</td></tr>
<tr><td>18</td><td>LPFO</td><td>O
3AI/F</td><td>Output pin for PLL section low-pass filter amplifier.</td><td>To be connected on the capacitor side.
See the application circuit diagram.</td></tr>
<tr><td>19</td><td>PV_{REF}</td><td>—</td><td>1.65 V reference voltage pin dedicated to the PLL section.</td><td>Connected to V_{REF} and VRO within the IC package. To be connected to 0.1 μF.</td></tr>
<tr><td>20</td><td>VCOF</td><td>O
3AI/F</td><td>VCO filter pin.</td><td>Connect a 0.01 μF capacitor between VCOF and PV_{SS3}.</td></tr>
<tr><td>21</td><td>VCOREF</td><td>I
3AI/F</td><td>Input pin for VCO center frequency reference level.</td><td>To be connected to PV_{REF} if AWRC is left unused.</td></tr>
<tr><td>22</td><td>DTCN</td><td>O
3AI/F</td><td>Analog slicer filter pin</td><td rowspan="2">To be connected to 0.022 μF.</td></tr>
<tr><td>23</td><td>DTCP</td><td>O
3AI/F</td><td>Analog slicer filter pin</td></tr>
<tr><td>24</td><td>PV_{SS3}</td><td>—</td><td>Grounding pin dedicated to the PLL section.</td><td>—</td></tr>
</table>

Pin No.	Symbol	I/O	Functional Description	Remarks
25	SLCO	O 3AI/F	EFM slice level output pin.	Select a capacitor to be connected according to the servo bandwidth.
26	RFI	I 3AI/F	RF signal input pin. An input resistance can be selected using a command.	Zin: 20 kΩ, 10 kΩ, 5 kΩ
27	RFRPI	I 3AI/F	RF ripple signal input pin.	—
28	RFEQO	O 3AI/F	RF equalizer circuit output pin.	To be connected to RFRPI via 0.1 μF and to RFI via 4700 pF or more.
29	AV_{DD3}	—	Power supply pin for 3.3 V analog circuits.	—
30	RESIN	I 3AI/F	Pin for connecting a resistor for reference current generation.	To be connected to 22 kΩ/ 680 pF.
31	VRO	O 3AI/F	1.65 V reference voltage output pin.	Connected to V_{REF} and PV_{REF} within the IC package. To be connected to 0.1 μF and 47 μF.
32	VMDIR	—	1.533 V reference voltage output pin.	Reference voltage for APC circuit. To be connected to 0.1 μF.
33	TESTR	O 3AI/F	Pin for connecting filter for RFEQO offset correction.	To be connected to 0.015 μF or more.
34	INVSEL	I 3AI/F	Pin for MDI input polarity select input. "L": Normal input. "H": Inverted input.	—
35	AGCI	I 3AI/F	Input pin for RF signal amplitude adjustment amp.	To be connected to RFO via 0.1 μF.
36	RFDCI	I 3AI/F	Input pin for RF signal peak detection.	To be connected directly to RFO.
37	RFO	O 3AI/F	Output pin for RF signal generation amp.	To be connected directly to RFDCI and, via 0.1 μF, to AGCI.
38	PNSEL	I 3AI/F	Pin for selecting an LDO connection transistor type for APC circuit.	L: NPN, H: PNP
39	EQSET	O 3AI/F	External-connection pin for RF signal equalizer.	Kept open when RFEQ is used.
40	RV_{DD3}	—	Power supply pin for 3.3 V RF amp core section.	—
41	LDO	O 3AI/F	Laser diode amp output pin.	—
42	MDI	I 3AI/F	Monitor photodiode amp input pin.	With reference to 178 mV (typ.)
43	RV_{SS3}	—	Grounding pin for RF amp core section.	—
44	FNI2	I 3AI/F	Main beam input pin. To be connected to PIN diode C.	—
45	FNI1	I 3AI/F	Main beam input pin. To be connected to PIN diode A.	—
46	FPI2	I 3AI/F	Main beam input pin. To be connected to PIN diode D.	—
47	FPI1	I 3AI/F	Main beam input pin. To be connected to PIN diode B.	—
48	TPI	I 3AI/F	Subbeam input pin. To be connected to PIN diode F.	—
49	TNI	I 3AI/F	Subbeam input pin. To be connected to PIN diode E.	—
50	FTE	O 3AI/F	Focus/tracking signal output pin. (Test pin for servo characteristic measurement.)	Either focus signal or tracking signal is selected using a command.
51	RFZI	I 3AI/F	Input pin for RF ripple zero-cross signal.	To be connected to RFRP via 0.033 μF.
52	AV_{SS3}	—	Grounding pin for analog circuits.	—

Pin No.	Symbol	I/O	Functional Description	Remarks
53	RFRP	O 3AI/F	RF ripple signal output pin.	To be connected to RFZI via 0.033 μF.
54	RFDC	O 3AI/F	Pin for the RF peak detection signal supporting hologram.	Pins for monitoring various signals.
55	FEI	O 3AI/F	Focus error signal pin.	
56	SBAD	O 3AI/F	Subbeam addition signal pin.	
57	TEI	O 3AI/F	Tracking error signal pin.	
58	TEZI	I 3AI/F	Input pin for tracking error signal zero-cross.	To be connected to TEI via 0.033 μF.
59	AV_{DD3}	—	Power supply pin for 3.3 V analog circuits.	—
60	FOO	O 3AI/F	Focus equalizer output pin. (Note)	—
61	TRO	O 3AI/F	Tracking equalizer output pin. (Note)	
62	V_{REF}	O 3AI/F	Reference voltage pin for analog circuits.	Connected to VRO and PV_{REF} within the IC package. To be connected to 0.1 μF.
63	FMO	O 3AI/F	Speed error/feed equalizer output pin. (Note)	PWM 3-value output. (AV_{DD3}, AV_{SS3}, V_{REF})
64	DMO	O 3AI/F	Disc equalizer output pin. (Note)	
65	IO2A	I/O 3AI/F	Input/output pin for general-purpose I/O devices	Input is selected at a reset.
66	IO3A	I/O 3AI/F		
67	MONIT	O 3AI/F	Pin for monitoring signals in the DSP	At this pin, flags in the DSP and PLL-circuit clock pulses can be monitored, using microcontroller commands. The pin can be used also to output text data serially.
68	FGIN	I 3AI/F	FG signal input pin for CAV. CLV: "L", CAV: FG input	—
69	V_{SS3}	—	Grounding pin for digital circuits.	—
70	V_{DD3}	—	Power supply pin for 3.3 V digital circuits.	—
71	TESIN	I 3AI/F	Test input pin, usually fixed at "L" level.	—
72	XV_{SS3}	—	Grounding pin for system clock oscillator circuit.	—
73	XI	I 3AI/F	Input pin for system clock oscillator circuit.	—
74	XO	O 3AI/F	Output pin for system clock oscillator circuit.	This pin is used to take system clock oscillator output into the MCK. It is “H” when the microcontroller command is XSTOP.
75	XV_{DD3}	—	Power supply pin for 3.3 V system clock oscillator circuit.	—
76	DV_{SS3}	—	Grounding pin for 1-bit DAC.	No capacitor is to be connected to the DVR pin if the built-in 1-bit DAC is not used. In this case, however, 3.3 V must be supplied across DV_{DD3} and DV_{SS3}.
77	RO	O 3AI/F	R channel data normal output pin for 1-bit DAC.	
78	DV_{DD3}	—	3.3 V power supply pin for 1-bit DAC.	
79	DVR	O	Reference voltage pin for 1-bit DAC.	
80	LO	O 3AI/F	L channel data normal output pin for 1-bit DAC.	
81	DV_{SS3}	—	Grounding pin for 1-bit DAC.	

Pin No.	Symbol	I/O	Functional Description	Remarks
82	ZDET	O 3-5I/F	Zero detection flag output pin for 1-bit DAC.	This pin is valid also when external inputs are supplied to the 1-bit DAC.
83	V_{SS5}	—	Grounding pin for interfaces	—
84	BUS0	I/O 3-5I/F	Data input/output pin for the microcontroller interface.	When 3.3 V is supplied to V_{DD5}, the output level of each interface pin (82, 84-87, 92-100, 1-3, and 6-10) is -VDD5 with reference to a ground. To be fixed at "H" or "L" when communication is not in progress, so the pin will not become Hiz.
85	BUS1	I/O 3-5I/F		
86	BUS2	I/O 3-5I/F		
87	BUS3	I/O 3-5I/F		
88	BUCK	I 3-5I/F	Clock input pin for the microcontroller interface.	To be fixed at "H" when communication is not in progress, so the pin will not become Hiz.
89	/CCE	I 3-5I/F	Chip enable signal input pin for the microcontroller interface. BUS3 to BUS0 are active if this pin is “L”.	
90	/RST	I 3-5I/F	Reset signal input pin. The internal registers and servo section registers are reset, respectively, when the reset signal is “L” and on the rising edge of the reset signal.	The XSTOP mode is released when /RST changes like: "H" → "L" → "H" To be connected to 0.1 μF.
91	V_{DD5}	—	Power supply pin for the interface.	5 or 3.3 V is supplied.
92	IO0B (EMPHI)	I/O 3-5I/F	General-purpose I/O pin. (1-bit DAC external input: EMPH.) (Flag output: A.)	Command bits are used to switch among general-purpose I/O (input is selected at a reset), flag output, and 1-bit DAC external input.
93	IO1B (BCKI)	I/O 3-5I/F	General-purpose I/O pin. (1-bit DAC external input: BCK.) (Flag output: B.)	
94	IO2B (AIN)	I/O 3-5I/F	General-purpose I/O pin. (1-bit DAC external input: AIN.) (Flag output: C.)	
95	IO3B (LRCK)	I/O 3-5I/F	General-purpose I/O pin. (1-bit DAC external input: LRCK.) (Flag output: D.)	
96	EMPH	O 3-5I/F	Emphasis flag output pin. ENPH on: “H”. EMPH off: “L”. The output polarity is switched, using a command.	—
97	BCK	O 3-5I/F	Bit clock output pin. 32 fs, 48 fs, and 64 fs can be selected, using a command.	×1 speed: 32 fs = 1.4112 MHz.
98	AOUT	O 3-5I/F	Audio data output pin. Which bit is first (MSB first or LSB first) can be selected, using a command.	—
99	LRCK	O 3-5I/F	LR channel clock output pin. “L” for the L-channel and “H” for the R-channel. The output polarity can be inverted, using a command.	×1 speed: 32 fs = 44.1 kHz.
100	DOUT	O 3-5I/F	Digital-out output pin.	As per CP-1201.

*: 3A I/F : 3 V analog circuit input/output pin.
3-5 I/F : 3-5 built-in interface pin (5 V input/output pin).
3 I/F : 3 V digital circuit input/output pin.

Note: The servo output pins (FOO, TRO, FMO, and DMO) become undefined under the following conditions:
- /RST pin = Low
- Crystal oscillation stopped according to the instructions by the Stop crystal oscillation command

To prevent the undefined pin states from affecting the servo circuitry or any other mechanical blocks in the system, appropriate measures should be taken, such as using a driver IC supporting a standby feature to place the system in standby mode while either of the above conditions is satisfied.

Maximum rating (unless otherwise specified, referred to ground and Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD5}	−0.3~6.0	V	91-83 pin
	V_{DD3}	−0.3~4.5		4-5, 70-69 pin 13-24, 40-43 pin 29, 59-52 pin 75-72 pin 78-76, 81 pin
Input voltage	V_{IN5}	−0.3~V_{DD5} + 0.3	V	3, 9~10, 84~90 pin 92~95 pin
	V_{IN3}	−0.3~V_{DD3} + 0.3		11, 17, 26, 27 pin 30, 34~36, 38 pin 42, 44~49, 51 pin 58, 65, 66, 68 pin 71, 73 pin
Permissible loss	P_D	1910	mW	—
Operating temperature	T_{opr}	−40~+85	°C	—
Storage temperature	T_{stg}	−55~+150	°C	—

Electrical characteristics

■RF core section

(unless otherwise specified, V_{DD5} = 5 V, V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = PV_{DD3} = 3.3 V, and Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Power supply voltage									
	Guaranteed-operation supply voltage	V_{DD3}	—	—		3.0	3.3	3.6	V
	Supply current	I_{DD3}	—	CMD: D4400E (FCSW = 00 for ×1 speed)		—	45	60	mA
Reference voltage									
	Reference voltage	VRO	—	—		—	1.65	—	V
	Output drain current	I_{OH}	—	ΔV = −0.1 V		3	—	—	mA
	Output sink current	I_{OL}		ΔV = +0.1 V		3	—	—	
APC section (MDI → LDO) MDI → LDO									
	Internal reference voltage	VMDIR	—	—		—	1.5	—	V
	Voltage gain 1	G_{VAPC1}	—	Ff = 1 kHz, normal-polarity LDO		—	200	—	V/V
	Voltage gain 2	G_{VAPC2}		Ff = 1 kHz, inverted-polarity LDO		—	−200	—	
	Operation reference voltage 1	V_{MDI1}	—	V_{LDO} = V_{DD} − 1.3 V, normal-polarity LDO		—	178	—	mV
	Operation reference voltage 2	V_{MDI2}		V_{LDO} = ground + 1.3 V, inverted-polarity LDO		—	178	—	
	LD-off voltage 1	V_{LDOP1}	—	VDD reference, CMD: LD-OFF, PNP		—	−0.2	—	V
	LD-off voltage 2	V_{LDOP2}		GND reference, CMD: LD-OFF, NPN		—	0.2	—	
	Input bias current	I_{APC}	—	$V_{MDI1/2}$ = 178 mV		−1	—	1	μA
RF section (FPI1/FPI2 (FNI1/FNI2) → RFO)									
	Voltage gain & variable range 1 (CD-DA mode)	G_{VA11RF}	—	f = 0.5Vpp/ 100 kHz, CMD: GVSW = 1	RFOGAINi = 0000	—	−6	—	dB
		G_{VA12RF}			RFOGAINi = 1111	—	12	—	
	Voltage gain & variable range 2 (CD-RW mode)	G_{VA21RF}		f = 0.5 Vpp/ 100 kHz, CMD: GVSW = 0	RFOGAINi = 0000	—	6	—	
		G_{VA22RF}			RFOGAINi = 1111	—	24	—	
	Frequency characteristic 1 (CD-DA mode) (Note 1)	f_{C1RF}	—	−3dB point, CMD: GVSW = 1, RFOGAINi = 1000		—	16	—	MHz
	Frequency characteristic 2 (CD-RW mode) (Note 1)	f_{C2RF}		−3 dB point, CMD: GVSW = 1, RFOGAINi = 1000		—	6	—	
	Output slew rate	SR_{RF}	—	C_{RFO} = 20 pF		10	20	—	V/μs
	Output upper-limit voltage	V_{OHRF}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLRF}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMRF}	—	—		5	10	—	kΩ

Note 1: Design guarantee.

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
AGC+RFEQ section (AGCI → RFEQO)								
Voltage gain 1 (Note 2)	G_{V1AGC}	—	f = 100 kHz	RFGC = 80h	—	−7.8	−6	dB
Voltage gain 2 (Note 2)	G_{V2AGC}			RFGC = 00h	—	0	—	
Voltage gain 3 (Note 2)	G_{V3AGC}			RFGC = 7Fh	6	7.8	—	
Peak frequency 1 (×1 speed mode)	f_{C1EQ}	—	CMD: D4C00E (Boost Max), RFGC = 00h		0.9	—	1.8	MHz
Peak frequency 2 (×2 speed mode)	f_{C2EQ}		CMD: D4C10E (Boost Max), RFGC = 00h		1.7	—	3.4	
Peak frequency 3 (×4 speed mode)	f_{C3EQ}		CMD: D4C20E (Boost Max), RFGC = 00h		3.3	—	6.6	
Group delay difference 11 (×1 speed mode) (Note 3)	GD_{1EQ}	—	CMD: D4400E, RFGC = 00h, f = 100 kHz (reference) to 1 MHz		−20	—	20	ns
Group delay difference 21 (×2 speed mode) (Note 3)	GD_{2EQ}		CMD: D4410E, RFGC = 00h, f = 200 kHz (reference) to 2 MHz		−10	—	10	
Group delay difference 31 (×4 speed mode) (Note 3)	GD_{3EQ}		CMD: D4420E, RFGC = 00h, f = 400 kHz (reference) to 4 MHz		−6	—	6	
Peak gain difference 11 (×1 speed mode) (Note 3)	fV_{1EQ}	—	f = 100 kHz (reference), RFGC = 00h, CMD: D4C00E (Boost Max)		—	5	—	dB
Peak gain difference 21 (×2 speed mode) (Note 3)	fV_{2EQ}		f = 100 kHz (reference), RFGC = 00h, CMD: D4C10E (Boost Max)		—	5	—	
Peak gain difference 31 (×4 speed mode) (Note 3)	fV_{3EQ}		f = 100 kHz (reference), RFGC = 00h, CMD: D4C20E (Boost Max)		—	5	—	
Output slew rate	SR_{AGC}	—	C_{RFEQO} = 20 pF		10	20	—	V/us
Output upper-limit voltage	V_{OHAGC}	—	GND reference		2.9	3.1	—	V
Output lower-limit voltage	V_{OLAGC}		GND reference		—	0.3	0.5	
Permissible load resistance	R_{LMAGC}	—	—		5	10	—	kΩ

Note 2: These values were measured in the AGC-AMP section.

Note 3: These values were measured in the RFEQ section. Design guarantee.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
FE section (FPI1/FPI2 (FNI1/FNI2) → FEI)									
	Voltage gain & variable range 1 (CD-DA mode)	G_{VA11FE}	—	f = 0.5Vpp/1kHz, CMD: GVSW = 1	FEOGAINi = 0000	—	−2.8	—	dB
		G_{VA12FE}			FEOGAINi = 1111	—	21.5	—	
	Voltage gain & variable range 2 (CD-RW mode)	G_{VA21FE}		f = 0.5Vpp/1kHz, CMD: GVSW = 0	FEOGAINi = 0000	—	9.5	—	
		G_{VA22FE}			FEOGAINi = 1111	—	33.5	—	
	Gain balance 1 (CD-DA mode)	GB_{1FE}	—	ΔG_{VA1*FE}		−1	0	+1	dB
	Gain balance 2 (CD-RW mode)	GB_{2FE}		ΔG_{VA2*FE}		−1	0	+1	
	Frequency characteristic 1 (CD-DA mode)	f_{C1FE}	—	−3dB point, CMD: FEBW = 0, CMD: GVSW = 1		—	29	—	kHz
	Frequency characteristic 2 (CD-RW mode)	f_{C2FE}		−3dB point, CMD: FEBW = 0, CMD: GVSW=0		—	29	—	
	Frequency characteristic 3 (CD-DA mode)	f_{C3FE}		−3dB point, CMD: FEBW = 1, CMD: GVSW = 1		—	44	—	
	Frequency characteristic 4 (CD-RW mode)	f_{C4FE}		−3dB point, CMD: FEBW = 1, CMD: GVSW = 0		—	44	—	
	Output offset voltage 1 (CD-DA mode) (Note 4)	V_{OF1FE}	—	VRO reference, FPI1/FPI2/FNI1/FNI2 open FEBC = 00h, CMD: GVSW = 1		−50	—	+50	mV
	Output offset voltage 2 (CD-RW mode) (Note 4)	V_{OF2FE}		VRO reference, FPI1/FPI2/FNI1/FNI2 open FEBC = 00h, CMD: GVSW = 0		−50	—	+50	
	Output upper-limit voltage	V_{OHFE}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLFE}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMFE}	—	—		10	15	—	kΩ

Note 4: These values are those for which offset correction is completed.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
TE section (TPI (TNI) → TEI)									
Voltage gain & variable range 1 (CD-DA mode)		G_{VA11TE}	—	f = 0.5Vpp/1 kHz, TEBC = 00h, CMD: GVSW = 1	TEOGAINi = 0000	—	8.5	—	dB
		G_{VA12TE}			TEOGAINi = 1111	—	32	—	
Voltage gain & variable range 2 (CD-RW mode)		G_{VA21TE}		f = 0.5Vpp/1 kHz, TEBC = 00h, CMD: GVSW = 0	TEOGAINi = 0000	—	20.5	—	
		G_{VA22TE}			TEOGAINi = 1111	—	44	—	
Gain balance adjustment width	H (DA)	ΔR_{T1TE}	—	TEBC = 7Fh		+50	+60	—	%
	L (DA)	ΔR_{T2TE}		TEBC = 80h		—	−60	−50	
Gain balance 1 (CD-DA mode)		GB_{1TE}	—	ΔG_{VA1*TE}		−1	0	+1	dB
Gain balance 2 (CD-RW mode)		GB_{2TE}		ΔG_{VA2*TE}		−1	0	+1	
Frequency characteristic 1 (CD-DA mode)		f_{C1TE}	—	−3dB point, CMD: TEBW = 0, CMD: GVSW = 1		—	29	—	kHz
Frequency characteristic 2 (CD-RW mode)		f_{C2TE}		−3dB point, CMD: TEBW = 0, CMD: GVSW = 0		—	29	—	
Frequency characteristic 3 (CD-DA mode)		f_{C3TE}		−3dB point, CMD: TEBW = 1, CMD: GVSW = 1		—	44	—	
Frequency characteristic 4 (CD-RW mode)		f_{C4TE}		−3dB point, CMD: TEBW = 1, CMD: GVSW = 0		—	44	—	
Output offset voltage 1 (CD-DA mode) (Note 5)		V_{OF1TE}	—	VRO reference, TPI/TNI open, TEBC = 00h CMD: GVSW = 1		−50	—	+50	mV
Output offset voltage 2 (CD-RW mode) (Note 5)		V_{OF2TE}		VRO reference, TPI/TNI open, TEBC = 00h CMD: GVSW = 0		−50	—	+50	
Output upper-limit voltage		V_{OHTE}	—	GND reference		2.9	3.1	—	V
Output lower-limit voltage		V_{OLTE}		GND reference		—	0.3	0.5	
Permissible load resistance		R_{LMTE}	—	—		10	15	—	kΩ

Note 5: These values are those for which offset correction is completed.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
RFRP section (RFRPI → RFRP)									
	Voltage gain 1	G_{V1RP}	—	RFRPI input amp gain	RFRPGi = 00	—	2.2	—	dB
	Voltage gain 2	G_{V2RP}			RFRPGi = 01	—	3.4	—	
	Voltage gain 3	G_{V3RP}			RFRPGi = 10	—	4.4	—	
	Voltage gain 4	G_{V4RP}			RFRPGi = 11	—	5.3	—	
	Detection frequency 1 (Note 6)	f_{1RP}	—	−3dB point with reference to low-frequency side on the assumption that RFRPI = 1.2 Vpp for V_{OP1RP} and output amplitude = 0dB for a 700 kHz sine wave input.	RPBW = 0	—	50	—	kHz
	Detection frequency 2 (Note 6)	f_{2RP}			RPBW = 1	—	100	—	
	Detection constant 1	T_{1RP}	—	RFRPI = 1.2 Vpp for V_{OP1RP} and slew rate (Cin > 1 μF) for a 5 kHz rectangular wave input.	RPBW = 0	—	35	—	V/ms
	Detection constant 2	T_{2RP}			RPBW = 1	—	70	—	
	Operating reference voltage 1	V_{OP1RP}	—	VRO reference, no input		−1.05	—	−0.75	V
	Operating reference voltage 2	V_{OP2RP}		VRO reference, RFRPI = 1.2Vpp/700 kHz		0.3	—	0.75	
	Output upper-limit voltage	V_{OHRP}	—	GND reference		2.9	3.1	—	V
	Permissible load resistance	R_{LMRP}	—	—		10	15	—	kΩ
RFDC section (FPI1/FPI2 (FNI1/FNI2) → RFDC)									
	Detection frequency 1 (Note 6)	f_{1DC}	—	−3dB point with reference to low-frequency side on the assumption that RFDCI = 1.2 Vpp for V_{OP1DC} and output amplitude = 0dB for a 700 kHz sine wave input.	RPBW = 0	—	20	—	kHz
	Detection frequency 2 (Note 6)	f_{2DC}			RPBW = 1	—	40	—	
	Detection constant 1	T_{1DC}	—	RFDCI = 1.2 Vpp for V_{OP1DC} and slew rate (Cin > 1 μF) for a 5 kHz rectangular wave input.	RPBW = 0	—	14	—	V/ms
	Detection constant 2	T_{2DC}			RPBW = 1	—	28	—	
	Operating reference voltage 1	V_{OP1DC}	—	VRO reference, FPI1/FPI2/FNI1/FNI2 open, CMD: RFOOLDi = 00		−0.35	—	+0.1	V
	Operating reference voltage 2	V_{OP2DC}		VRO reference, RFDCI = 1.2Vpp/350 kHz, CMD: RFOOLDi = 00		0.2	—	0.55	
	Output upper-limit voltage	V_{OHDC}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLDC}		GND reference		—	0.5	0.75	
	Permissible load resistance	R_{LMDC}	—	—		20	25	—	kΩ

Note 6: The detection frequency values are for only reference purposes.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
SBAD section (TPI (TNI) → SBAD)									
	Voltage gain 1 (CD-DA mode)	G_{V1SB}	—	f = 1kHz, TEBC = 00h CMD: GVSW = 1	SBADGAINi = 0000	—	−3.0	—	dB
					SBADGAINi = 1111	—	21.0	—	
	Voltage gain 2 (CD-RW mode)	G_{V1SB}		f = 1kHz, TEBC = 00h CMD: GVSW = 0	SBADGAINi = 0000	—	9.0	—	
					SBADGAINi = 1111	—	33.0	—	
	Frequency characteristic	f_{CSB}	—	−3dB point		—	44	—	kHz
	Operating reference voltage 1 (CD-DA mode)	V_{OP1SB}	—	VRO reference No input SBADINV = 0		−1.1	−0.8	−0.5	V
	Operating reference voltage 2 (CD-RW mode)	V_{OP2SB}				−1.1	−0.8	−0.5	
	Output upper-limit voltage	R_{OHSB}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	R_{OLSB}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMSB}	—	—		10	15	—	kΩ

■DSP core section

DC characteristics (1)

(unless otherwise specified, V_{DD5} = 5 V, V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = RV_{DD3} = PV_{DD3} = 3.3 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage		V_{DD5}	—	—	4.5	5.0	5.5	V
		V_{DD3}			3.0	3.3	3.6	
		AV_{DD3}						
		DV_{DD3}						
		PV_{DD3}						
		RV_{DD3}						
		XV_{DD3}						
Operating power supply current	×1 speed	I_{DD5}	—	XI = 16.9344 MHz	—	2	5	mA
		I_{DD3}			—	40	50	
	×2 speed	I_{DD5}			—	2.5	6	
		I_{DD3}			—	45	55	
	×4 speed	I_{DD5}			—	3	7	
		I_{DD3}			—	50	60	
Input voltage 1	"H" level	V_{IH5}	—	CMOS input pins (5 V circuits) excluding analog input pins	3.5	—	—	V
	"L" level	V_{IL5}			—	—	1.5	
Input current 1	"H" level	I_{IH5}	—	V_{IH5} = 5 V	—	—	1.0	μA
	"L" level	I_{IL5}		V_{IL5} = 0 V	−1.0	—	—	
Tristate leak current 1	"H" level	I_{TLH5}	—	V_{IH5} = 5 V, Pins listed at (1), (2), and (3) in the following table.	—	—	1.0	μA
	"L" level	I_{TLL5}		V_{IL5} = 0 V	−1.0	—	—	
Output current 1	"H" level	I_{OH5}	—	V_{OH5} = 4.6 V, Pins listed at (1) in the following table.	—	—	−2.0	mA
	"L" level	I_{OL5}		V_{OL5} = 0.4 V	2.0	—	—	
	"H" level	I_{OH5}		V_{OH5} = 4.6 V, Pins listed at (2) and (3) in the following table.	—	—	−4.0	
	"L" level	I_{OL5}		V_{OL5} = 0.4 V	4.0	—	—	
Input voltage 2	"H" level	V_{IH3}	—	CMOS input pins (3 V circuits) excluding analog input pins	2.3	—	—	V
	"L" level	V_{IL3}			—	—	1.0	
Input current 2	"H" level	I_{IH3}	—	V_{IH3} = 3.3 V	—	—	1.0	μA
	"L" level	I_{IL3}		V_{IL3} = 0 V	−1.0	—	—	
Tristate leak current 2	"H" level	I_{TLH3}	—	V_{IH3} = 3.3 V, Pins listed at (4) and (5) in the following table.	—	—	1.0	μA
	"L" level	I_{TLL3}		V_{IL3} = 0 V	−1.0	—	—	
Output current 2	"H" level	I_{OH3}	—	V_{OH3} = 2.9 V, Pins listed at (4) in the following table.	—	—	−2.0	mA
	"L" level	I_{OL3}		V_{OL3} = 0.4 V	2.0	—	—	
	"H" level	I_{OH3}		V_{OH3} = 2.9 V, Pins listed at (5) in the following table.	—	−80	—	μA
	"L" level	I_{OL3}		V_{OL3} = 0.4 V	—	80	—	
	"H" level	I_{OH3}		V_{OH3} = 2.9 V, Pins listed at (6) in the following table.	—	−121	—	
	"L" level	I_{OL3}		V_{OL3} = 0.4 V	—	121	—	
V_{REF} output-on resistance		R_{ON}	—	—	—	—	500	Ω
Input amp feedback resistance		R_N	—	FGIN feedback resistance	1.0	—	3.0	MΩ
Pull-up resistance		R_{UP}	—	Pins listed at (8) in the following table.	25	50	75	kΩ
Output resistance integrated at pin		R_{O1}	—	Pins listed at (5) in the following table.	—	5.0	—	kΩ
		R_{O2}		Pins listed at (6) and (7) in the following table.	—	3.3	—	

DC characteristics (2)

(unless otherwise specified, V_{DD5} = V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = RV_{DD3} = PV_{DD3} =3.3 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Operating power supply voltage		V_{DD5}	—	—		3.0	3.3	3.6	V
		V_{DD3}							
		AV_{DD3}							
		DV_{DD3}							
		PV_{DD3}							
		RV_{DD3}							
		XV_{DD3}							
Operating power supply current	×1 speed	I_{DD5}	—	XI = 16.9344 MHz		—	2	5	mA
		I_{DD3}				—	40	50	
	×2 speed	I_{DD5}				—	2.5	6	
		I_{DD3}				—	45	55	
	×4 speed	I_{DD5}				—	3	7	
		I_{DD3}				—	50	60	
Input voltage 1	"H" level	V_{IH5}	—	CMOS input pins (5 V circuits) excluding analog input pins		2.5	—	—	V
	"L" level	V_{IL5}				—	—	0.8	
Input current 1	"H" level	I_{IH5}	—	V_{IH5} = 3.3 V	(VDD5 = 3.3 V)	—	—	1.0	μA
	"L" level	I_{IL5}		V_{IL5} = 0 V		−1.0	—	—	
Tristate leak current 1	"H" level	I_{TLH5}	—	V_{IH5} = 3.3 V	Pins listed at (1), (2), and (3) in the following table.	—	—	1.0	μA
	"L" level	I_{TLL5}		V_{IL5} = 0 V		−1.0	—	—	
Output current 1	"H" level	I_{OH5}	—	V_{OH5} = 2.9 V	Pins listed at (1) in the following table.	—	—	−2.0	mA
	"L" level	I_{OL5}		V_{OL5} = 0.4 V		2.0	—	—	
	"H" level	I_{OH5}		V_{OH5} = 2.9 V	Pins listed at (2) and (3) in the following table.	—	—	−2.0	
	"L" level	I_{OL5}		V_{OL5} = 0.4 V		2.0	—	—	
Input voltage 2	"H" level	V_{IH3}	—	CMOS input pins (3 V circuits) excluding analog input pins		2.3	—	—	V
	"L" level	V_{IL3}				—	—	1.0	
Input current 2	"H" level	I_{IH3}	—	V_{IH3} = 3.3 V		—	—	1.0	μA
	"L" level	I_{IL3}		V_{IL3} = 0 V		−1.0	—	—	
Tristate leak current 2	"H" level	I_{TLH3}	—	V_{IH3} = 3.3 V	Pins listed at (4) and (5) in the following table.	—	—	1.0	μA
	"L" level	I_{TLL3}		V_{IL3} = 0 V		−1.0	—	—	
Output current 2	"H" level	I_{OH3}	—	V_{OH3} = 2.9 V	Pins listed at (4) in the following table.	—	—	−2.0	mA
	"L" level	I_{OL3}		V_{OL3} = 0.4 V		2.0	—	—	
	"H" level	I_{OH3}		V_{OH3} = 2.9 V	Pins listed at (5) in the following table.	—	− 80	—	μA
	"L" level	I_{OL3}		V_{OL3} = 0.4 V		—	80	—	
	"H" level	I_{OH3}		V_{OH3} = 2.9 V	Pins listed at (6) in the following table.	—	−121	—	
	"L" level	I_{OL3}		V_{OL3} = 0.4 V		—	121	—	
V_{REF} output-on resistance		R_{ON}	—	—		—	—	500	Ω
Input amp feedback resistance		R_N	—	FGIN feedback resistance		1.0	—	3.0	MΩ
Pull-up resistance		R_{UP}	—	Pins listed at (8) in the following table.		50	80	120	kΩ
Output resistance integrated at pins		R_{O1}	—	Pins listed at (5) in the following table.		—	5.0	—	kΩ
		R_{O2}		Pins listed at (6) and (7) in the following table.		—	3.3	—	

Pin Group	Pin Name
(1) Pin	SBOK, SFSY, SBSY, IO0A~IO1A, ZDET
(2) Pin	BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA, IO0B~IO3B, EMPH
(3) Pin	BUS3, BUS2, BUS1, BUS0
(4) Pin	TMAX, TMAXS
(5) Pin	PDO
(6) Pin	FMO, DMO
(7) Pin	FOO, TRO, IO2A~IO3A
(8) Pin	/RST

AC characteristics
(unless otherwise specified, V_{DD5} = 5 V, V_{DD3} = AV_{DD3} = DV_{DD3} = XV_{DD3} = RV_{DD3} = PV_{DD3} = 3.3 V, Ta = 25°C)

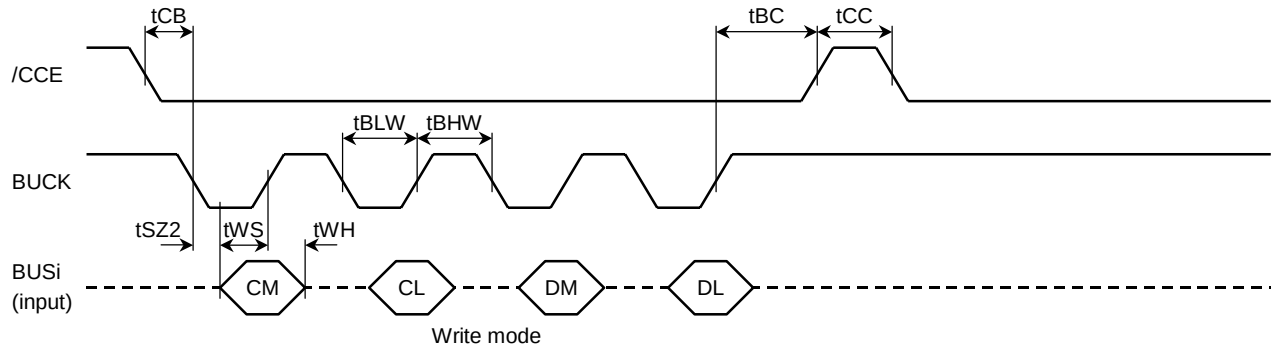
1. Microcontroller Interface

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
/CCE = “H” pulse width	tCC	—	—	120	—	—	ns
Data disable time	tSZ1	—	With reference to the BUCK rising edge	0	—	—	
/CCE, BUCK delay time	tCB	—	With reference to the /CEE falling edge	0	—	—	
BUCK-to-/CEE delay time	tBC	—	With reference to the BUCK rising edge	0	—	—	
BUCK = “L” pulse width	tBLW	—	Write, SRC mode	120	—	—	
	tBLW	—	QDRC, TEXT mode	240	—	—	
BUCHK = “H” pulse width (1)	tBHW	—	Write, SRC mode	120	—	—	
BUCHK = “H” pulse width (2)	tBHW	—	QDRC, TEXT mode (×1 speed)	3000	—	—	
BUCHK = “H” pulse width (3)	tBHW	—	QDRC, TEXT mode (×2 speed)	1500	—	—	
BUCHK = “H” pulse width (4)	tBHW	—	QDRC, TEXT mode (×4 speed)	800	—	—	
Write data set-up time	tWS	—	With reference to the BUCK rising edge	60	—	—	
Write data hold time	tWH	—	With reference to the BUCK rising edge	20	—	—	
Data disable time	tSZ2	—	With reference to the BUCK falling edge	0	—	—	
Read data access time	tRD	—	With reference to the BUCK falling edge	0	—	—	

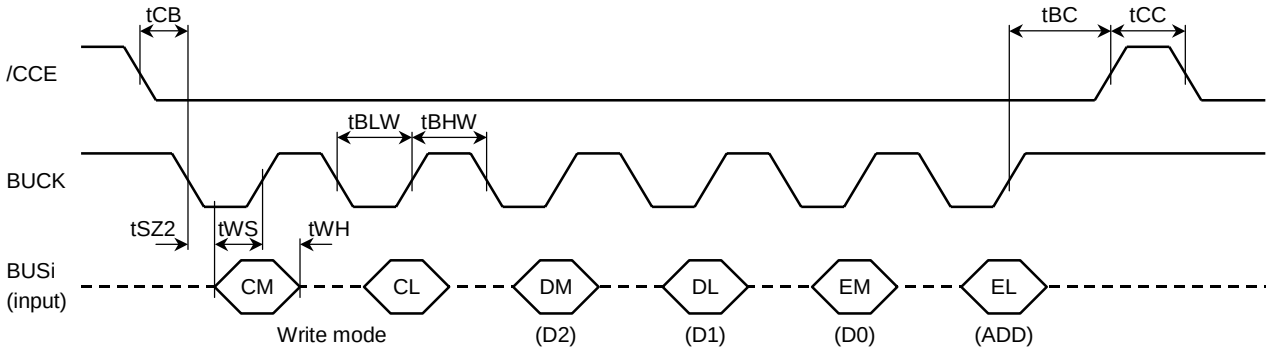
Supplement: Cautions about write command entry

No write command is taken into the microcontroller if the WBUSY flag in SRC5 is “H”. If you want to issue write commands one after another, make sure that the WBUSY flag is “L” before issuing each command. Read commands can be taken in no matter what the state of the WBUSY flag is. The WBUSY flag stays on the “H” level for up to 25 μs after a command is entered.
The system clock frequency must be 16.9344 MHz.

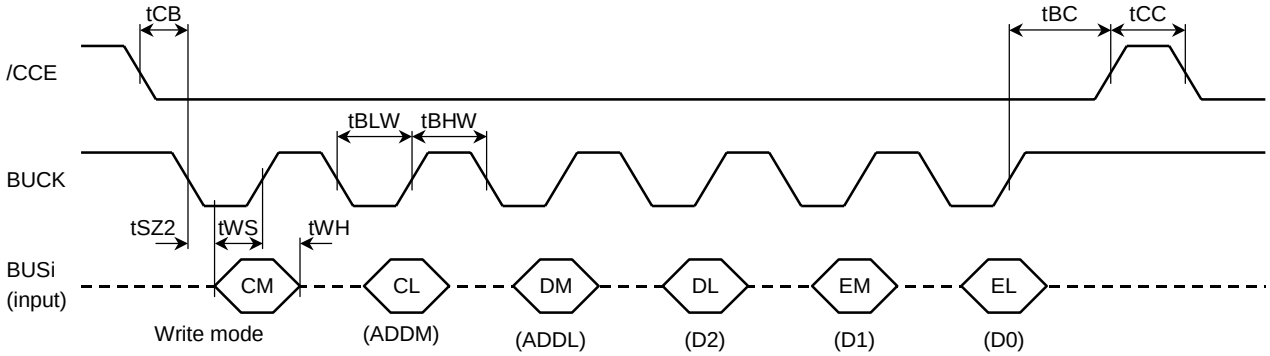
(1) Write command mode
4-word command



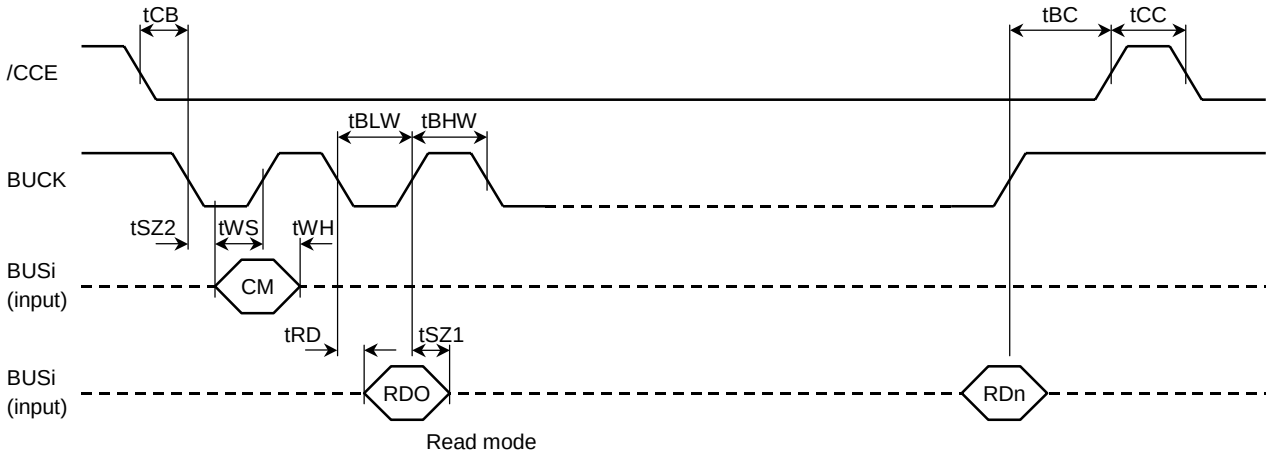
(2) Write command mode: D command in 6-word mode when DEXT = H
Six -word command



(3) Write command mode: Bxxxxx and Fxxxxx commands
Six -word command



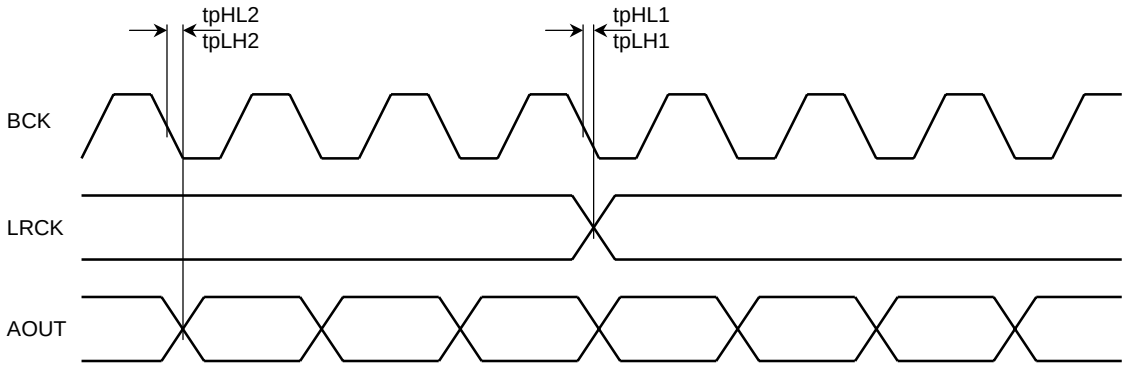
(4) Read command mode



Read mode

2. AOUT Data Output Timing

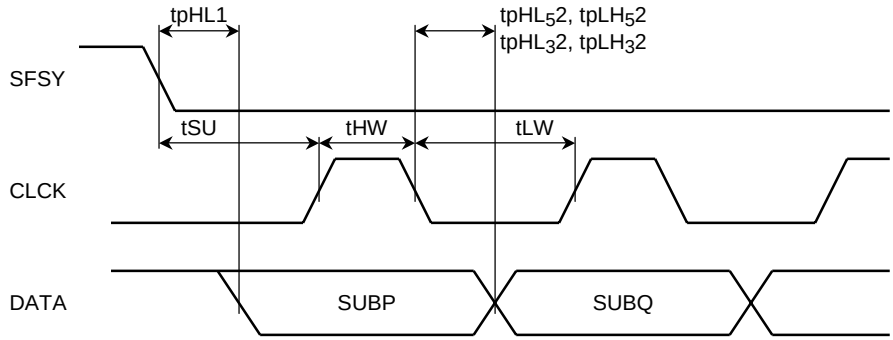
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer time (1)	“H” level	tpLH1	—	LRCK	—	—	5	ns
	“L” level	tpHL1	—		—	—	5	
Transfer time (2)	“H” level	tpLH2	—	AOUT	—	—	5	
	“L” level	tpHL2	—		—	—	5	



3. DATA and CLCK Input/Output Timing

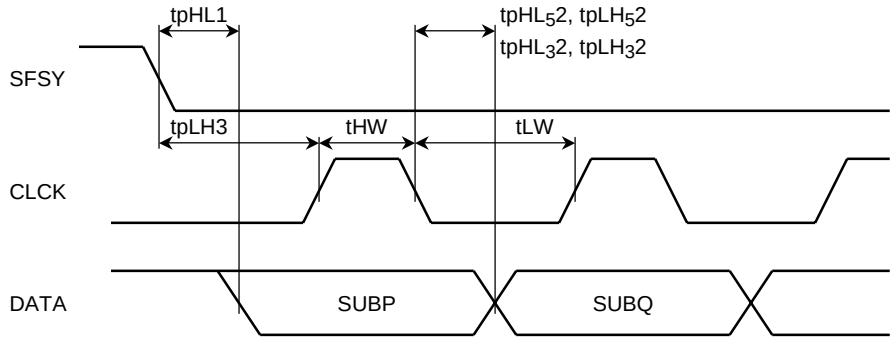
(1) CLCK input mode (constant no matter what the state of the HS and UHS bits of the SPEED command is)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	—	CLCK input mode	50	—	—	ns
	"L" level	tLW			50	—	—	
Input set-up time		tSU	—		400	—	—	
Transfer time (1)	"L" level	tpHL1	—		—	—	5	
Transfer time (2)	"H" level	$tpLH_52$	—		—	—	15	
	"L" level	$tpHL_52$			—	—	15	
	"H" level	$tpLH_32$		V_{DD5} = 3.3 V	—	—	20	
	"L" level	$tpHL_32$			—	—	20	



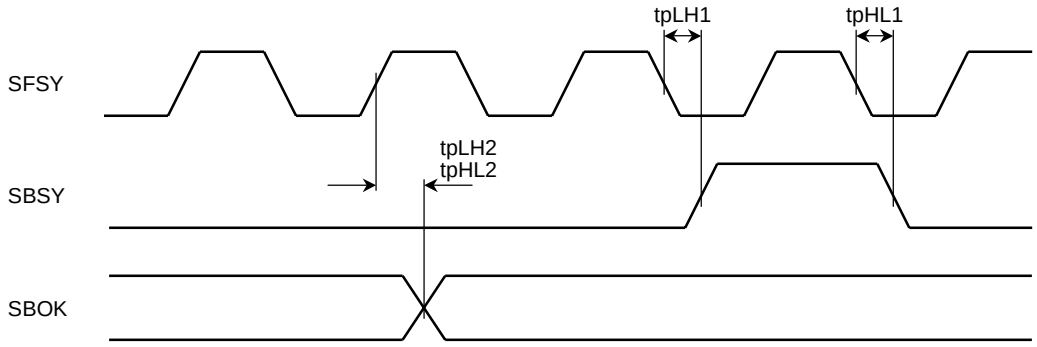
(2) CLCK output mode (only for tHW, tLW, and tpLH3, ×n speed × 1/n)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	—	CLCK output mode	—	—	950	ns
	"L" level	tLW			—	—	950	
Transfer time (1)	"L" level	tpHL1	—		—	—	5	
Transfer time (2)	"H" level	$tpLH_52$	—	CLCK input mode	—	—	15	
	"L" level	$tpHL_52$			—	—	15	
	"H" level	$tpLH_32$		V_{DD5} = 3.3 V	—	—	20	
	"L" level	$tpHL_32$			—	—	20	
Transfer time (3)	"H" level	tpLH3	—	CLCK output mode	—	—	850	



4. SBSY and SBOK Input/Output Timing

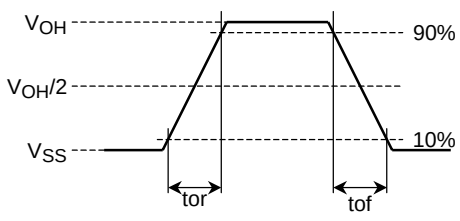
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer time (1)	"H" level	tpLH1	—	SBSY	—	—	5	ns
	"L" level	tpHL1			—	—	10	
Transfer time (2)	"H" level	tpLH2	—	SBOK	—	—	15	
	"L" level	tpHL2			—	—	20	



5. Output Pin Timing

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Rising time 5 (1)	$tor_5 1$	—	Pin (1)	—	—	7	ns
Falling time 5 (1)	$tof_5 1$	—		—	—	12	
Rising time 3 (1)	$tor_3 1$	—	V_{DD5} = 3.3 V	—	—	14	
Falling time 3 (1)	$tof_3 1$	—		—	—	24	
Rising time 5 (2)	$tor_5 2$	—	Pin (2)	—	—	7	
Falling time 5 (2)	$tof_5 2$	—		—	—	7	
Rising time 3 (2)	$tor_3 2$	—	V_{DD5} = 3.3 V	—	—	14	
Falling time 3 (2)	$tof_3 2$	—		—	—	14	
Rising time 5 (3)	$tor_5 3$	—	Pin (3)	—	—	7	
Falling time 5 (3)	$tof_5 3$	—		—	—	7	
Rising time 3 (3)	$tor_3 3$	—	V_{DD5} = 3.3 V	—	—	14	
Falling time 3 (3)	$tof_3 3$	—		—	—	14	
Rising time 5 (4)	$tor_5 4$	—	Pin (4)	—	—	10	
Falling time 5 (4)	$tof_5 4$	—		—	—	10	

Pin Group	Pin Name
Pin (1)	SBOK, SFSY, SBSY, IO0A~IO1A, ZDET
Pin (2)	BCK, LRCK, AOUT, DOUT, IPF, CLCK, DATA
Pin (3)	BUS3, BUS2, BUS1, BUS0
Pin (4)	TMAX, TMAXS



Analog Circuit Characteristics

1. AD Conversion Section

Characteristics		Test Circuit	Test Condition	Min	Typ.	Max	Unit
Resolution		—	—	—	10	—	bit
Sampling frequency	FE	—	—	—	176.4	—	kHz
	TE			—	176.4	—	
	SBAD(RFDC)			—	88.2	—	
	RFRP			—	176.4	—	
Conversation input range		—	AV_{SS} = 0 V AV_{DD3} = 3.3 V	0.15 × AV_{DD3}	—	0.85 × A_{VDD3}	V

2. DA Converter (Focus and Tracking Sections)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Bit number	—	—	—	5	—	bit
Sampling frequency	—	—	—	2.8	—	MHz
Output signal range	—	AV_{SS} = 0 V, AV_{DD3} = 3.3 V	AV_{SS3}	—	AV_{DD3}	V

3. PLL Section Filter Amp

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input/output signal range	—	—	PV_{SS3}	—	PV_{DD3}	V
Frequency characteristic	—	−3dB point (Gain = 1)	—	8	—	MHz

4. Active Wide-Range Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	—	—	PV_{SS3}	—	PV_{DD3}	V

5. AWRC (Active Wide-Range Control) Output DA Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Bit number	—	—	—	8	—	bit
Sampling frequency	—	—	—	88.2	—	kHz
Output signal range	—	—	AV_{SS3}	—	AV_{DD3}	V

6. VCO (PLL)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Oscillation center frequency	—	LPFO = VCOREF = V_{REF} VCOUP1 = “L” , VCOUP0 = “L”	—	69	—	MHz
Frequency variation range	—	VCOGS0 = “L”	—	±25	—	%
		VCOGS0 = “H”	—	±35	—	

7. VCO (Slice)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Oscillation center frequency	—	LPFO = VCOREF = V_{REF} VCOUP1 = "L", VCOUP0 = "L"	—	69	—	MHz
Frequency variation range	—	VCOGS0 = "L"	—	±25	—	%
		VCOGS0 = "H"	—	±35	—	

8. TEZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	—	—	AV_{SS3}	—	AV_{DD3}	V
Hysteresis voltage	—	V_{REF} reference	—	±50	—	mV

9. RFZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	—	—	AV_{SS3}	—	AV_{DD3}	V
Hysteresis voltage	—	V_{REF} reference	—	±50	—	mV

10. Data Slicer Circuit

(1) Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input amplitude	—	V_{REF} reference	0.6	1.2	2.0	V_{pp}

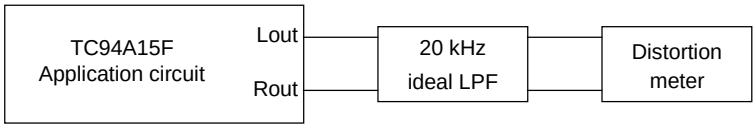
(2) R-2R DAC (DAC for digital slicer)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output conversation range	—	—	3/4 V_{REF}	—	5/4 V_{REF}	V
Output impedance	—	—	—	2.5	—	kΩ

11. Audio DAC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Noise distortion factor	THD + N (1)	1	1 kHz sine wave, full scale input.	—	−88	−80	dB
	THD + N (2)		10 kHz sine wave, full scale input.	—	−80	−75	
S/N ratio	S/N (1)	1	Internal zero detection off	87	92	—	dB
	S/N (2)		Internal zero detection on	95	100	—	
Dynamic range	DR	1	1 kHz sine wave, −60 dB input conversion	85	90	—	dB
Crosstalk	CT	1	1 kHz sine wave, full scale input.	—	−90	−85	dB
Analog output amplitude	DACout	1	1 kHz sine wave, full scale input.	790	820	850	mVrms

Test circuit 1: The application circuit shown in the following example is used.

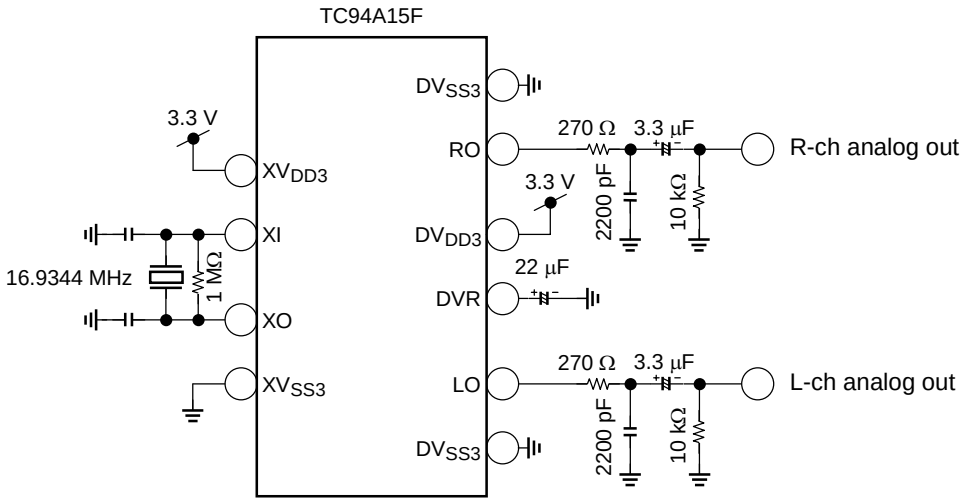


LPF: Filter incorporated in the SHIBASOKU distortion meter 725D.
Distortion meter: SHIBASOKU 725D or equivalent.

Characteristics	Distortion Filter Setting: A-weight
THD + N, CT	OFF
S/N, DR	ON

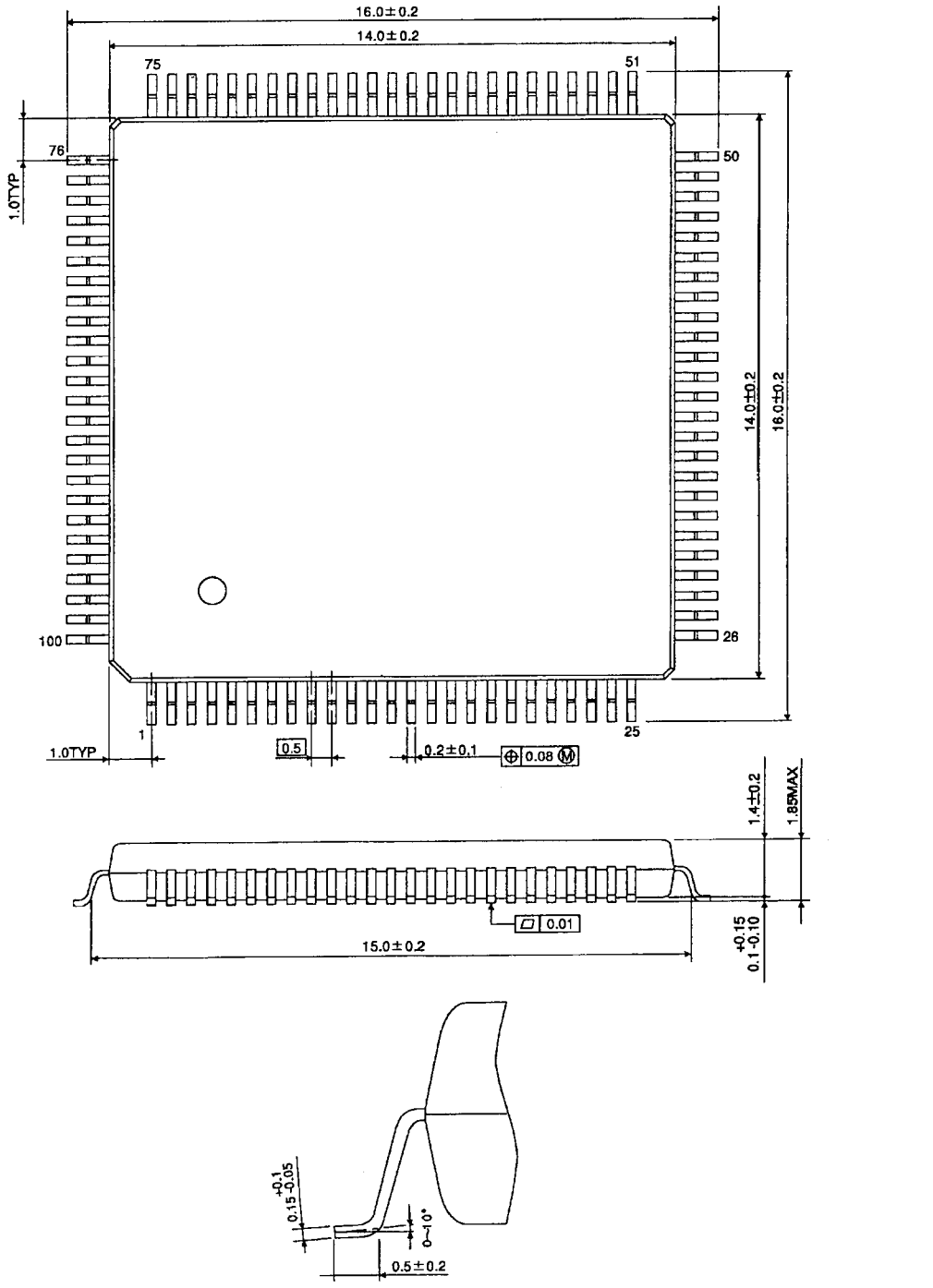
A-weight: IEC-A or equivalent

Application circuit example



Package Dimensions

LQFP100-P-1414-0.50C Unit : mm



Weight: 0.65 g (typ.)

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